An Analog CMOS Double-Edge Multi-Phase Low-Latency Pulse Width Modulator

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Abstract-**This paper presents an analog CMOS double-edge multi-phase low-latency pulse width modulator. The PWM signal is generated by comparing the phase difference between two matched ring oscillators, which are differentially driven by the command voltage and the feedback voltage developed in a minor loop that forces the average frequency of each of the oscillators to be equal. Both rising and falling edges of the PWM signal are controlled by the instantaneous input voltage, resulting in a low latency relative to that achieved with conventional latched PWM circuitry. The developed pulse width modulator has high precision, good linearity, good noise immunity and wide duty ratio range. Further, it can be flexibly reconfigured for multi-phase PWM operation with no restriction on duty cycle range. The complete double-edge pulse width modulator IC is implemented in a 0.18 μm CMOS process. It can generate as many as sixteen PWM outputs. The active chip area is 0.04 mm^2. The quiescent bias current of the chip is 80 μA at 1.2 MHz PWM frequency.**

I. INTRODUCTION

A multi-phase double-edge pulse width modulation (PWM) scheme with low latency is important for achieving fast controller response for high bandwidth applications, such as those arising in applications like microprocessor voltage regulator modules [1] or dynamic power supplies for RF power amplifiers [2]. Although, the required functionality might be realized with a conventional ramp-comparator modulator, such a modulator imposes a maximum duty cycle of 1/N, where N is the number of phases. Another embodiment of the conventional ramp-comparator modulator to realize multi-phase operation without the duty cycle constraint requires N comparators and N uniformly skewed ramp signals. The modulator described in this paper realizes all the desired features in a single simple circuit cell.

This paper presents an analog multi-phase double-edge pulse width modulator suitable for implementation in CMOS technology. The PWM signal is generated by comparing the phase difference between two matched ring oscillators, each of which functions as a current-controlled oscillator. These two matched oscillators are fed by the currents developed in a differential input stage. This balanced input stage is driven by the command voltage waveform, and a feedback voltage developed in a minor loop that forces the average frequency of each of the current-controlled ring oscillators to be equal. The minor loop constrains the duty ratio of the PWM signal to be proportional to the input modulation voltage over the full bandwidth of the minor loop. Both rising and falling edges of the PWM signal are controlled by the instantaneous input voltage, resulting in a low latency relative to that achieved with conventional latched PWM circuitry. The developed pulse width modulator has high precision, good linearity, good noise immunity and wide duty ratio range. Further, it can be flexibly reconfigured for multi-phase PWM operation with no restriction on duty cycle range.

II. CONCEPT OF OPERATION

A simplified schematic of the ring-oscillator-based pulse-width modulator is shown in Fig. 1. A matched pair M_{P1}-M_{P2} drives two identical ring oscillators as a matched load. As illustrated in Fig. 1(b), the phase difference of the two oscillators is detected by a phase comparator, the output of which is used as the PWM signal. This phase-sensitive signal is then passed through a low pass filter (LPF), aimed at removing ripple, with the resulting signal V_{FB} applied to the differential pair in an internal feedback loop. In steady state, the voltage V_{FB} which is proportional to the duty cycle, is forced to be equal to the command voltage V_{in} by the minor feedback loop. When the command modulation voltage V_{in} increases, the error voltage between V_{in} and V_{FB} develops differential current in the two ring oscillators that results in instantaneous differential frequency and phase shift as shown in Fig. 1(c). The resulting phase difference of the two ring oscillators is increased until the signals V_{in} and V_{FB} are equal. When the command modulation voltage V_{in} decreases, as shown in Fig. 1(d), the phase difference of the two ring oscillators is decreased until the voltages V_{in} and V_{FB} are equal. As both edges of the output PWM signal are modulated by the input command voltage V_{in}, the behavior of this ring-oscillator-based pulse width modulator is similar to a double-edge PWM modulator. The phase difference of two ring oscillators is actually equal to the time integral of the differences of the two ring oscillator frequencies, which is proportional to the error voltage. Therefore, integration inherently takes place in the loop and any high frequency noise or glitch at the input is filtered, suppressing false transitions. Instead of comparing the phase difference once per switching period, M uniformly spaced taps on each respective ring oscillator are compared in a multi-phase phase comparator, reducing latency and increasing the phase comparator ripple frequency. Further, uniformly spaced

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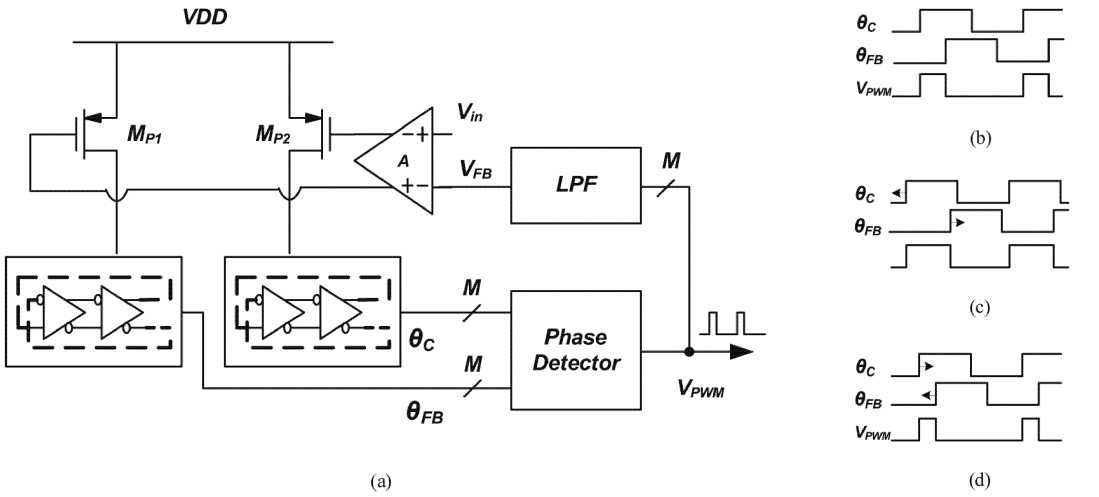


Figure 1. (a) Simplified schematic of ring-oscillator-based pulse-width modulator (b) Steady state switching waveforms (c) Switching waveforms as input control voltage increases (d) Switching waveforms as input control voltage decreases.

multi-phase PWM signals are available from the multi-phase phase comparator. A multi-input low pass filter is applied to suppress ripple in the minor loop.

Ignoring the nonlinearity of the input differential pair and phase comparator, a linear model representing the ring-oscillator-based pulse-width modulator is shown in Fig. 2. This model consists of the input differential pair with transconductance G_m, the phase comparator modeled as a gain term K_{PD}, the low pass filter (LPF) with -3dB frequency ω_{LPF}; the buffer with voltage swing of V_{DD} to drive the low pass filter; and the current-starved ring oscillator modeled as an integrator 1/S with the gain K_{OSC} [3]. The closed-loop transfer function of the pulse-width modulator is given by

$$\frac{D}{V_{in}} = \frac{K_{OSC}K_{PD}G_m(s+\omega_{LPF})}{s^2+\omega_{LPF}s+K_{OSC}K_{PD}G_mV_{DD}\omega_{LPF}} \qquad (1)$$

This corresponds to a second-order feedback loop with two open-loop poles given by $p_1 = 0$ and $p_2 = \omega_{LPF}$. As the loop gain further increases, the two poles become complex with real part equal to $-\omega_{LPF}/2$ and move parallel to the jω-axis. The loop gain, which is equal to $K_{OSC}K_{PD}G_mV_{DD}$, is designed such that the loop has large bandwidth for fast dynamic response and enough phase margin so as not to cause significant overshoot in the step response. Since there is one open-loop pole at the origin, the loop gain goes to infinity as $s \rightarrow 0$ which ensures that the error voltage goes to zero in steady state. In equation 1, by making $s \rightarrow 0$, the duty cycle of the pulse width modulator output is given by

$$D = V_{in} / V_{DD} \qquad (2)$$

which is proportional to the input control voltage V_{in}.

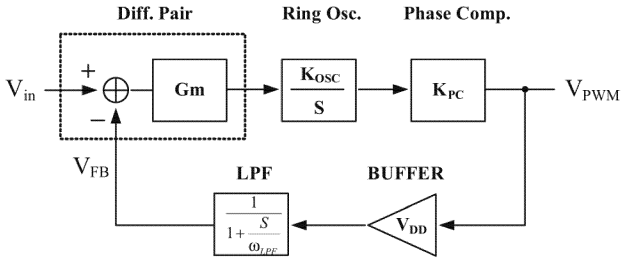


Figure 2. Linear model of the ring-oscillator based pulse-width modulator

III. CIRCUIT IMPLEMENTATION

A. Input Stage

The input stage compares the voltage difference between the command V_{in} and the feedback voltage V_{FB}, and converts voltage into current to bias the ring oscillators. There are several design considerations regarding the input stage of this ring-oscillator-based pulse-width modulator. First, the input stage should not saturate with large differential voltage as saturation would significantly limit the transient response of the modulator. Second, the transconductance of the input stage should be large enough to achieve the desired loop bandwidth, and be well controlled to keep good phase margin. Finally, the quiescent current supplied to the ring oscillator must be well controlled as it determines the nominal ring oscillator frequency, which is the same as the PWM switching frequency. Based on the above considerations, common-source transistor M_{P1} and M_{P2} together with a pre-amplifier [4] are used as the input stage, as shown in Fig. 3(a). The whole input stage is symmetric and Fig. 3(b) shows half of the

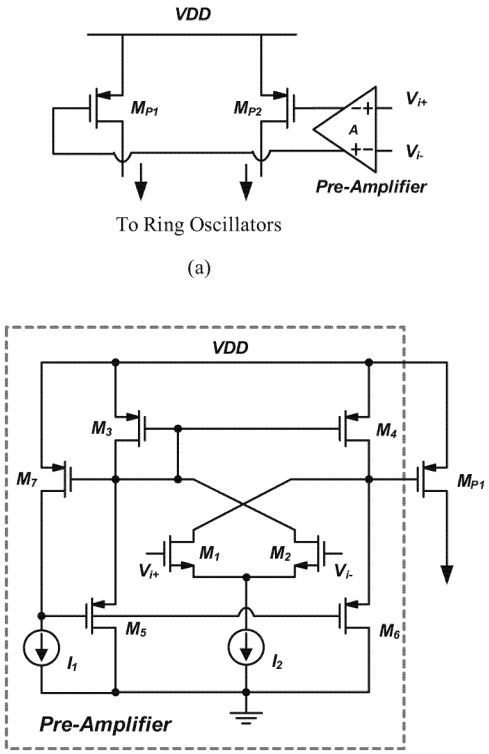


Figure 3. (a) Simplified schematic of the input stage (b) Half-circuit of the pre-amplifier.

circuit. The error voltage at the input is sensed by differential pair M_1 and M_2, which is biased by the tail current source I_2. Common drain transistors M_5 and M_6 are in parallel with the current mirror load M_3 and M_4 to reduce the output resistance so that the gain of the error amplifier can be set to a well-defined value. The negative feedback loop, including transistors M_3, M_5, M_7 and current source I_1, adjusts the gate voltage of M_5 such that M_7 operates in the active region and conducts I_1. It can be shown that the quiescent bias current of M_{P1} is given by

$$I_{D,M_{P1}} = I_1 \frac{(W/L)_{P1}}{(W/L)_7} \tag{3}$$

and the overall transconductance of the input stage is

$$G_m = \frac{g_{m1}}{g_{m6}} g_{m,M_{P1}} \tag{4}$$

Compared to the conventional differential pair, this input stage provides a large relative constant transconductance over a wide range of differential input voltage, and the quiescent bias current of M_{P1} can be precisely controlled by current source I_1.

B. Ring Oscillator

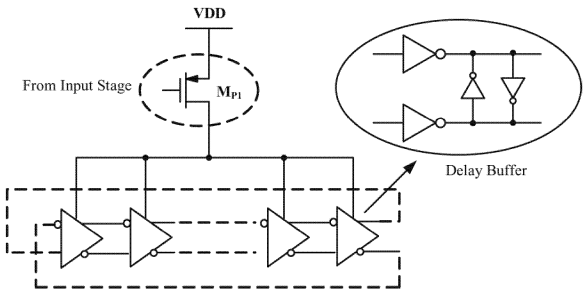


Figure 4. Simplified schematic of the ring oscillator

A current starved differential ring oscillator similar to the design in [5] is used here for its small area and low power consumption. As shown in Fig. 4, the supply current to the ring oscillator is generated by the common source transistor M_{P1} from the input stage. The differential delay buffer in the ring oscillator is a pair of inverters with outputs coupled by weak cross-coupled inverters, aiming at minimizing the delay skew between two paths. The voltage swing on the ring oscillator is below the threshold of the MOSFET, which gives the ring oscillator a good linear dependency of the oscillation frequency on the supply current [5].

C. Phase Comparator

The phase comparator compares the phase difference of the two ring oscillators and the PWM signal is taken from the output. The phase comparator is designed to have comparison range from 0 to 2π, linearly corresponding to 0 to 100% duty ratio. When the instantaneous phase difference exceeds the 0 to 2π range, the duty cycle should saturate to 0 or 100% to avoid wind-up. The problem with this saturating phase detection scheme is that the frequency of the two oscillators will lose lock if the phase difference exceeds the 0 to 2π range, as more feedback voltage will have to be applied to the input differential pair in order for the oscillator phase to shift accordingly. However, the phase comparator can produce no more dc output voltage to shift the oscillator frequency further, as the duty ratio reaches 0 or 100%, so the loop will lose lock.

To resolve this frequency tracking problem, a phase and frequency detection scheme is developed as shown in Fig. 5(a). A phase-frequency comparator compares the phase and frequency difference of two ring oscillators, and the PWM signal is taken from the output. Instead of feeding back the DC component of the PWM signal, a four level signal V_{int} as shown in Fig. 5(b) is developed from the phase comparator to close the internal feedback loop. When the phase difference is within 0 to 2π range, V_{LP} swings between V_L and V_H, linearly corresponding to 0 to 100% duty ratio. When the phase difference becomes negative, V_{LP} swings between 0 and V_L, providing extra voltage to pull the phase difference of the two

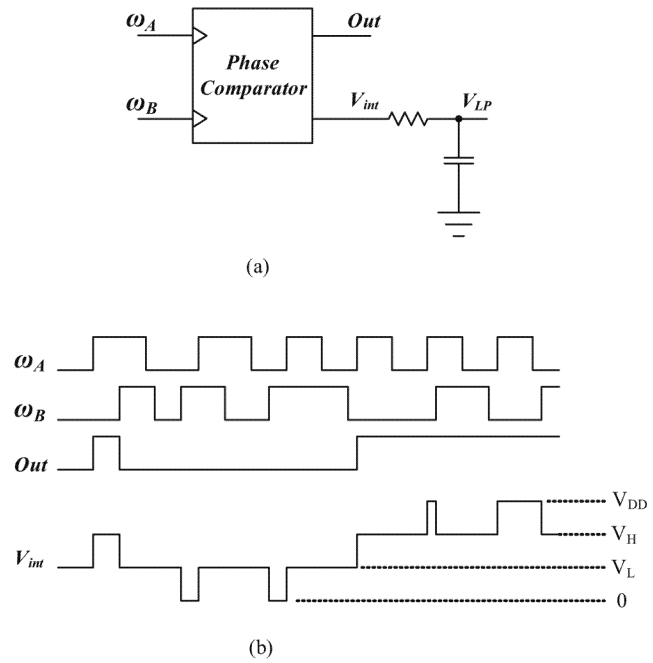


Figure 5. Proposed phase frequency detection scheme.

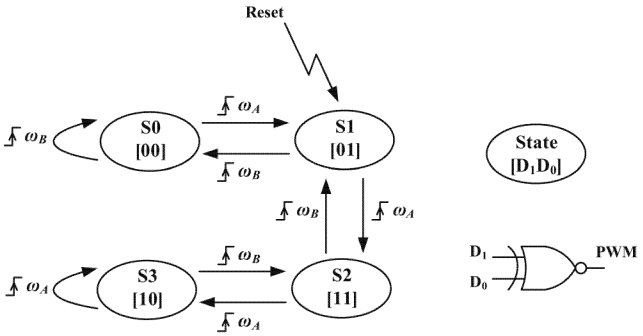


Figure 6. State transition diagram of the phase frequency comparator state machine.

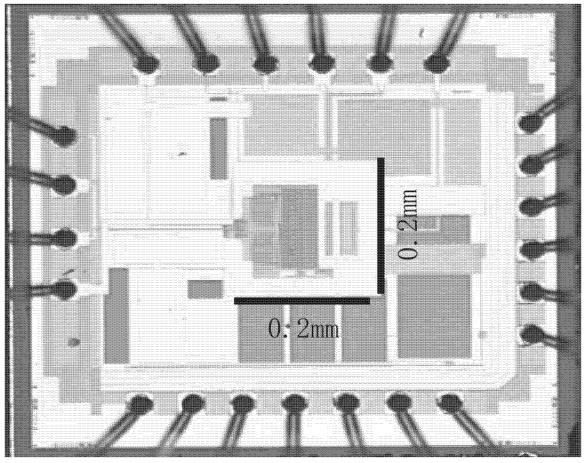


Figure 7. Chip micrograph.

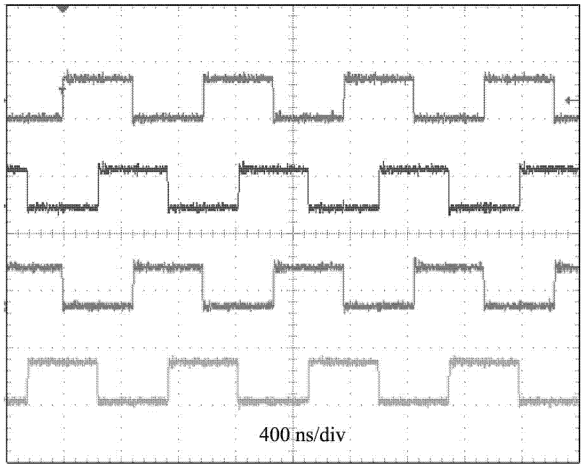


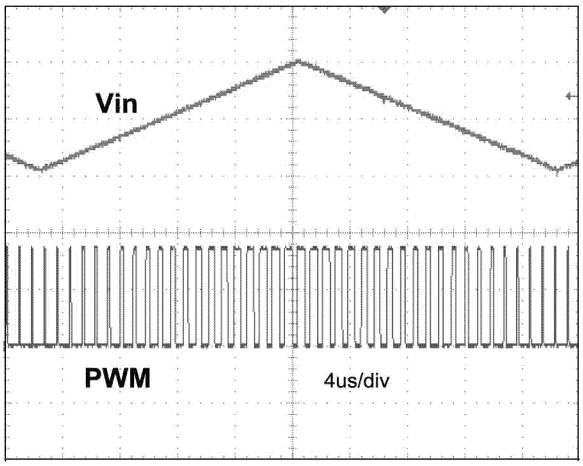
Figure 8. Four symmetric PWM output signals

ring oscillators back to zero and keep the loop locked. An analogous case applies when phase difference exceeds 2π, V_{LP} swings between V_H and V_{DD}, providing extra voltage room on the feedback node to keep the loop in lock.

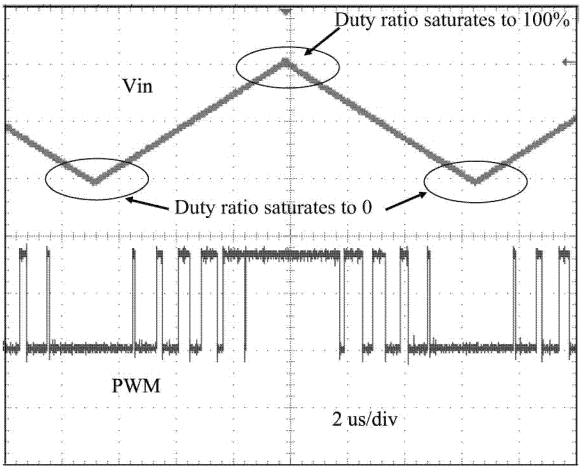
The proposed phase and frequency detection scheme is implemented by using a state machine with the state transition diagram shown in Fig. 6. A state transition occurs only when the rising edge of either one of the frequency inputs is detected by the phase comparator. When the phase difference is within the normal 0 to 2π range, transitions only occur between states S_1 and S_2. When the state machine receives two consecutive rising edges from either one of the frequency inputs, meaning the phase difference exceeds the 0 to 2π range, the state machine will transition to a saturation state, with S_0 and S_3 corresponding to the case of phase difference below 0 or above 2π, respectively. The PWM signal is taken by combining the two bits of the state in a XNOR gate. A set of M such phase frequency comparators are used to compare all the taps from two ring oscillators to reduce the latency. A multi-input low pass filter is used to reduce the ripple voltage and increase the loop bandwidth.

IV. EXPREIMENTAL RESULTS

The complete double-edge pulse width modulator IC is implemented in a 0.18 μm CMOS process. The die photo of the chip is shown in Fig. 7. The active chip area is 0.04 mm^2. It can generate as many as sixteen PWM outputs. Fig. 8 shows four of sixteen symmetric PWM output signals. The quiescent bias current of the chip is 80 μA at 1.2 MHz PWM frequency, and much higher PWM frequency is possible by



(a)



(b)

Figure 9. Experimental time domain response of the modulator to a triangle input voltage (a) no duty ratio saturation (b) with duty ratio saturates to both 0 and 100%.

increasing the bias current of the ring oscillator.

Fig. 9(a) shows the time domain response of the modulator to a triangle input voltage command V_{in} without duty ratio saturation. The functionality of the proposed phase comparator is verified by applying a large triangle voltage command V_{in} at the input and forcing the duty ratio of the PWM signal to saturate to zero and 100%. Fig. 9(b) shows the corresponding time domain response of the modulator output. The modulator is able to generate PWM signal with zero and 100% duty ratio and recover from each saturation state to normal operation. Fig. 10 gives the measured output PWM duty ratio versus input voltage command V_{in}, showing the good linearity of the pulse-width modulator. The low-latency double-edge modulation characteristic is verified by applying a large step voltage at the input. A negative step input voltage

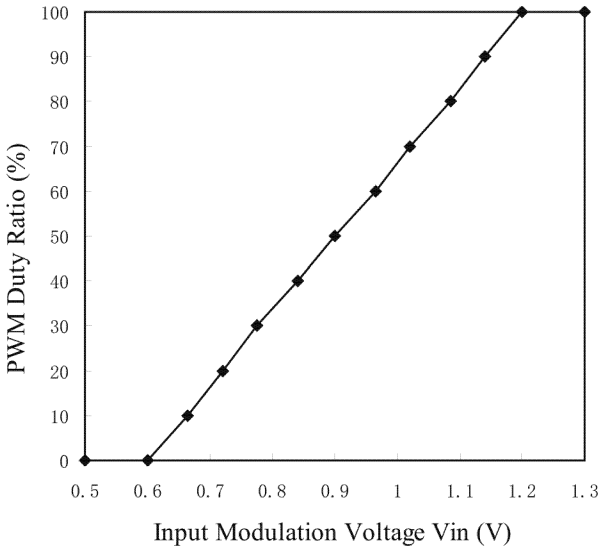
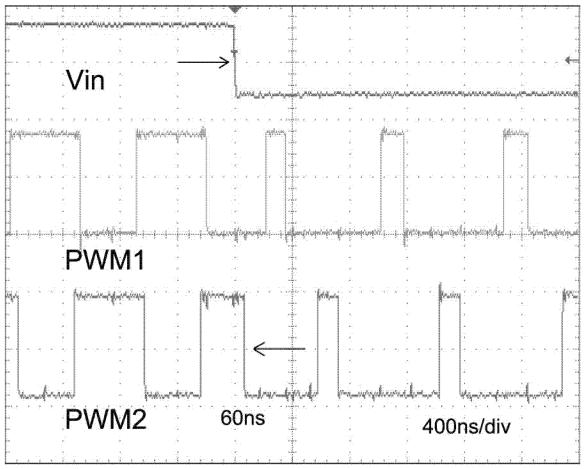


Figure 10. Measured transfer characteristic of PWM duty ratio versus input voltage.

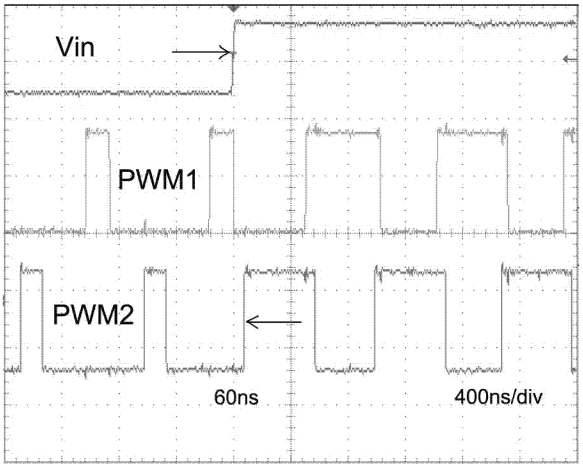
and two of the sixteen PWM output signals (with 180 degree phase shift) are shown in Fig. 11(a). The period of the PWM signal is approximate 880ns. The falling edge of PWM_2 is generated right after applying the voltage step at the input with 60ns delay. The response to a positive step input voltage is shown in Fig. 11(b). The rising edge of PWM_2 is generated right after applying the voltage step at the input with 60ns delay. As seen, both edges of the PWM signal are modulated by the input voltage and the designed PWM modulator provides fast transient response.

V. CONCLUSION

A CMOS double-edge pulse-width modulator has been demonstrated in this paper. The PWM signal is generated by comparing the phase difference between two ring oscillators, which are driven by the input command voltage and a feedback voltage developed in a minor feedback loop that forces the average frequency of the two oscillators to be equal. A multi-state phase frequency detection scheme is developed to keep the frequency of two oscillators always in lock. Both rising and falling edge of the PWM signal are controlled by the instantaneous input voltage, resulting in a low latency relative to that achieved with conventional PWM circuitry. The fast transient response, good re-configurability, good linearity and noise immunity, low power and low cost make it an attractive pulse width modulator candidate for integrated power management ICs.



(a)



(b)

Figure 11. Experimental transient response of the pulse-width modulator (a) applying step down voltage at input (b) applying step up voltage at input.

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