A Digital Multi-Mode Multi-Phase IC Controller for Voltage Regulator Application

Jianhui Zhang Seth R. Sanders
University of California, Berkeley
Berkeley, CA 94720, USA
zhangjh, sanders@eecs.berkeley.edu

Abstract-**This paper presents a digital multi-mode multi-phase IC controller for the voltage regulator application. The IC controller combines load current feedforward with a load-scheduled digital PID feedback control to achieve a fast load transient response. The multi-mode control strategy is applied in the designed controller IC, allowing high efficiency operation of a voltage regulator over a wide load range. A high resolution 13-bit digital pulse width modulator (DPWM) and 4mV quantization bin analog-to-digital converter (ADC) is implemented in the IC controller to ensure tight DC regulation of the regulator. The prototype 4-phase IC controller takes 0.5 mm^2 active area in a 0.18 μm CMOS process.**

I. Introduction

The scaling of CMOS technology has posed significant challenges to power management circuits of today's high performance processors for both accurate and efficient power delivery. Requirements for tight voltage tolerance, fast transient response, and high efficiency operation over a wide load range for portable applications present challenges to microprocessor voltage regulator module (VRM) design. This paper presents a digital multi-mode 4-phase IC controller for the microprocessor VRM application. The IC controller combines load current feedforward [1] with load-current-scheduled PID feedback control to achieve fast load transient response over the multiple modes of operation. The multi-mode control strategy is applied in the designed controller IC, allowing high efficiency operation of a VRM over a wide load range. A 120ps resolution digital pulse width modulator (DPWM) and 4mV quantization bin analog-to-digital converter is implemented in the IC controller to enable tight DC regulation.

As shown in Fig. 1, the controller IC combines a voltage feedback loop and a load current feedforward control. The use of load current feedforward extends the useful bandwidth beyond the limits imposed by feedback stability constraints, which improves the load transient response of the voltage regulator (VR) [1]. The output V_{out} and load line voltage V_{ref} - I_{out}*R_{ref} are directly combined in the analog domain at the ADC input of the feedback loop. The total duty ratio commands are obtained by combining the output of the digital PID compensation network and feedforward control. A multi-mode control strategy is applied in the designed controller. The optimal synchronous rectifier (SR) timing is scheduled as a function of the load current and stored in a look up table. Depending on the load current, transitions among continuous conduction mode (CCM) and discontinuous conduction mode (DCM) occur automatically by timing the SR switch appropriately, and by suppressing gate pulses to effect pulse skipping. The details of load current feedforward and multi-mode control are presented in Section II.

The digital pulse width modulator (DPWM) module takes the duty ratio command and the SR timing as inputs and converts this data into four-phase PWM and SR signals that control the high side and low side switches. In order to achieve tight voltage regulation, a high resolution 13-bit DPWM is designed with effective 1.5mV step size. The ADC quantization step size is designed to be 4mV to avoid sub-harmonic limit cycling [2]. The details of the circuit implementation are discussed in Section III.

A prototype multi-mode 4-phase digital-controlled VRM controller is implemented in a 0.18 μm CMOS process. The active area of the chip is about 0.5 mm^2. The multi-mode operation improves the converter efficiency by at least a factor of ten in light load condition. Combined load current feedforward and load-scheduled digital PID control enable fast and glitch-free large-signal load transient response. The experimental results are detailed in Section IV.

II. Architecture

A. Load Current Feedforward Control

The specifications for modern microprocessor voltage regulators (VR's) require that the microprocessor supply voltage follows a prescribed load line with a slope of about one milliohm [3]. This requires tight regulation of the voltage regulator output impedance. The method of using load-current feedforward to extend the useful bandwidth beyond the limits imposed by feedback stability constraints has been proposed in [1]. With this approach, feedforward is used to handle the bulk of the regulation action, while feedback is used only to compensate for imperfections of the feedforward and to ensure tight DC regulation. In this case, the size of the output capacitor is determined by large signal transient and switching-ripple considerations, and not by a feedback stability constraint.

In [1], load current feedforward control is developed in a continuous-time analog framework, as shown in Fig. 2, and

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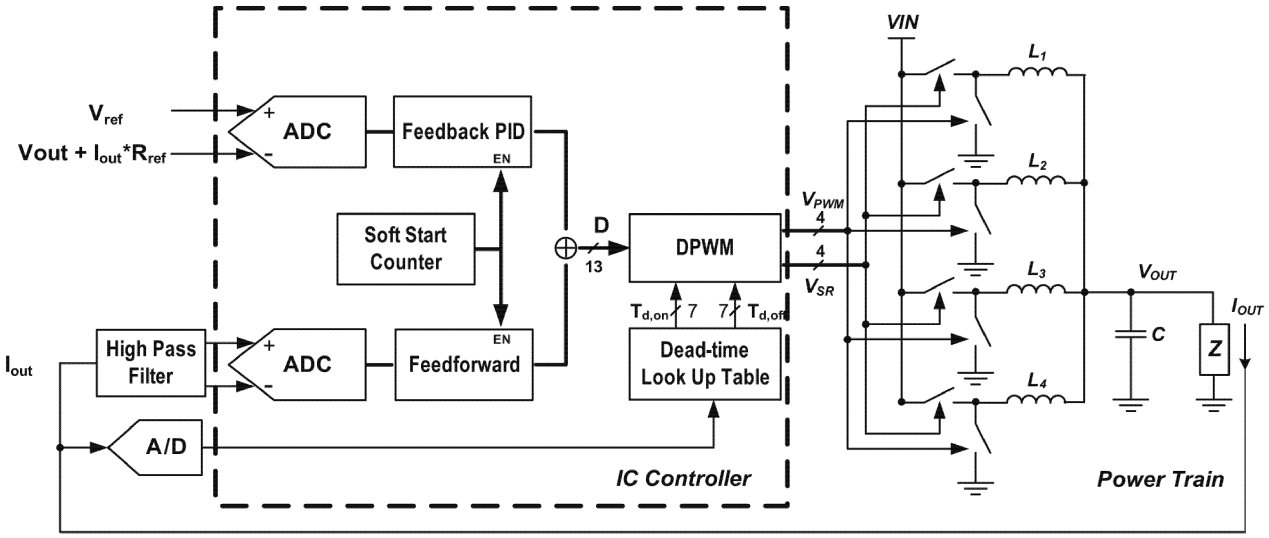


Figure 1. Block diagram of multi-mode multi-phase buck converter controller IC and external power train.

the feedforward control law can be approximated as

$$H_{FF}(s) \approx \frac{sL}{sR_{ref}C+1} \tag{1}$$

where R_{ref} is the load line reference impedance. Low latency associated with the load current feedforward control is essential for achieving a fast controller response.

There are several technical issues when applying load current feedforward to a discrete-time, digital control implementation by directly sampling and processing the load current in the digital domain. Most significantly, the aggressive load current transient (with slew rate of 1 A/ns [3]) requires fast sampling and processing of the load current. Another issue is the large dynamic range required by directly quantizing the load current over a wide load range.

Fig. 3 shows the discrete time, digital implementation of feedforward control. To relax the sampling speed requirement and reduce the latency associated with the processing of load current in digital domain, most of the feedforward control law is implemented in the analog domain by using a simple RC type high pass filter with transfer function

$$H(s) = \frac{sRC/2}{sRC/2+1} \tag{2}$$

Ignoring the sampling and processing delay, the feedforward control law will be equivalent in the analog and digital implementations by matching the RC time constants in equation 1 and equation 2, and by adjusting the feedforward gain K_{FF} in the digital domain, which can be done by a simple digital multiplication. The total duty ratio commands is obtained by combining the output of the feedback compensator D_{FB} and feedforward control D_{FF}. The sampling

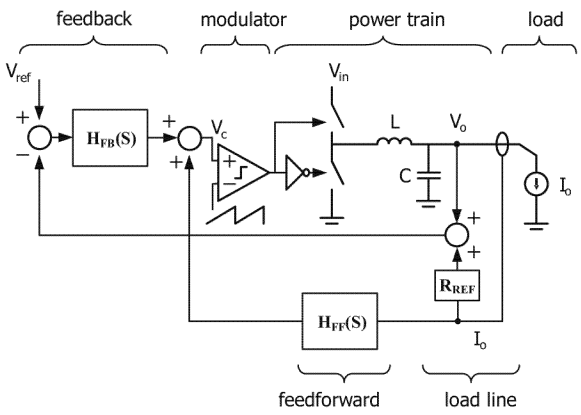


Figure 2. Block diagram of a buck converter with load current feedforward control

speed of the feedforward ADC is determined by the duty cycle command update rate in the DPWM module. In the prototype IC, the sampling rate of the feedforward control is set to 4 MHz, which is equal to the update rate of the DPWM module. Since the dc level of the feedforward signal is blocked by the high pass filter, a simple low-resolution windowed ADC structure [4] can be used to quantize it, and the imperfection of the feedforward control due to the sampling delay and the moderate quantization resolution is compensated by the feedback loop.

B. Multi-Mode Operation

A single phase synchronous buck converter with corresponding high side and low side switch control signals is

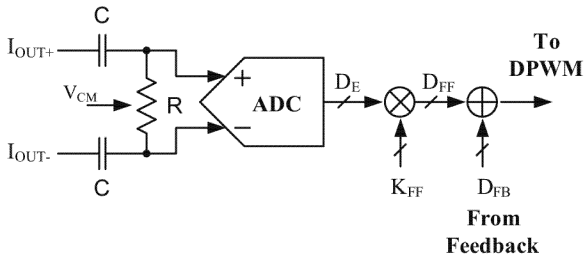


Figure 3. Block diagram of feedforward control in digital controller

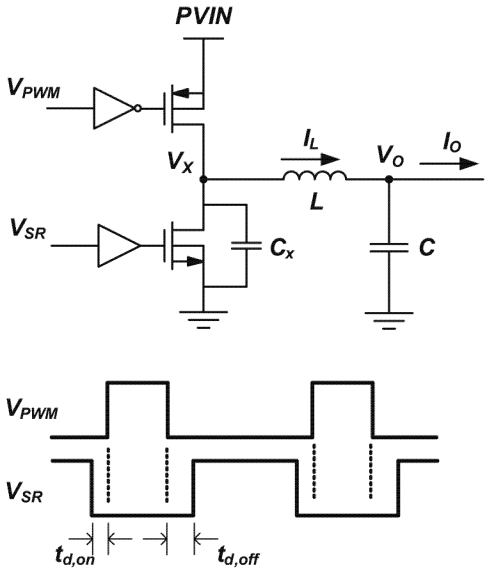


Figure 4. Synchronous buck converter and corresponding control signals

shown in Fig. 4. Under different load conditions there are different optimal gating patterns for the switches. To ensure high efficiency operation over a wide load range, the buck converter can be operated in different modes depending on the load current.

When the load current is high, the converter runs in fixed frequency continuous conduction mode (CCM). Ignoring the delay of the switch, the optimal turn-off dead time $t_{d,off\text{-}opt}$ depends on the time it takes to discharge the switching node capacitance C_x [5],

$$t_{d,off-opt} = \frac{V_{in} C_x}{I_O} \tag{3}$$

The optimal turn-on deadtime $t_{d,on\text{-}opt}$ is a small constant, to prevent conduction overlap between the control switch and the synchronous rectifier (SR) switch.

When the load current is light, i.e.

$$I_o < \frac{V_o T_s (V_{in} - V_o)}{2 V_{in} L} \tag{4}$$

the converter enters discontinuous conduction mode (DCM), where the low side SR is gated such that inductor current is zero during part of the switching period. The duty ratio depends on the load current,

$$D = \sqrt{\frac{2LI_o V_o}{T_s V_{in} (V_{in} - V_o)}} \tag{5}$$

The optimal $t_{d,on\text{-}opt}$ is equal to the time the inductor current is zero,

$$t_{d,on-opt} = T_s \left(1 - \frac{DV_{in}}{V_{out}}\right) \tag{6}$$

At very light load, the power loss is dominated by the switching loss and proportional to the switching frequency. It is advantageous to allow variable frequency operation at very light loads. This is done by setting a minimum duty ratio D_{min} in the digital controller. When the duty ratio command is less than D_{min}, the PWM pulse will be skipped and the effective switching frequency is reduced.

As discussed above, transitions among different operation modes occur automatically by timing the SR switch appropriately based on the load current. Experiments [6] show that there is a broad minimum in the power loss versus SR timing curve, and only moderate precision timing data is required. Therefore, it is straightforward to program the optimal SR timing obtained from off-line power loss measurement into a dead-time look up table, scheduling as a function of the load current.

C. Load-Scheduled Integrator Array

When a buck voltage regulator runs in discontinuous conduction mode (DCM), from equation 5, the steady-state duty-ratio command varies substantially as a function of the load current, unlike in CCM where it is ideally constant. The load transient response may be slow since the integrator has to slew over a wide range. An adaptive scheme in the digital feedback compensation network is applied to resolve this problem. As shown in Fig. 5, instead of a single integrator in

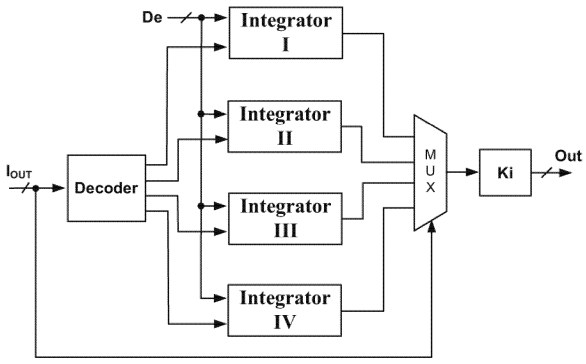


Figure 5. Simplified block diagram of load-scheduled integrator array.

the PID controller, multiple integrators are used, to span over the converter operating load range. Based on the load current level, a decoder is used to choose which integrator is enabled and its corresponding value goes to the output, while the other integrators are simply locked with their stored states. In this way, no integrator needs to slew over a wide range when the regulator transitions between DCM and CCM. Glitch free fast transient response is achieved.

III. CIRCUIT IMPLEMENTATION

A. High Resolution Multi-Phase Digital Pulse Width Modulator

A 4-phase, 13-bit resolution DPWM is designed by combining 3-bit dither modulation [2] and a 10-bit hardware DPWM. A hybrid approach [8] combining the counter-comparator and ring-oscillator-MUX scheme [4] is used to achieve sub-nanosecond resolution in the 10-bit hardware DPWM module. The rising edge of the PWM signal is set by a clock signal which is generated from the ring oscillator and the falling edge is generated by combining the comparator and MUX output. As illustrated in Fig. 6(a), the five LSB fine resolution obtained from ring-oscillator-MUX is shared among all the phases, the five MSB coarse resolution is generated through the counter-comparator approach. The ring oscillator runs at the frequency of $2^5 f_s$, where f_s is the switching frequency, and the 5-bit counter divides the switching period into 2^5 segments. In each segment, the ring oscillator generates 2^5 equally spaced square waves from the symmetrically oriented taps. Phase shift among the multiple phase outputs is implemented through a constant offset added to the counter. Good duty cycle matching among the phases is inherently guaranteed by this architecture, and is only limited by the clock skew which can be well managed by using automated layout tools.

Directly combining the multiplexer and comparator output through a flip-flop has a potential metastability problem when the delay difference between the counter-comparator and the multiplexer is large enough such that the set up time requirement of the flip-flop is violated. A synchronization scheme is incorporated here to combine the comparator and MUX outputs and avoid a potential race condition. The details of the synchronization circuit are described in [6]. A representative schematic and the corresponding switching waveforms are shown in Fig. 6(b) and Fig. 6(c). With this synchronization scheme, a subnanosecond resolution DPWM is achievable and the DPWM can be fully synthesized.

Fig. 7 shows the block diagram for generating the synchronous rectifier (SR) control signal with programmable

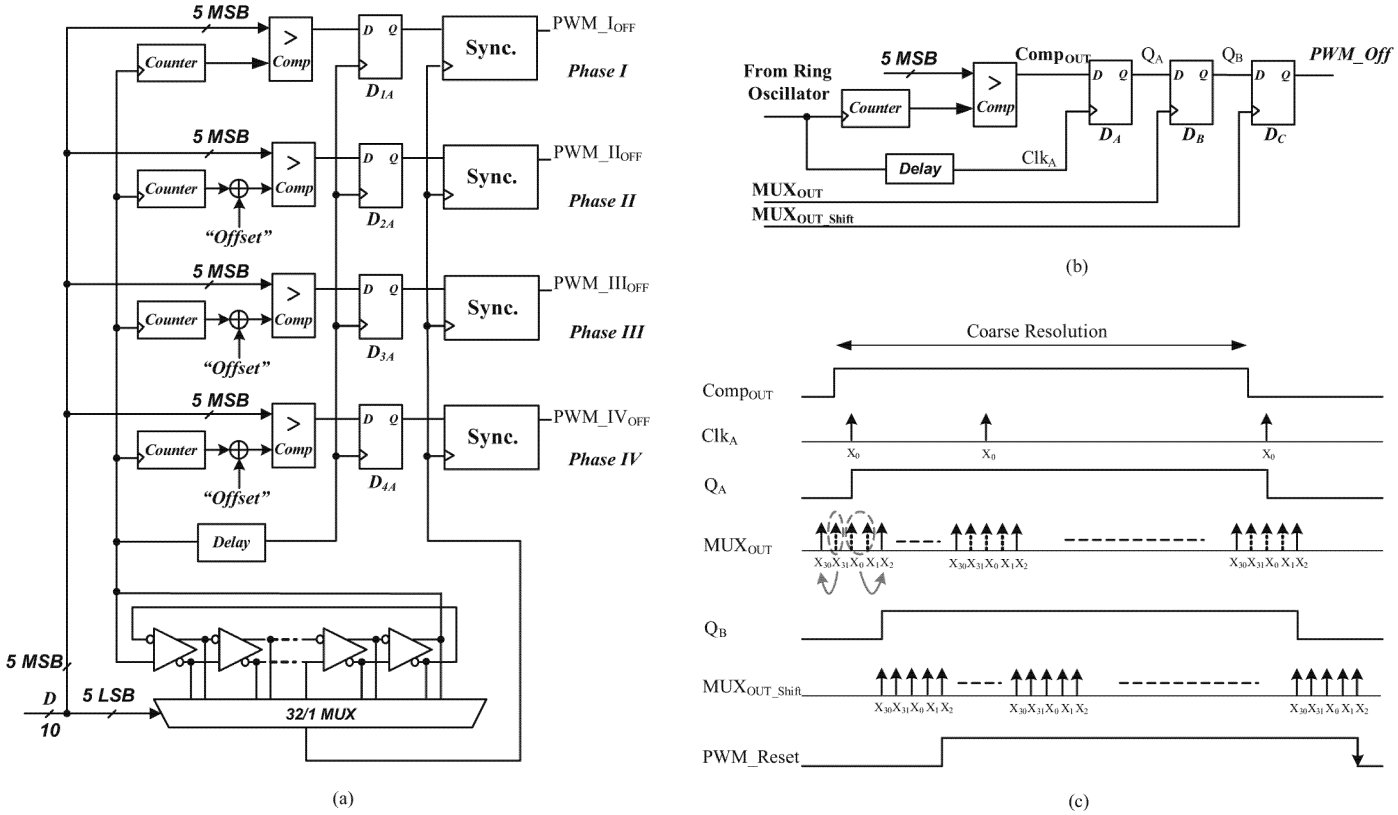
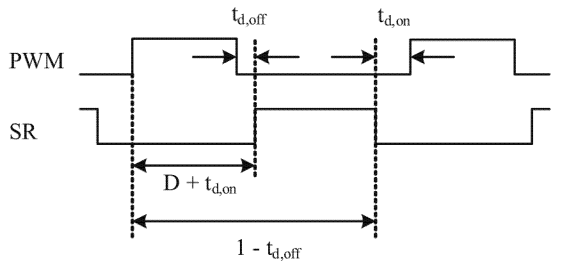


Figure 6. (a) Simplified block diagram of a multi-phase DPWM module (b) simplified schematic of the double flip-flop synchronization scheme (c) the switching waveforms of the double flip-flop synchronization circuit.

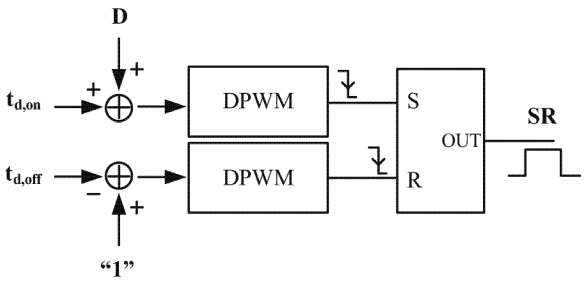
deadtime and its corresponding switching waveform. The synchronous rectifier has a complementary switching pattern with deadtime $t_{d,on}$ and $t_{d,off}$ relative to the rising and falling edges of the PWM signal. The same circuit used to generate PWM signal is used here to generate the rising edge and falling edge of the SR control signal respectively with duty cycle input D+ $t_{d,off}$ and 1- $t_{d,on}$ respectively. A falling edge triggered set-reset flip-flop is used to combine the two signals to generate the SR control signal. The deadtime $t_{d,on}$ and $t_{d,off}$ are stored in registers and can be programmed through the serial parallel interface.

B. Ring Oscillator Based ADC

A ring-oscillator-based analog-to-digital conversion scheme [4] is applied here. Fig. 8 shows the simplified block diagram of the ring-oscillator-based ADC. The error voltage V_e between converter output voltage V_{OUT} and reference voltage V_{REF} is amplified by the input stage and converted to a differential current that results in instantaneous differential frequency in the two ring oscillators. The digital error command D_e, based on the frequency difference of two ring oscillators, is generated by comparing the difference of the counter outputs. Instead of counting the frequency from one tap per ring oscillator, all M uniformly spaced taps on each respective ring oscillator are observed for frequency information, increasing the ADC resolution by M. An input stage similar to the design in [7] is applied in the developed ADC to achieve a large transconductance over a wide saturation range, enabling 4 mV LSB resolution with 4 MHz sampling frequency. The ADC in the feedback loop and the one in the feedforward control are identical to maintain simplicity in the design.



(a)



(b)

Figure 7. Synchronous rectifier control signal generation (a) switching waveform (b) simplified block diagram.

IV. Experimental Results

The complete multi-mode 4-phase digital-controlled VRM IC controller is implemented in a 0.18 μm CMOS process. The die photo is shown in Fig. 9. The active area of the chip is about 0.5 mm^2. A 4-phase, 80 A synchronous regulator board is built to test the performance of the designed IC controller. Table I summarizes the application and measured performance of the IC.

Fig. 10(a) shows the switching waveform of the converter while running at continuous conduction mode with 20A output current. V_{PWM} and V_{SR} are high side and low side n-channel MOSFET command voltage, respectively, generated by the IC controller and V_X is the corresponding switching node waveform. Fig. 10(b) and Fig. 10(c) show the switching waveforms corresponding to discontinuous conduction and pulse skipping mode, respectively, with output current at 4A and 0.5 A, respectively. The efficiency of the converter as a function of load current is plotted in Fig. 11. The peak efficiency is moderate (about 80%) due to the particular power train used. However, with DCM and pulse skipping mode operation, the efficiency improves as much as 40% in light load condition.

Fig. 12 compares the VR transient response, with and without load current feedforward, for 40A loading between 10A and 50A with the load slew rate of 400A/us. It can be seen from Fig. 12(a) that with both feedback and feedforward control, the output voltage follows well with the desired load line with less than 20mV overshoot voltage. With only the feedback control, however as shown in Fig. 12(b), the overshoot voltage reaches about 50mV, which reflects the

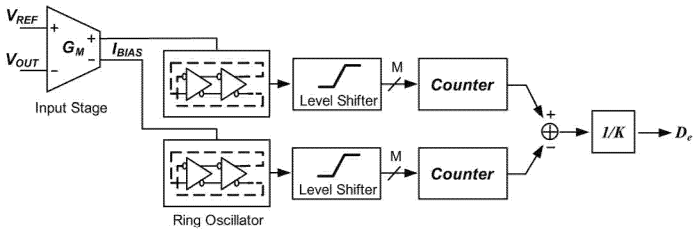


Figure 8. Block diagram of a ring oscillator based ADC

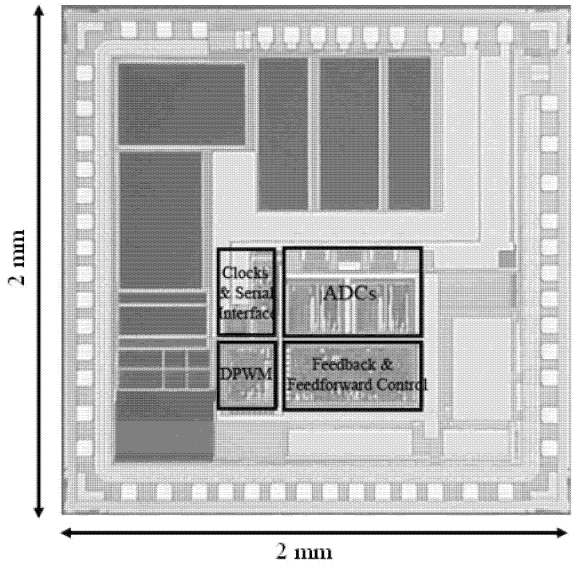


Figure 9. Chip micrograph

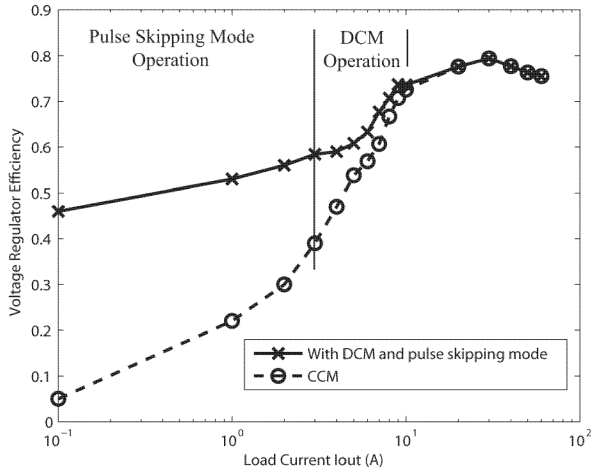
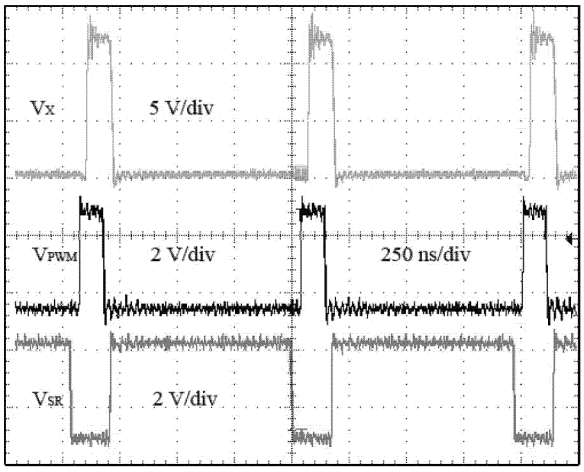


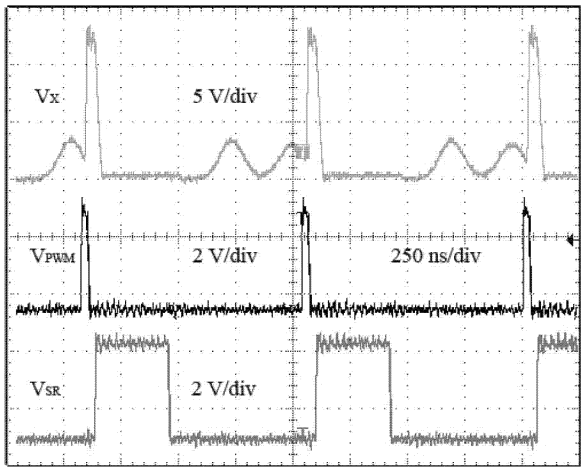
Figure 11. Measured converter efficiency as a function of load current with V_{in}=12V and V_{out}=1.3V.

bandwidth limitation of the feedback controller. A faster transient response has evidently been achieved with feedforward control.

Fig. 13 shows the VR transient response, with the VR operating between DCM and CCM with a single integrator, for 12A loading and unloading between 4A and 16A. A relative large output overshoot and long settling time is observed in the loading and unloading transient as the integrator has to slew over a wide range between DCM and CCM. As a comparison, Fig. 14 shows the VR transient response with the load-scheduled integrator array. Both the



(a)



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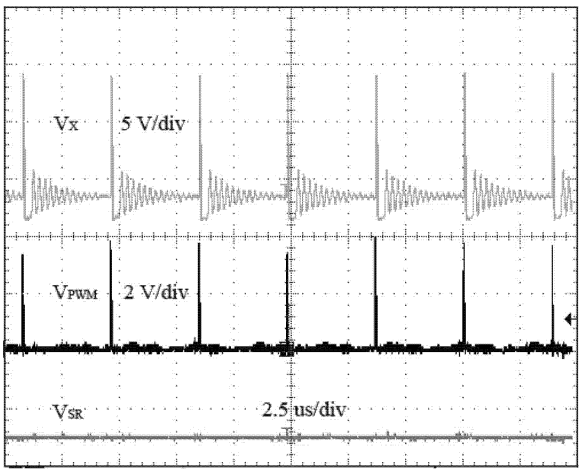
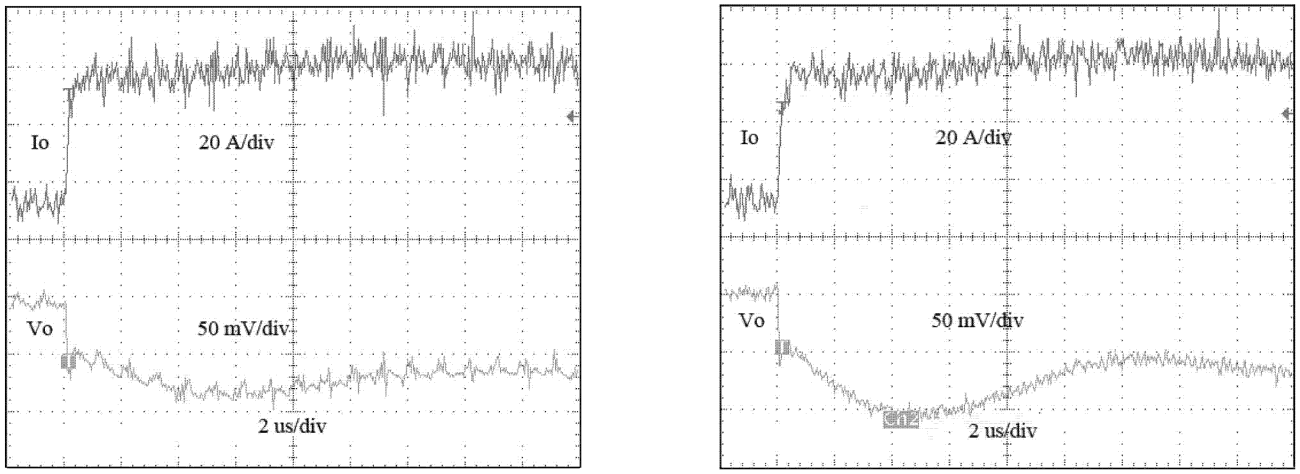


(c)

Figure 10. Measured switching waveforms when VRM runs in different operation mode (a) continuous conduction mode (b) discontinuous conduction mode (c) pulse skipping mode.

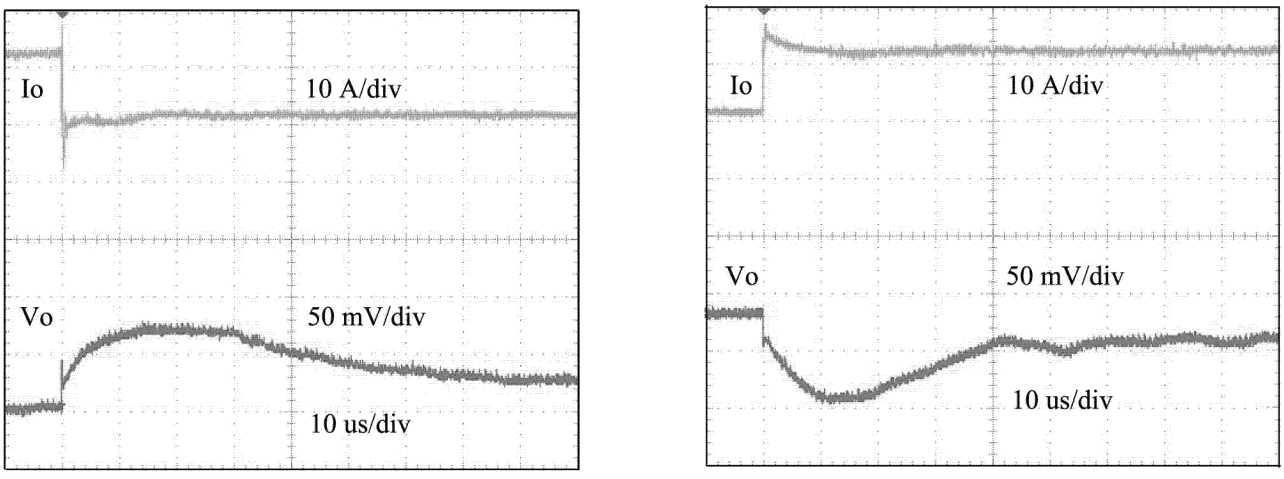


(a) (b)

Figure 12. Experimental 40A loading transient with 400A/μs slew rate (a) with load current feedforward and feedback control (b) with feedback control only.

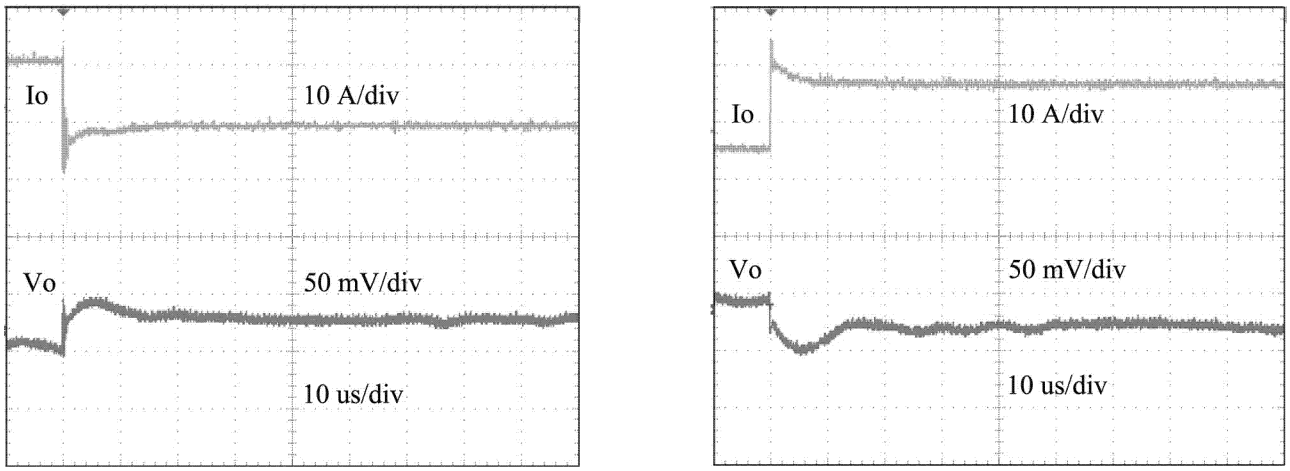
TABLE I
CHIP PERFORMANCE SUMMARY

Technology	0.18 μm CMOS
Number of phases	4
External LC filter	L_{phase}=300 nH, C_{total}=1000 μF
Input voltage	12 V
Output voltage range	0.8–1.8 V
Switching frequency	1 MHz
DPWM resolution	120 ps (13 bit resolution)
ADC sampling frequency	4 MHz
DC output voltage precision	± 0.2%
Power consumption	3.78 mW
Active chip area	0.5 mm^2



(a) (b)

Figure 13. Experimental 12A load transient response with single integrator (a) unloading transient with VR operating from CCM to DCM (b) loading transient with VR operating from DCM to CCM.



(a) (b)

Figure 14. Experimental 12A load transient response with load-scheduled integrator array (a) unloading transient with VR operating from CCM to DCM (b) loading transient with VR operating from DCM to CCM.

output overshoot voltage and settling time are substantially reduced.

V. CONCLUSION

This paper describes a digital multi-mode 4-phase IC controller for the voltage regulator application. The multi-mode operation improves the converter efficiency by at least a factor of ten in light load condition. Combined load current feedforward and load-scheduled digital PID control enable fast and glitch-free large-signal transient response. A high resolution digital pulse width modulator and 4mV quantization bin analog to digital converter is implemented in the IC controller to ensure tight DC regulation.

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