Architecture and IC Implementation of a Digital VRM Controller

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Abstract—**This paper develops the architecture of a digital PWM controller for application in multi-phase voltage regulation modules (VRM's) with passive current sharing. In this context, passive current sharing and VRM transient response are analyzed. A scheme for sensing a combination of the VRM output voltage and output current with a single low-resolution windowed analog-to-digital converter (ADC) is proposed. The architecture and IC implementation of a digital PWM (DPWM) generation module, using a ring-oscillator-MUX scheme, is discussed. Experimental results from a prototype VRM and a partial controller IC implementation are presented.**

I. Introduction

DIGITAL controllers are a strong candidate for use in voltage regulation modules (VRM's) due to their low quiescent power, immunity to analog component variations, ease of integration with other digital systems, ability to implement sophisticated control schemes, and potentially faster design process. In particular, the ability of digital controllers to accurately match multiple pulse-width modulation (PWM) signals, may allow for the use of passive current sharing schemes in multi-phase VRM's, thus reducing the units' cost and complexity. Further, the ease of interface between a digital controller and other digital hardware can be advantageous in microprocessor and communication systems. In addition, the low power dissipation of digital controllers makes them an attractive choice for portable applications.

In this paper we develop an architecture for a digital VRM controller and discuss aspects of its integrated circuit (IC) implementation. In Section II we start with a brief overview of the structure of a digitally controlled multi-phase VRM. In Section III we analyze passive current sharing, and derive estimates for the possible phase current mismatch due to power train parameter variations. In Section IV we discuss the VRM transient response, and introduce an implementation of optimal voltage positioning with a digital controller. We then propose a low resolution analog-to-digital converter (ADC) topology that can be used in the VRM. Results from a prototype VRM are presented. Section V addresses the architecture of digital PWM (DPWM) generation modules. We analyze the stability of a differential ring oscillator and discuss the IC implementation of a ring-oscillator-MUX DPWM scheme. Data from a test chip implementing this DPWM scheme is presented. Finally, in Section VI we overview the plan for a complete IC implementation of a digital VRM controller.

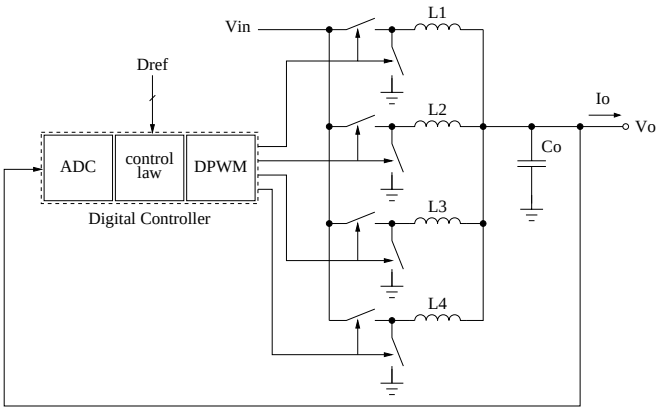

Fig. 1. Block diagram of a digitally controlled multi-phase VRM.

II. Overview of a digitally controlled multi-phase VRM

A block diagram of a digitally controlled 4-phase buck VRM is shown in Fig.1. A controller with similar structure has been discussed in [1]. The controller consists of an ADC which converts the regulated quantity (typically a combination of the output voltage V_o and the output current I_o), a discrete-time control law which calculates the duty cycle command from the output of the ADC and a digital reference word (typically a voltage identification code (VID) supplied by a microprocessor), and a DPWM module which generates the gating signals for the power train switches. The four phases are switched $360°/4 = 90°$ out of phase which reduces the output voltage ripple and the input current ripple, and can improve the transient response of the converter.

III. Passive Current Sharing in a Digitally Controlled Multi-phase VRM

In general, like analog controllers, digital controllers for multi-phase VRM's can be used successfully with active current sharing schemes, typically involving individual current sensing of each phase. However, unlike their analog counterparts, digital controllers have the advantage of almost perfect matching of the duty cycles of the PWM signals among the different phases, potentially allowing for the use of *passive current sharing* schemes, which eliminates the need for individual sensing and control of the phase currents. The use of passive current sharing may reduce the cost of the VRM, as a result of the smaller number of current sensors needed, as well as the

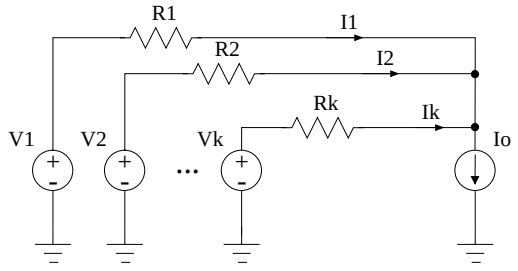

Fig. 2. DC current sharing model of a k-phase converter.

reduced pin count of the controller IC.

To study the DC current sharing among the different phases in a k-phase converter we model the latter with the circuit shown in Fig.2. Resistors R_1, R_2, ... , R_k model the DC resistance of each phase of the power train, and $V_1, V_2, \ldots, V_k$ model the average open-circuit voltage for each phase, i.e.

$$V_i = V_{in} D(i), \qquad i = 1, 2, \ldots, k \tag{1}$$

where $D(i)$ is the duty cycle command for phase i, and V_{in} is the input voltage.

With R_1, R_2, ... , R_k having arbitrary and possibly mismatched values, as a result of power train mismatches among the phases, the total power dissipation of the system is minimized when $V_1 = V_2 = \ldots = V_k$. To see this, consider the quantity

$$\hat{P} = \sum_{i=1}^{k} R_i I_i^2 + \lambda (I_o - \sum_{i=1}^{k} I_i), \tag{2}$$

which is the total DC power loss in the power train with the constraint that, the sum of the individual phase currents must equal the total load current, appended with Lagrange multiplier λ. A necessary condition for a minimum of the total power loss subject to the constraint is that all first order partial derivatives of $\hat{P}$ in equation (2) are zero. This yields

$$2R_i I_i - \lambda = 0 \tag{3}$$

for each index i corresponding to each phase of the converter. The constraint (3) implies that the DC voltage drops $R_i I_i$ for all phases are equal, which is equivalent to the power optimality condition $V_1 = V_2 = \cdots = V_k$ stated above.

The above result implies that when the duty cycles applied to different phases are identical, the power loss is minimized regardless of the possible resistive mismatch among the phases. A digital controller can produce acurately matched PWM waveforms for the different phases, with possible timing mismatch resulting only from parameter variations of the power FETs and gate drives, which is discussed in Section III-B.

A. Phase Current Mismatch Due to Power Train Resistance Mismatch

As it was argued above, if the multi-phase converter has matched duty cycles but mismatched power train resistances among the phases, the output current distributes itself among the phases so as to minimize the power dissipation in the power train. However, the actual current mismatch is still of interest since it may have undesirable consequences such as possible saturation of the inductors.

Assume matched duty cycles among the phases, $V_1 = V_2 = \ldots = V_k = V_{in} D$. Then, a power train resistance mismatch ΔR results in worst case current mismatch through a particular phase (let this be phase i) when all other phases have the same power train resistance equal to R, while that phase has mismatched resistance $R_i = R + \Delta R$. Since the power train resistances of the different phases form a current divider for the output current I_o, the current through phase i is

$$I_i = I_o \frac{R/(k-1)}{R_i + R/(k-1)}. \tag{4}$$

Then, the mismatch current flowing in phase i is the difference between current I_i and the nominal phase current I_o/k,

$$\Delta I_i = I_i - \frac{I_o}{k} = -I_i \frac{k-1}{k} \frac{\Delta R}{R}. \tag{5}$$

Hence, the worst case phase current variation due to a power train resistance mismatch ΔR, is

$$\left(\frac{\Delta I_i}{I_i} \right)_R = -\frac{k-1}{k} \frac{\Delta R}{R}. \tag{6}$$

Finally, the value of the effective power train resistance for each phase can be estimated from

$$R = D R_{DS(on),h} + (1-D) R_{DS(on),l} + R_L + R_{trace} \tag{7}$$

where D is the duty cycle; $R_{DS(on),h}$ and $R_{DS(on),l}$ are the on-resistances of the high- and low-side MOSFET switches, respectively; R_L is the inductor DC resistance; and R_{trace} is the resistance of the printed circuit board traces in the power train for each phase. The relative variations of these parameters can be obtained from the data sheet for a particular process, and (7) can be used in conjunction with (6) to estimate the total current mismatch due to power train resistance mismatch.

B. Phase Current Mismatch Due to Duty Cycle Mismatch

Consider again Fig.2 and let $R_1 = R_2 = \ldots = R_k = R$. However, assume that $V_1, V_2, \ldots, V_k$ are not equal as a result of duty cycle mismatch among the phases. A duty cycle mismatch ΔD results in worst case current mismatch through a particular phase (let this be phase i) when all other phases are switched with the same duty cycle D, while that phase is switched with a mismatched duty cycle $D + \Delta D$, *i.e*

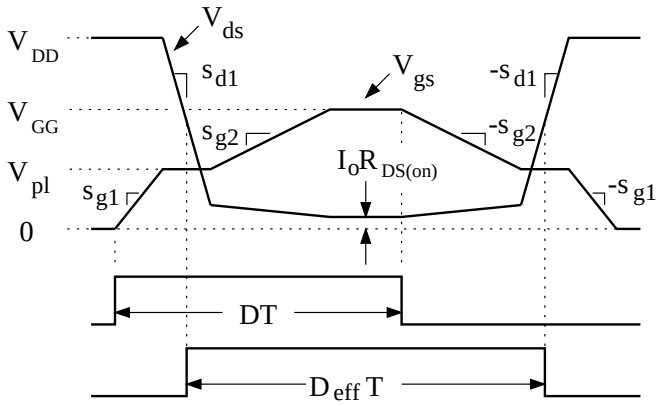

Fig. 3. Duty cycle variation due to the MOSFET switching characteristic.

$V_i = V_{in}(D + \Delta D)$. The mismatch current through phase i, $\Delta I_i = I_i - I_o/k$, is then

$$\Delta I_i = \frac{V_i - V_{in}D}{R + R/(k-1)} = \frac{k-1}{k}\frac{V_{in}}{R}\Delta D. \tag{8}$$

The power loss in the multi-phase part of the power train is $P_{loss,mp} = I_o^2 R/k$, and the converter input power is $P_{in} \approx DV_{in}I_o$. Then the efficiency of the multi-phase part of the converter power train is

$$\eta_{mp} = 1 - \frac{P_{loss,mp}}{P_{in}} \approx 1 - \frac{I_o^2 R/k}{DV_{in}I_o}. \tag{9}$$

Solving (9) for R and substituting in (8), we obtain an expression for the worst case phase current variation, $\Delta I_i/I_i$ due to a duty cycle mismatch ΔD,

$$\left(\frac{\Delta I_i}{I_i}\right)_D \approx \frac{k-1}{k}\frac{1}{1-\eta_{mp}}\frac{\Delta D}{D}. \tag{10}$$

One immediate observation from (10) is that the current mismatch sensitivity becomes worse if the efficiency of the converter improves, or if the duty cycle decreases.

Duty Cycle Mismatch due to MOSFET Switching Parameter Variations

A digital PWM controller can provide very accurate matching among the duty cycles for the different phases, thus the main source of duty cycle mismatch are the analog gate drives and power switches. Fig.3 shows a simplified model of the switching characteristic of a MOSFET which determines the relation between the duty cycle output by the controller (D) and the effective duty cycle seen at the switching node of the power train (D_{eff}). The gate drive of the MOSFET is modeled as a current source with output current $\pm I_G$ and maximum output voltage V_{GG}. Let C_{gs} and C_{gd} denote respectively the transistor gate-source and gate-drain capacitances, and let subscripts $_{sat}$ and $_{lin}$ refer respectively to the saturation and linear regions of operation of the MOSFET.

In the beginning of the switching period ($T = 1/f_{sw}$) the gate drive sources current I_G into the high-side MOSFET gate, making its gate-source voltage V_{gs} ramp up at a rate of $s_{g1} = I_G/(C_{gs} + C_{gd})_{sat}$. The drain-source voltage V_{ds} remains at the supply voltage V_{DD} until the drain current I_d reaches the value of the output current I_o. At this point, V_{gs} plateaus at a value

$$V_{pl} \approx V_{TH} + \sqrt{2I_o/k_m} \tag{11}$$

where k_m is the device gain factor and we assume that $I_o \gg I_G$. While $V_{gs} = V_{pl}$, V_{ds} moves down at a rate of $s_{d1} = -I_G/C_{gd(sat)}$ until the transistor goes into the linear region. Then V_{gs} continues to increase at a rate $s_{g2} = I_G/(C_{gs} + C_{gd})_{lin}$ until it reaches V_{GG}. In the linear region V_{ds} is about $I_o R_{DS(on)}$. The MOSFET turn-off is analogous.

From Fig.3 it can be seen that the effective duty cycle, measured between the midpoints in the swing of V_{ds}, is

$$D_{eff} \approx D + (V_{GG} - 2V_{pl})f_{sw}/s_g \tag{12}$$

where, for simplicity, we have set $s_g = s_{g1} = s_{g2}$. Then the variation of D_{eff} due to perturbations of V_{TH} and s_g is, respectively,

$$(\Delta D_{eff})_{V_{TH}} \approx -2f_{sw}/s_g \cdot \Delta V_{TH} \tag{13}$$

and

$$(\Delta D_{eff})_{s_g} \approx -(V_{GG} - 2V_{pl})f_{sw}/{s_g}^2 \cdot \Delta s_g. \tag{14}$$

Since typically $2V_{pl}$ is close to V_{GG}, (14) has small contribution to the overall D_{eff} variation relative to (13), and its effect may be neglected. Then, (13) can be used in conjunction with (10) to estimate the current variation among phases due to duty cycle mismatch.

C. A Passive Current Sharing Calculation Example

Given a certain specification on the maximum tolerable current mismatch among the phases of a multi-phase converter ($\Delta I_i/I_i$), the equations developed above can be used to estimate converter parameters such as the maximum allowable power MOSFET gate rise/fall time ($t_g = V_{GG}/s_g$), and total power train resistive mismatch among the phases ($\Delta R/R$). Equations (6), (10), and (13) were used to derive the constraints in Table I based on a sample converter design. Finally, it should be noted again that, while the possible 20% phase current mismatch due to duty cycle mismatch may result in non-optimal power dissipation, the 20% current mismatch due to resistive mismatch will not degrade the converter efficiency. In this example, it is seen that a modest gate drive rise/fall time of < 13ns leads to quite acceptable current-sharing behavior.

TABLE I

A PASSIVE CURRENT SHARING EXAMPLE

	Specifications	
$\Delta I_i/I_i$	phase current mismatch	40%
$(\Delta I_i/I_i)_R$	– due to resistive mismatch	20%
$(\Delta I_i/I_i)_D$	– due to duty cycle mismatch	20%
	Some Converter Parameters	
k	number of phases	4
f_{sw}	switching frequency	1 MHz
D	duty cycle	$1/5$
η_{mp}	multi-phase power train efficiency	90%
V_{GG}	gate drive voltage	5 V
ΔV_{TH}	threshold voltage variation	1 V
	Resulting Constraints	
s_g	power MOSFET gate rate	> 0.38 V/ns
t_g	power MOSFET gate rise/fall time	< 13 ns
$\Delta R/R$	power train resistive mismatch	$< 26\%$

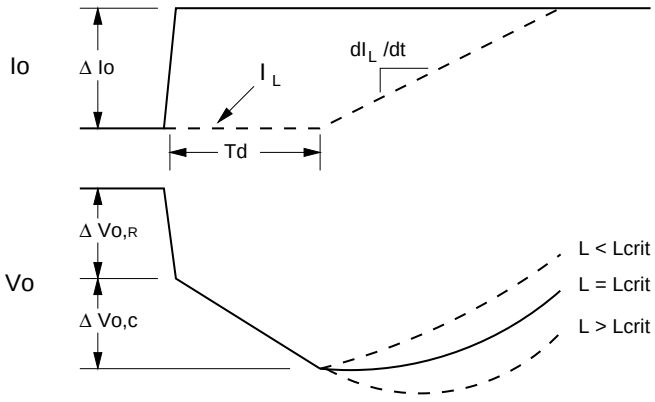

Fig. 4. Transient response of a buck VRM due to load current step.

IV. OUTPUT SENSING AND ANALOG-TO-DIGITAL CONVERSION

The precision with which a digital controller positions the output voltage V_o is determined by the resolution of the ADC. In particular, V_o can be regulated with a precision of one LSB of the ADC. Many applications, such as next-generation microprocessor VRM's, are expected to require regulation tolerances of less than 50mV [7], demanding ADC modules with very high resolution. For example, regulation resolution of 10mV at $V_{in} = 5$V corresponds to ADC resolution of $N_{adc} = \log_2(5V/10mV) = 9$ bits. Further, microprocessor VRM designs target switching frequencies in the megahertz range, implying ADC conversion times of less than a microsecond. The need for high resolution and fast conversion time may result in expensive and high-power ADC designs. Therefore, it is advantageous to look for low-resolution ADC topologies that meet the tight regulation specification.

A. VRM Transient Response

An output voltage transient of a buck VRM due to an increase in the load current, I_o, by ΔI_o is illustrated in Fig.4. The load current step will first cause output voltage drop of magnitude $\Delta V_{o,R} = \Delta I_o R_{ESR}$ due to the effective series resistance (R_{ESR}) of the output capacitor (here, for clarity, we are ignoring the initial V_o drop due to the series inductance of the output capacitor). Then, since the controller has non-zero response delay, V_o will continue to drop due to discharge of the output capacitor C_o. Let T_d be the delay of the controller response, *i.e.* the time between the instant a step in the load current has occurred and the resulting update of the duty cycle by the controller. Then the V_o drop due to the capacitive discharge will be $\Delta V_{o,C} = \Delta I_o T_d/C_o$. After time T_d, the controller responds to the load step by increasing the duty cycle, resulting in inductor current (I_L) increase at a rate of $dI_L/dt = \Delta V_L/L$, where, assuming saturated controller response, $\Delta V_L = V_{in} - V_o$ ($\Delta V_L = -V_o$ for an unloading transient). Consequently, V_o exhibits second-order behavior and eventually starts to increase. Reference [8] gives a condition ensuring that V_o starts increasing immediately after the I_L begins to ramp up,

$$\frac{dI_L}{dt} \geq \frac{\Delta I_o}{\tau_o} \tag{15}$$

where $\tau_o = R_{ESR}C_o$ is the technology-dependent time constant of the output capacitor. This implies a critical value of L,

$$L_{crit} = \frac{\tau_o \Delta V_L}{\Delta I_o}. \tag{16}$$

For $L \leq L_{crit}$, V_o starts to increase immediately after I_L begins to ramp up.

B. Implementation of Optimal Voltage Positioning

The concept of optimal voltage positioning has been widely used in recent voltage regulator designs. The idea is to always position V_o at $V_{ref} - R_{ESR}I_o$, where V_{ref} is the reference voltage, instead of driving it to V_{ref} [8]. In that case, the converter behaves as a voltage source with value V_{ref} and output impedance that is always real and equal to R_{ESR}. If optimal voltage positioning is used, ideally C_o can be made half the size required for a stiff voltage regulator design, which can save on cost and circuit area and volume.

The optimal voltage positioning technique can be extended to include non-zero controller delays. From Fig.4 it can be seen that, assuming $L \leq L_{crit}$, the V_o excursion due a load current step ΔI_o is

$$\begin{aligned} \Delta V_o &= \Delta V_{o,R} + \Delta V_{o,C} \\ &= \Delta I_o R_{ESR} + \Delta I_o T_d/C_o \\ &= \Delta I_o R_{ESR}\left(1 + T_d/\tau_o\right). \end{aligned} \tag{17}$$

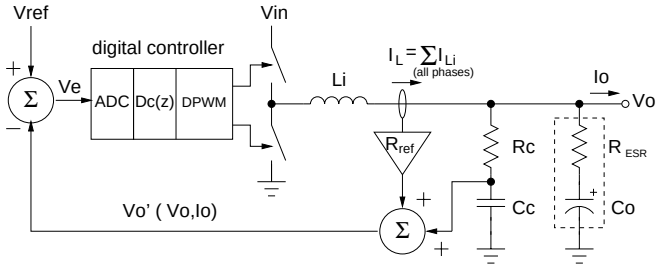

Fig. 5. Implementation of optimal voltage positioning with a digital controller.

Equation 17 shows that the output voltage step is directly proportional to the output current step, with proportionality constant which is a linear combination of the output capacitor ESR and the delay of the controller. Thus, using the reasoning behind the optimal voltage positioning technique, we can design the controller to always position V_o at

$$V_o \rightarrow V_{ref} - R_{ref} I_o \tag{18}$$

where

$$R_{ref} = R_{ESR}\left(1 + \frac{T_d}{\tau_o}\right). \tag{19}$$

This extension is particularly important for capacitor technologies with small τ_o such as ceramic capacitors, where the term corresponding to controller delay may dominate.

A scheme for implementing optimal voltage positioning with a digital controller is shown in Fig.5. The sensed quantities are the total inductor current through all phases, $I_L = \sum_{i=1}^{4} I_{Li}$, and the output of an estimator consisting of resistor R_c and capacitor C_c, which gives information about V_o and the current flowing through C_o during transients. The total inductor current I_L is amplified by a transresistance gain of R_{ref} and is then added to the output of the estimator $R_c - C_c$. Thus the resulting quantity

$$V_o'(V_o, I_o) = V_o \frac{1}{1 + s\tau_c} + R_{ref} I_L \tag{20}$$

where $\tau_c = R_c C_c$ is the time constant of the estimator, contains information about both the output voltage and output current. The quantity V_o' is then subtracted from V_{ref} to form the error signal V_e which is quantized by the ADC and fed into a digital PID control law $D_c(z)$. The control law represented in the discrete-time domain has the form

$$\begin{aligned} D_c(n+1) = K_p D_e(n) + K_d[D_e(n) - D_e(n-1)] + \\ + K_i D_i(n) + D_{ref}(n) \end{aligned} \tag{21}$$

where $D_c(n)$ is the duty cycle command at discrete time n, $D_e(n)$ is the error signal

$$D_e(n) = D_{ref}(n) - D_o'(n), \tag{22}$$

and $D_i(n)$ is the state of an integrator

$$D_i(n+1) = D_i(n) + D_e(n). \tag{23}$$

Further, K_p is the proportional gain, K_d is the derivative gain, and K_i is the integral gain. All variables are normalized to the input voltage, V_{in}. Quantities $D_o'(n)$ and $D_{ref}(n)$ are the digital representations of V_o' and V_{ref}, respectively. Variable $D_{ref}(n)$ is used as a feedforward term in (21).

From (20) it can be seen that in steady state for $K_i > 0$ the controller will position V_o according to (18). To ensure that during transients the output impedance of the converter (Z_o) is approximately R_{ref} as well, the numerator and denominator of the impedance function $Z_o(s) = -V_o/I_o$ are matched to first order yielding

$$\tau_c = \tau_o \frac{1 + K_p R_{ref}/R_{ESR} - L/R_{ref}\tau_o}{K_p - 1} \tag{24}$$

where $L = L_i/N_\phi$ and N_ϕ is the number of phases. Notice that for large values of K_p the estimator time constant asymptotically approaches the output capacitor time constant ($\tau_c \rightarrow \tau_o$).

Finally, observe that the sensing approach introduced above uses only one ADC to obtain information about both V_o and I_o.

C. Experimental Results

A prototype digitally controlled VRM using a 4-phase buck topology with passive current sharing was simulated and built with the parameters shown in Table II. The simulation was done in MATLAB, while the actual controller was implemented using a DSP board connected to a PC, and an FPGA to produce the overall timing and the multi-phase DPWM signals. The controller has 9 bits of effective ADC resolution, and effective 10 bits of DPWM resolution (7 bits of hardware resolution plus 3 bits of digital dither [10]). Optimal voltage positioning was implemented using the scheme discussed in Section IV-B. Figures 6(a)[1] and (b) show, respectively, the simulated and experimental response of the converter to a load current change from 1A to 11A and back to 1A ($\Delta I_o = 10$A).

D. ADC Topology

Next generation microprocessors are expected to have current slew rates of more than $350\text{A}/\mu\text{s}$ [7] demanding VRM's with extremely fast responses. Further, topologies with low ADC latency are desirable in the cases when the ADC is inside a feedback loop, since delays in the ADC correspond to phase shift that may degrade the loop response. Consequently the ADC's used in digital VRM controllers should have very low latency. While multi-stage ADC topologies may have high throughput (high sampling rate), they have larger latency due

[1] In this simulation the data is sampled at the switching frequency, therefore the switching ripple on V_o and V_o' cannot be seen. For this discussion the switching ripple is not of interest and its omission makes the plots clearer.

TABLE II

PROTOTYPE VRM PARAMETERS

V_{ref}	reference voltage	1.5 V
V_{in}	input voltage	5 V
k	number of phases	4
f_{sw}	switching frequency	250 kHz
T_d	controller delay	5 μs
N_{adc}	effective ADC resolution	9 bit
N_{dpwm}	effective DPWM resolution	7 bit (hardware) + 3 bit (dither)
L_i	phase inductors	4.4 μH
C_o	output capacitance	4 mF (tantalum)
R_{ESR}	output capacitor ESR	4 $m\Omega$
R_{ref}	closed-loop output impedance	$5m\Omega$

to either multiple comparisons (pipeline ADC's), or digital filtering ($\Sigma\Delta$ ADC's). Thus a single stage (flash) topology is preferable in applications such as VRM's where the speed of response is of paramount importance. From Fig.6 it can be seen that the controlled quantity V_o' does not have large excursions beyond V_{ref}. Thus, using a high resolution flash ADC that covers the full range between ground and V_{in} will demand excessive power and silicon area. Rather, an ADC topology can be conceived of, which has high resolution only in a small window around V_{ref}.

A block-diagram of such a "windowed" ADC is presented in Fig.7. A Digital-to-Analog Converter (DAC) converts the digital reference word D_{ref} to an analog voltage V_{ref}. Note that this DAC can be slow compared to the response time of the regulator, since D_{ref} does not change very fast, if at all. Then, a number of comparators are connected to V_{ref} through an offset network with steps ΔV_{ref}, creating a few quantization bins around V_{ref}. The controlled quantity V_o' is fed in the other input of the comparators. Note that, since V_o' is compared against V_{ref}, the resulting digital signal (D_e) is the difference between the two, which is a digital representation of the error signal V_e. Hence, the windowed architecture implements both an ADC and an error amplifier.

For example, if the converter is designed for regulation tolerance of 50mV, V_o' will not exceed $\pm$50mV about V_{ref} under normal operation. In this case ADC resolution of $\Delta V_{ref} = 10$mV seems reasonable to provide good control of V_o within the tolerance window. Then only $2 \times 50\text{mV}/10\text{mV} = 10$ ADC bins are required to cover the range of V_o', which corresponds to ADC resolution between 3 and 4 bits. In fact, the ADC in the prototype VRM from Section IV-C used a windowed structure.

E. V_o Clamping

A modification of the above control scheme may result in a smaller number of comparators in the ADC and faster regulator response: The number of comparators is reduced to, say, four, and the two comparators at the extremes of the ADC quantization window are sampled at a frequency higher than the switching frequency. If V_o' exceeds the range of the quantization window during a large transient, these comparators turn *all* converter phases on or off (depending on the direction of the transient), in an attempt to clamp V_o. This approach can substantially speed up the response of the regulator without changing the converter steady-state switching frequency, resulting in smaller output capacitors. It comes at the cost of implementing two very fast comparators. A similar clamping approach has been successfully used in analog VRM controllers [9].

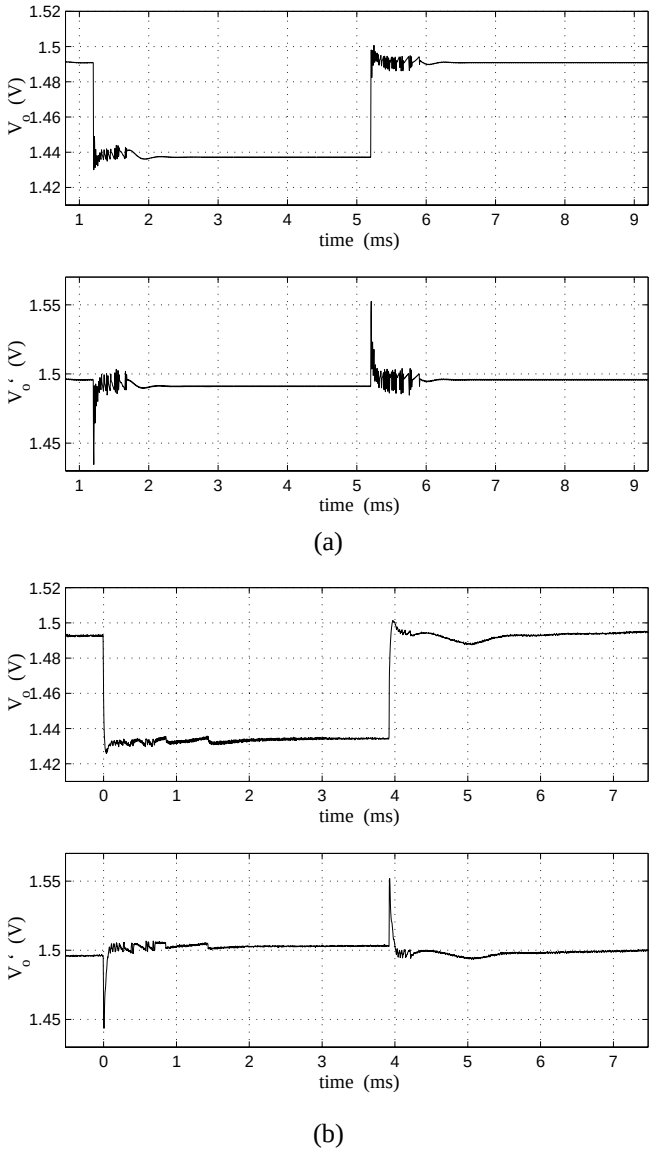

Fig. 6. Transient response of a prototype digitally controlled multi-phase buck converter with parameters from Table II, resulting from a 10A load current step: (a) simulation, and (b) experimental results. V_o is the output voltage, and V_o' is the quantity compared to V_{ref} to form the error signal.

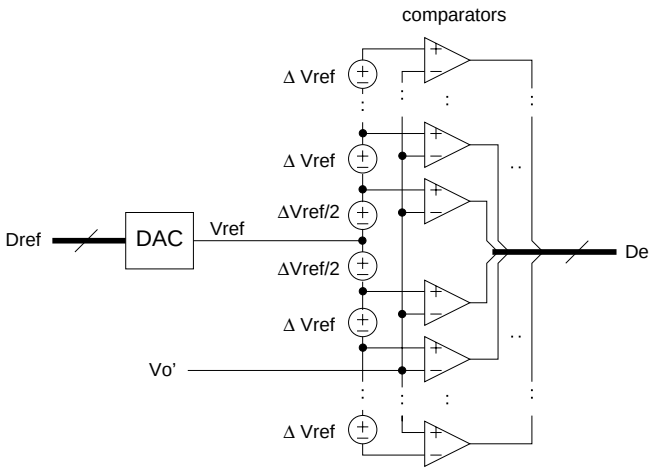

Fig. 7. Block diagram of a windowed ADC. It implements both an ADC and an error amplifier.

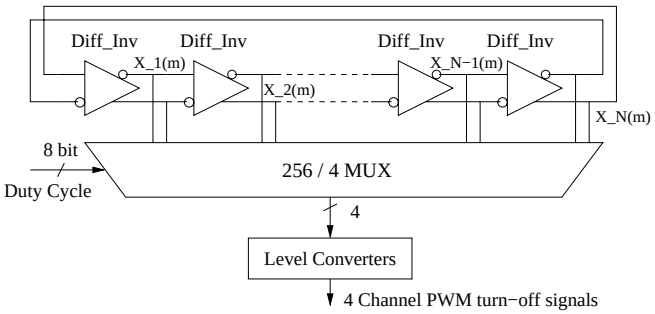

Fig. 8. PWM generation block diagram

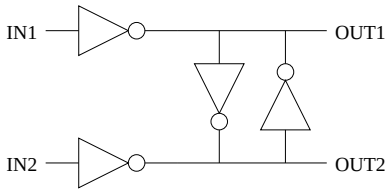

Fig. 9. Ring oscillator delay cell

V. Digital PWM Generation Circuits

A. Overview of Digital PWM Generation Schemes

One method to create PWM signals is with a fast-clocked counter-comparator scheme [2]. Such a design takes reasonable die area but the power consumption reported is on the order of mW's. The main reason is that in this scheme, a high frequency clock and other related fast logic circuits are needed to achieve a high control resolution based on a reasonable switching frequency. Even worse, in a multi-phase application, PWM generation circuitry cannot easily be shared among phases. Thus, an independent counter-comparator pair has to be implemented for each of the phases, leading to increased die area and power.

A tapped delay line scheme is proposed in [3]. Power is significantly reduced with respect to the fast-counter-comparator scheme since the fast clock is replaced by a delay line which runs at the switching frequency of the converter. One drawback of this design is that the delay line is not well suited for multi-phase application. In a multi-phase controller, precise delay matching among the phases places a stringent symmetry requirement on the delay line. Also, area is a limiting factor for this scheme since the size of the MUX grows exponentially with the number of resolution bits N.

A combined delay line-counter structure is reported in [4], aiming to make a compromise between area and power. However, the asymmetry of the delay line remains a problem for multi-phase applications.

B. Ring-Oscillator-MUX Scheme

A ring-oscillator-MUX implementation, as illustrated in Fig. 8, has area and power considerations similar to those of the delay line approach. However, this scheme has the advantage of a symmetric structure.

The main components of the ring-MUX scheme are a 128-stage differential ring oscillator, which yields 256 symmetrically oriented taps, and a 256-to-4 MUX that can select appropriate signals from the ring. The MUX allows control of PWM timing for each of four phases, as would be used in a four-phase VRM.

A square wave propagates along the ring. When the rising edge reaches tap zero in the ring, the rising edge of the PWM signal for phase one is generated. The falling edge of this PWM signal is generated when the rising edge of the propagating square wave reaches a specified tap in the ring. The MUX is used to specify the tap for phase one, in accord with the commanded duty cycle. The PWM signals for each of phases two through four are generated in an analogous manner, but using taps on the ring offset by 64 positions for each subsequent phase.

A fully differential inverter is used as the basic cell of the ring oscillator, as shown in Fig. 9, allowing a ring with an even number of stages to support a stable oscillation. This makes the ring oscillator scheme especially suited for multi-phase PWM generation since the different phases can be tapped out from symmetric positions on the ring.

The ring oscillator provides the clock for the digital controller. The frequency of the ring oscillator can be controlled by adjusting the supply current to the entire ring. The ring frequency obeys the relationship

$$f = \alpha \cdot I_{avg}/C_{load} \cdot V_{swing}, \tag{25}$$

where I_{avg} is the current supplied to the ring oscillator, V_{swing} is the voltage swing seen in the ring, and α is a constant. Thus, it is straightforward to control frequency by adjusting the oscillator current.

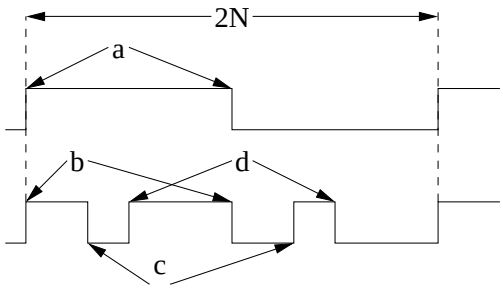

Fig. 10. Possible oscillation modes of the ring. The upper waveform is the fundamental sequence with the period of $2N$, where "a" denotes the only pair of edges. The lower waveform is a sequence of 3 pairs of edges with the same period, where "b", "c" and "d" denote the 3 pairs of edges.

C. Stability of Ring Oscillator

The desired oscillation mode of a ring oscillator is a quasi-square wave at the fundamental frequency which can be derived as in [5]. However, in principle, a ring oscillator can support more than one frequency mode, depending upon initial condition. In this section, we characterize the possible modes of oscillation of the designed ring oscillator, and discuss stability of these modes.

We begin by assuming that each stage has a unit delay, and by building a model by examining taps from alternating polarity along the differential ring structure, as shown in Fig.8. The N-stage differential ring oscillator of Fig.8 can be approximately modeled by the following difference equation:

$$\mathbf{X}(\mathbf{m}+\mathbf{1}) = \begin{bmatrix} 0 & \dots & \dots & 0 & -1 \\ 1 & 0 & \dots & \dots & 0 \\ 0 & 1 & 0 & \dots & 0 \\ \dots & \dots & \dots & \dots & \dots \\ 0 & \dots & 0 & 1 & 0 \end{bmatrix} \cdot \mathbf{X}(\mathbf{m}) \qquad (26)$$

where $\mathbf{X}(\mathbf{m})$ is the state vector of alternating single-sided states of the N-stage differential ring. To have physical meaning, each of the components in $\mathbf{X}(\mathbf{m})$ takes a value of either 1 or -1, standing for high or low voltage level. The sample time corresponds to one cell delay. The N eigenvalues of the matrix in (26) above are uniformly distributed on the unit circle, with values given by

$$\lambda_l = e^{j\pi/N} e^{jl2\pi/N} \qquad (27)$$

for $l = 1, 2, \dots, N$. It turns out that the matrix in (26), denoted A, satisfies

$$A^{2N} = I. \qquad (28)$$

Thus, it can be seen that the primary fundamental periodic sequence has period $2N$, and all other periodic sequences have period $2N$, whether fundamental or not. When an output sequence of the fundamental length $2N$ is examined, obtained by sampling at any tap of the ring structure, one finds that it exhibits n pairs of symmetric transitions, where n is an odd integer. By a transition, we refer to an edge between a $+1$ value and a -1 value. By a pair of symmetric transitions, we mean opposite transitions occuring at times separated by N unit delay periods. The transitions occur in symmetric pairs due to the differential structure of the ring. The waveforms of the fundamental sequence and a non-fundamental sequence are shown in Fig.10. In summary, all possible output sequences are periodic with period $2N$, and are characterized by an odd number of symmetric pairs of transitions. In fact, each pair of transitions corresponds to one differential edge propagating in the differential ring.

The above analysis is actually overly constrained in requiring that one differential edge be precisely delayed with respect to another differential edge by an integral number of unit delays. In fact, the ring is a continuous time dynamical system, and thus permits differential edges to propagate with arbitrary mutual delay times. In the underlying continuous time system, each differential edge existing in the ring structure propagates independently, and is subject to accumulating independent phase noise. One source of independent phase noise is thermal noise. The process of accumulating phase noise is actually a Brownian motion process, which results in asymptotically unbounded phase variance. As discussed in [6], the growth of the phase variance of a given edge in a ring oscillator is specified by

$$\sigma^2_{\Delta T} = K^2 \cdot T, \qquad (29)$$

where T is the elapsed time and K is a proportionality constant determined by circuit parameters. The calculation of K is illustrated in [6].

If the initial state of the ring structure is such that there is more than one differential edge propagating, pairs of differential edges eventually collide due to the unbounded and independent growth of their respective phase variances. When a pair of edges collide, they mutually annihilate one another. Thus, with any initial condition corresponding to an odd number of edges, the dynamics are such that the system evolves until a single edge remains. This rough argument illustrates the stability of the fundamental mode.

D. Experimental Results

A test chip to generate an 8-bit resolution PWM signal has been fabricated on a 0.25μm CMOS process, the die photo of which is shown in Fig.11. Instead of using a flat MUX, a binary-tree MUX is used because of its smaller transistor count and smaller area. The oscillator runs in current-starved mode and the voltage swing is reduced to the range of 0.4V to 1V depending on the frequency. The target DC-DC buck converter switches at a frequency range of 100kHz to 5MHz. The corresponding current drawn by the entire chip comprising the ring oscillator and one MUX is 80μA at 5MHz and less than 1μA at 100KHz. The waveforms of the complementary outputs of

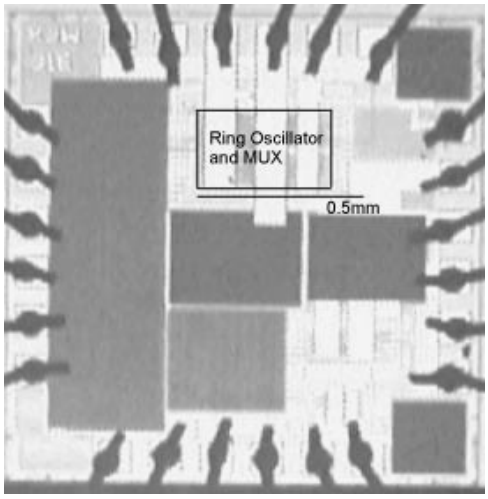

Fig. 11. Die photo of ring-oscillator-MUX test chip in 0.25μm CMOS process

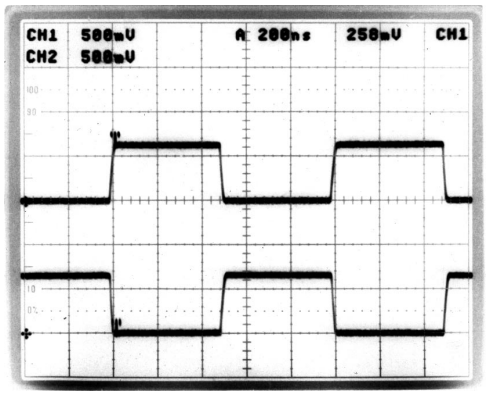

Fig. 12. Differential output of one ring oscillator delay stage. The upper waveform is taken from one tap on one stage of the ring, and the lower waveform is taken from the symmetric tap from the same stage. The vertical scale is 500mV/div, and horizontal scale is 200ns/div.

one of the stages are shown in Fig.12. Fig.13 shows the LSB resolution of 4ns for 1MHz operation. Level converters convert the reduced voltage swing back to rail to rail, and each level converter takes 2μA at 1MHz. In the test chip, only the fundamental oscillation mode has ever been observed.

VI. Digital Controller IC Architecture

A summarizing block diagram of a digital controller IC for a 4-phase VRM and the associated timing diagram are shown in Fig.14. The windowed ADC samples V_o' at the switching frequency, producing the error signal D_e. The Duty Cycle Calculation block implements a PID control law (21) using two's complement arithmetic to calculate the duty cycle command D_c based on D_e. CAD tools such as SPW, Synopsys, Apollo, Hercules and Cadence were used in designing this digital block. In the timing diagram, $T_{d,ADC}$ is the total delay of the windowed ADC, and $T_{d,Dc}$ is the latency of the Duty Cycle Calculation block. Subsequently, two MUX's are used in

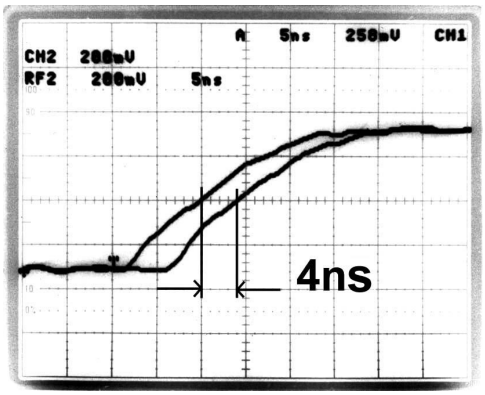

Fig. 13. 8-Bit resolution is achieved between two adjacent outputs of a ring oscillator delay cell. At 1MHz oscillation frequency, the resolution is 4ns.

an interleaved manner, in conjunction with a differential ring oscillator, to generate the PWM signals for the four phases. During every switching period, the new duty cycle command $D_c(n)$ is applied to one of the MUX's while the other one is holding the previous value $D_c(n-1)$ to ensure correct PWM signal generation for all phases. In general, two MUX's are sufficient for updating D_c in a multi-phase application.

Presently, a test IC, implementing the Duty Cycle Calculation module, is being fabricated.

VII. Conclusion

This paper developed the architecture of a digital PWM controller for application in multi-phase VRM's with passive current sharing. Passive current sharing was investigated, and estimates of the phase current mismatch due to power train parameter variations were derived. The VRM transient response was analyzed, and a scheme for sensing a combination of the VRM output voltage and output current with a single low-resolution windowed ADC was proposed. The architecture and IC implementation of a DPWM generation module, using a ring-oscillator-MUX scheme, was discussed. Experimental results from a prototype VRM and an IC implementation of the DPWM module were presented.

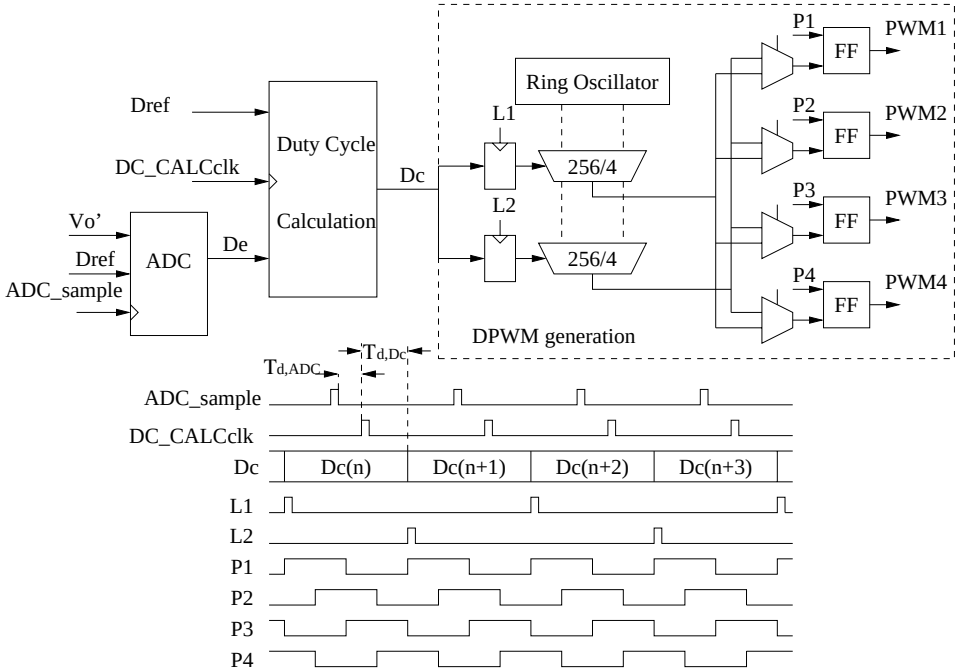

Fig. 14. Block diagram and timing of proposed digital controller IC

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