

# A 4- $\mu$ A Quiescent-Current Dual-Mode Digitally Controlled Buck Converter IC for Cellular Phone Applications

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**Abstract**—This paper describes a dual-mode digitally controlled buck converter IC for cellular phone applications. An architecture employing internal power management is introduced to ensure voltage compatibility between a single-cell lithium-ion battery voltage and a low-voltage integrated circuit technology. Special purpose analog and digital interface elements are developed. These include a ring-oscillator-based A/D converter (ring-ADC), which is nearly entirely synthesizable, is robust against switching noise, and has flexible resolution control, and a very low power ring-oscillator-multiplexer-based digital pulse-width modulation (PWM) generation module (ring-MUX DPWM). The chip, which includes an output power stage rated for 400 mA, occupies an active area 2 mm<sup>2</sup> in 0.25- $\mu$ m CMOS. Very high efficiencies are achieved over a load range of 0.1–400 mA. Measured quiescent current in PFM mode is 4  $\mu$ A.

**Index Terms**—Analog–digital conversion, CMOS integrated circuits, dc–dc power conversion, digital–analog conversion, digital control, digital pulse-width modulation (DPWM), pulse frequency modulation, pulse-width-modulated power converters, pulse-width modulation (PWM), ring ADC, ring-MUX DPWM.

## I. INTRODUCTION

THIS paper presents an ultralow-quiescent-power dual-mode digitally controlled buck converter IC for cellular phone applications. While the cellular phone is in talk mode, the load on the buck converter is high and pulse-width modulation (PWM) is used to achieve high regulation quality as well as high efficiency. However, when the cellular phone is in standby mode, in which the load current is very low, PWM mode leads to low efficiency due to excessive switching, gate drive, and quiescent current losses. To extend the standby time a cellular phone can sustain with each full charge of the battery, pulse frequency modulation (PFM) mode is preferred for light load operation. The designed IC supports PWM mode for heavy loads and PFM mode for light loads. The system block diagram of the buck converter IC and the external filter is shown

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in Fig. 1. The pin MODE is used to switch between the two modes. The PFM-mode quiescent power is the fundamental limitation on light-load efficiency, and, in this study, an ultralow quiescent current of 4  $\mu$ A is achieved in PFM mode. Details of the dual-mode design are presented in Section II.

For a digital implementation, small feature size processes with low supply voltages are preferred for implementing the digital circuits to achieve small die area, high speed, and low power consumption. In cellular phone applications, the power supply of the buck converter system is usually a single-cell lithium-ion battery, with voltage range of 2.8–5.5 V. Thus, the input voltage of the converter may be higher than the allowed supply voltage of the process (e.g., a maximum 2.75 V for a 0.25- $\mu$ m CMOS process). A solution that allows a low-voltage process to be used for the digital controller with high input voltage can be of great interest considering the possible cost reduction from integrating the switching regulator on the same die with the power train devices. Internal power management is introduced to resolve the conflict of high input voltage and a low-voltage process, the details of which are also presented in Section II.

The analog-to-digital converter (ADC) and the digital pulse-width modulator (DPWM) are used to provide the interface between the digital compensation network and the analog power train. A general purpose ADC can be unnecessarily expensive in terms of both power consumption and chip area; therefore, a ring-oscillator-based averaging ADC (ring-ADC) is developed which has reduced the quantization range. The details of the ADC are presented in Section III. The DPWM runs in both PWM and PFM modes, and thus low power is a primary design objective for this block. A very low-power DPWM scheme based on a ring-oscillator-multiplexer structure (ring-MUX DPWM) is developed, the details of which are presented in Section IV.

A prototype IC takes an active area of 2 mm<sup>2</sup> in a 0.25- $\mu$ m CMOS process. With a cascode power train and internal power management, the IC demonstrates safe operation of a standard CMOS process rated for 2.75 V with a 5.5-V supply. The power train on the chip is rated for a 400-mA load current, and efficiency above 90% is achieved for a load range of approximately 50–300 mA under PWM operation. Efficiency above 70% is achieved over the load range of 0.1–400 mA in PFM mode. The latter result is enabled by a 4- $\mu$ A quiescent current in PFM mode. Further experimental results are detailed in Section V.

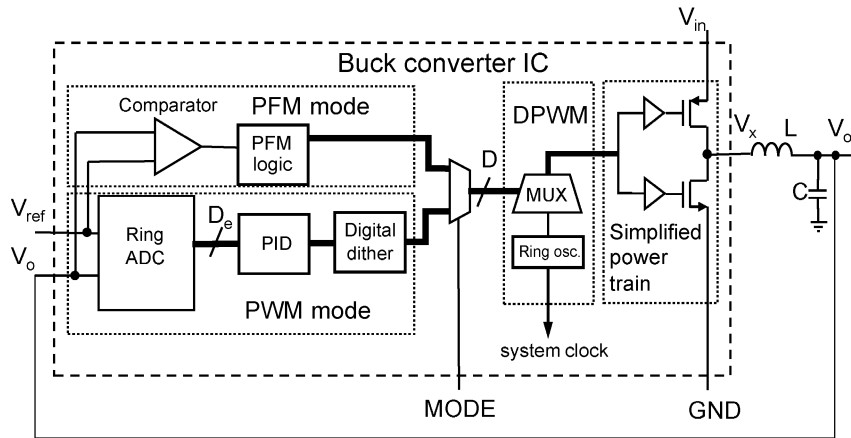


Fig. 1. Block diagram of dual-mode buck converter IC and external LC filter.

## II. ARCHITECTURE AND VOLTAGE COMPATIBILITY

### A. PWM Mode

The PWM mode runs the converter in continuous conduction. As shown in Fig. 1, in PWM mode, the error voltage  $V_e = V_o - V_{ref}$  is quantized by the ADC to provide an error signal in the digital domain  $D_e$ , and the digital PID compensation network [1] generates a duty ratio command  $D$ . The DPWM converts the duty ratio command into a PWM signal that controls the high-side and the low-side switches.

Subharmonic limit cycles may occur in a digitally controlled dc–dc converter because of the presence of two quantization operations, one in the ADC and one in the DPWM. Sufficient conditions to avoid subharmonic limit cycles are given in [2]. One step to avoid subharmonic limit cycles is to use a modulator (DPWM) that has a higher resolution (smaller quantization bin size) than that of the ADC. To meet this limit-cycle-avoidance condition, as well as the dc voltage-precision specifications, the ADC quantization step size is designed to be 16 mV, and the DPWM step size is designed to be 5.4 mV. We note that this is one convenient design choice but that substantially smaller step sizes can be readily implemented with the technology at hand.

A digital dither method that effectively reduces the DPWM hardware requirement while keeping the same output resolution is employed [2]. With this method, 10-b output resolution is achieved with a 5-b hardware DPWM and a 5-b digital dither modulation process. The DPWM is implemented with a very low-power ring-MUX reported in [3]. The ring oscillator in the DPWM runs at the switching frequency  $f_s$  and provides clock signals for the whole system. Thus, high modulation resolution is obtained without any high-frequency clock. The digital dither modulation provides very fine-scale resolution of an additional 5 b by modulating the hardware LSB over a 32-clock cycle period [2].

The output voltage ripple is a sum of switching ripple and dither ripple and is independent of the resolution of the quantizer. The switching ripple is a function of the cut-off frequency of the external filter and the PWM switching frequency [4]. The ripple caused by the dither process is a function of the cut-off frequency of the external filter and the dither frequency [2].

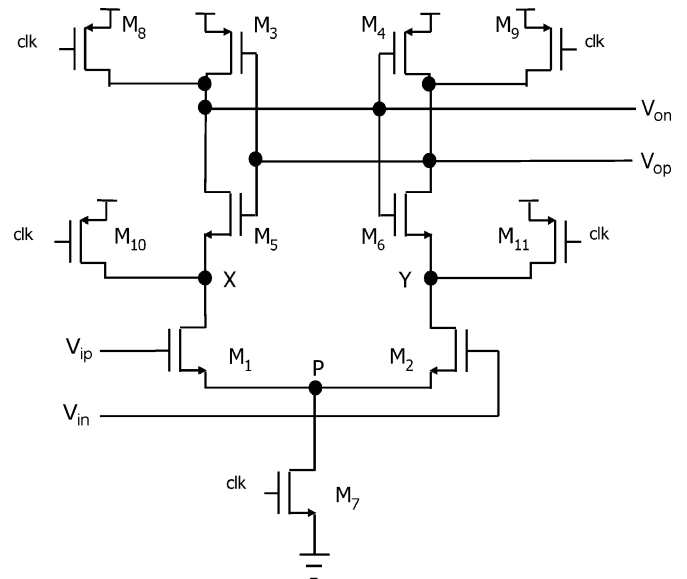


Fig. 2. Zero-bias-current comparator.

### B. PFM Mode

The PFM mode runs the converter in discontinuous conduction mode with fixed sampling frequency, fixed ON-time, and variable OFF-time. Referring again to Fig. 1, a comparator samples the output voltage  $V_o$  at a fixed frequency  $f_{s\text{amp,PFM}}$  and compares it to the reference  $V_{ref}$ . When  $V_o < V_{ref}$ , the controller generates a fixed-ON-time pulse through the DPWM to charge up the output capacitor. Otherwise, the converter and the controller are idling. The switching frequency in PFM mode scales roughly proportionally to the load current, thus the switching loss is greatly reduced in light load conditions. Thus, PFM mode enables high efficiency with ultralight loads and is ideal to control the converter in standby mode.

The PFM mode quiescent power is the fundamental limitation on ultralight load efficiency. To reduce it, a clocked zero-dc-current comparator [5] is used, as shown in Fig. 2. When the clock signal  $clk$  is low, the comparator is in reset mode. Nodes  $V_{op}$ ,  $V_{on}$ ,  $X$ , and  $Y$  of the comparator are precharged to supply voltage by  $M_8 - M_{11}$ . When  $clk$  goes high, the comparator goes into evaluation and regeneration mode. Input pair  $M_1$  and

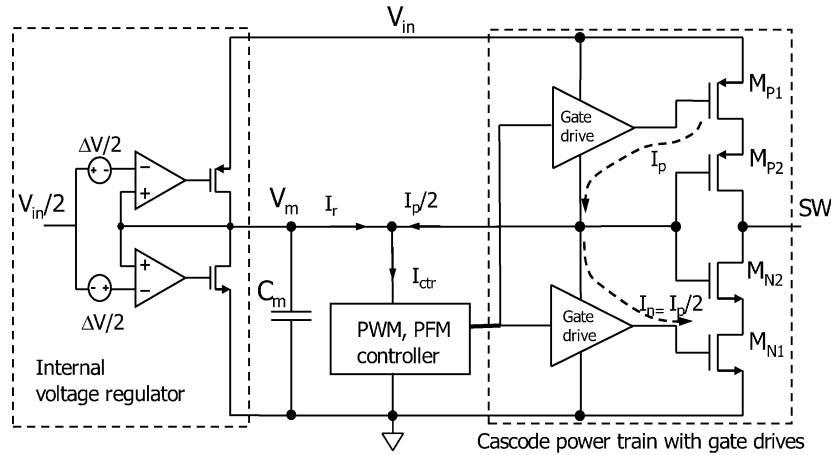


Fig. 3. Block diagram of internal power management.

$M_2$  resolves the input voltage, and the differential current develops a voltage difference between nodes  $X$  and  $Y$  before the cross-coupled latch turns on. Then, the latch transistors  $M_3 - M_6$  regenerate the amplified output signal back to full swing. After the output signals are fully regenerated, the cross-coupled inverter pair holds the logic levels without taking any power. Very low power is consumed by this comparator since only dynamic current flows through the input pair and the regeneration pair during the evaluation transient, and, once the output signals are fully established, there is no dc current flowing in the comparator. The transistors in the PFM comparator are sized to have less than 5-mV offset within  $3\sigma$  distribution [6].

### C. Voltage Compatibility and Internal Power Management

Small feature size processes with intrinsic low supply voltage are preferred to implement the digital circuit to achieve small die area, high speed, and low power. A 0.25- $\mu\text{m}$  CMOS process with the highest allowable supply of 2.75 V is used to implement the IC. As mentioned in Section I, the battery in cellular phones supplies a voltage range between 2.8-5.5 V. Thus, the circuit cannot run directly from the battery, and internal power management is introduced to ensure voltage compatibility.

The high-voltage interface components are the power train switches. As shown in Fig. 3, a cascode structure is used to protect both switches from seeing excessive gate-drain or gate-source voltage. The cascode transistors  $M_{P2}$  and  $M_{N2}$  are biased with an intermediate voltage  $V_m = V_{in}/2$ . Thus, the gate-drain and gate-source voltages of each transistor in the power train never exceed half of the input voltage.

The high-side gate driver works between supplies  $V_{in}$  and  $V_m$ , and the low-side gate driver works between  $V_m$  and ground. In each switching cycle, the average current  $I_p$  flowing into node  $V_m$  through the high-side gate driver is approximately twice the current  $I_n$  flowing out of  $V_m$  through the low-side gate driver, since the power train PMOS transistor has twice the width of the NMOS transistor in this design, to optimize conduction loss. The difference current  $I_p - I_n$  can be used as a partial or complete supply for the controller. The total current consumed by the controller and the gate drivers can be calculated by summing the equivalent dc current that flows into the ground node. If the internal power management scheme were not employed,

the resulting total current consumption would be  $I_p + I_n + I_{ctr}$ , where  $I_{ctr}$  is the equivalent dc current drawn by the controller. With the internal power management scheme, the overall current consumption reduces to the larger of  $I_p$  and  $I_n + I_{ctr}$ . The dc bias current in the class-B internal regulator is more than two orders of magnitude lower than  $I_{ctr}$  alone and is thus neglected. Therefore, a current savings that equals the smaller of  $I_p$  and  $I_n + I_{ctr}$  is achieved in PWM mode by using the internal power management scheme.

An internal push-pull class-B regulator is used to provide a stable midpoint voltage  $V_m$ . This voltage serves as a safe supply voltage for the digital controller circuits. A regulation window  $\Delta V$  of 50 mV is allowed on this regulator, and it is achieved by a built-in offset at the input stage of the linear regulator. The internal regulator only needs to handle the difference between  $I_p$  and  $I_n + I_{ctr}$ . The output stage is composed of a current source and a current sink, neither of which is conducting when  $V_m$  is within its regulation window. The bias current of the class-B regulator is 1  $\mu\text{A}$ .

### III. RING-OSCILLATOR ADC

In PWM mode, since  $V_o$  is regulated to be in the vicinity of  $V_{ref}$ , an ADC that can handle a rail-to-rail input is not necessary, and a windowed ADC that realizes high resolution with a reduced quantization range can be used [3], [7]. The main idea is to reduce the quantization window to the possible  $V_o$  variation range, which is usually tens of millivolts centered at  $V_{ref}$ . Due to switching activities of the power train, disturbances might be observed on  $V_o$ . Therefore, an averaging ADC that is insensitive to switching noise and has a windowed quantization range is desirable.

Synthesizable ADCs based on VCO or delay-line structures have been reported [8], [9]. In this study, we develop an averaging windowed ring-ADC which is nearly entirely synthesizable. Compared to the VCO or delay-line-based ADC, the resolution of the developed ring-ADC is invariant under reference voltage changes and can be flexibly adjusted to meet a wide range of applications.

The design of the ring-ADC is based on the observation that the oscillation frequency in a CMOS ring oscillator, biased in

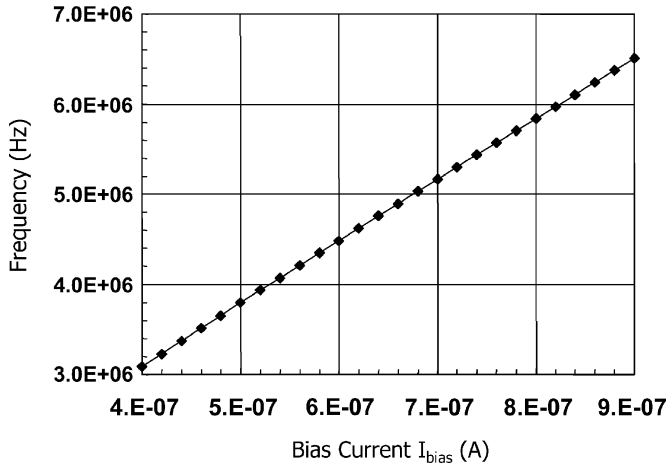


Fig. 4. Simulated frequency–current dependency of a four-stage differential ring oscillator biased in the subthreshold region.

the subthreshold region, has a linear dependency on the bias current, as illustrated in Fig. 4. The block diagram of the ring-ADC is shown in Fig. 5. The ADC consists of a simple analog block and a synthesizable digital block. A differential transistor pair  $M_1$ – $M_2$  drives two identical ring oscillators as a matched load. The bias current is such that the voltage swing on the ring oscillator is below threshold. Thus, each ring oscillator’s frequency is linearly dependent on its supply current. The error voltage  $V_e$  develops differential current in the two branches that results in instantaneous differential frequency at the two oscillators. The frequency of each oscillator is captured by a counter that is reset at the beginning of each sampling cycle. At the end of the cycle, one counter output is subtracted from the other, and the result  $C_e$  is used to calculate digitized error voltage  $D_e$ . Since there is uncertainty in the initial and ending phase, instead of looking at one output per ring, all of the  $M$  taps on each ring oscillator are observed for frequency information. It can be shown that, ignoring quantization error and assuming good linearity in the input differential pair,  $C_e$  is given by

$$C_e = Mk_1g_mT_{ADC}V_e \quad (1)$$

where  $M$  is the number of taps on each ring,  $k_1$  is the constant characterizing the ring oscillator frequency sensitivity to bias current,  $g_m$  is the transconductance of the input differential pair, and  $T_{ADC}$  is the ADC sampling period, which equals the switching period  $T_s$  of the converter. Finally, digitized error voltage  $D_e$  is calculated by scaling  $C_e$ . Since the saturation behavior of the input differential pair is dependent on the ratio of the input signal and the overdrive voltage of the differential pair, good linearity of the input transistors can be obtained by designing the overdrive voltage a few times higher than the differential input voltage. Since  $V_e$  is usually less than 100 mV, the overdrive voltage needs to be only a few hundred millivolts.

In this design, a ring-ADC with 16-mV quantization bin size and a total quantization window of 80 mV takes a chip area of 0.15 mm<sup>2</sup>. At 500-kHz sampling frequency, the measured current consumption of this ADC is 37  $\mu$ A. The transistors of the ring-ADC are sized to have less than 3-mV offset within  $3\sigma$

distribution [6]. The digital block can be further simplified by using a decoder and a counter, instead of a number of counters, to monitor the signals on all of the taps in each ring, resulting in significantly smaller die area and much lower power consumption. Compared to ADCs based on a VCO or a delay line, this ring-ADC has invariant resolution under different reference voltage levels due to the common-mode rejection capability of the differential pair and thus is suitable for a wide range of applications. Furthermore, the resolution of the ring-ADC can be controlled through the bias current, which can be made either constant or adjusted for automatic gain control (AGC). For example, the bias current in the differential pair of the ring-ADC can be made a function inverse to the square of the input voltage. Thus, when the input voltage is reduced, the gain of the ADC increases and, hence, the controller gain is also raised proportionally, resulting in an invariant loop gain. In summary, the ring-ADC has low power and small area, and its resolution can be designed with high flexibility depending on application requirements. The quantization resolution of the ring-ADC can be scaled by changing the number of stages in the ring and varying the bias current of the differential pair.

#### IV. RING-MUX DPWM

One method to digitally create PWM signals is with a fast-clocked counter-comparator scheme [10]. Such a design takes reasonable die area but the power consumption reported is on the order of milliwatts because of the high clock frequency in the counters [11]. A tapped delay-line scheme is proposed in [12]. Power is significantly reduced with respect to the fast-counter-comparator scheme since the fast clock is replaced by a delay line which runs at the switching frequency of the converter. A combined delay-line-counter structure is reported in [8] and [13], aiming to make a compromise between area and power.

A ring-oscillator-MUX implementation of a DPWM module, with the block diagram shown in Fig. 6(a), has area and power considerations similar to those of the delay-line approach. The ring oscillator runs with subthreshold voltage swing, and thus the power consumption is much lower than the delay-line structure due to the reduced swing. Since the ring oscillator in the DPWM runs in the current starved mode, the frequency can be controlled by adjusting the supply current to the entire ring. Thus, the switching frequency of the converter can be locked to an external clock by controlling the DPWM ring current. The ring oscillator in the DPWM also generates the clock signals for the entire converter system, i.e., the sampling clock with frequency  $f_{\text{samp,PFM}}$  in PFM mode and ADC sampling clock as well as PID clock in PWM mode.

The main components of the ring-MUX scheme are an  $N$ -stage differential ring oscillator, which yields  $2N$  symmetrically oriented taps and a  $2N/1$  MUX that can select appropriate signals from the ring. The delay stage in the differential ring oscillators in the DPWM is shown in Fig. 6(b). A square wave propagates along the ring. When the rising edge reaches a fixed tap in the ring, the rising edge of the PWM signal is generated. The falling edge of this PWM signal is generated when the rising edge of the propagating square wave reaches a specified

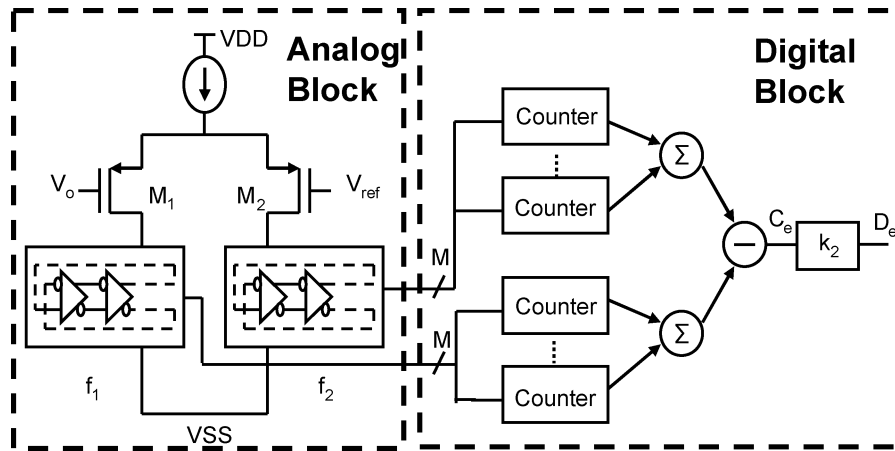
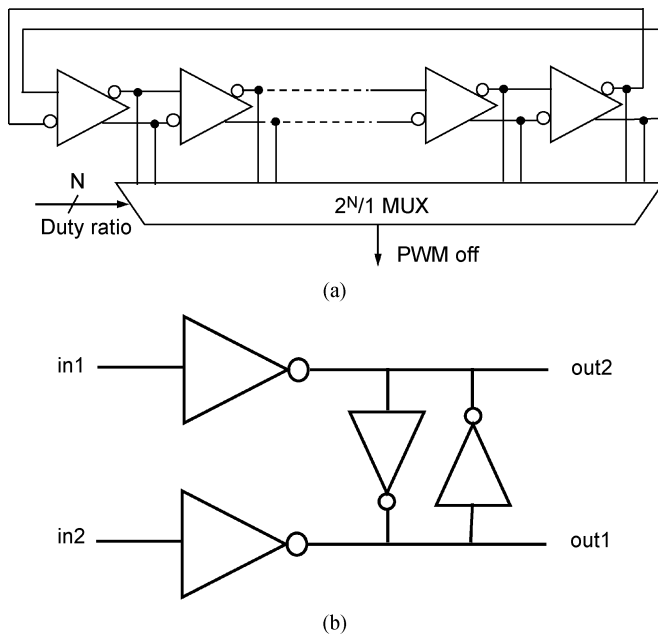


Fig. 5. Block diagram of a ring-ADC.

Fig. 6. (a) Block diagram of an  $N$ -bit ring-MUX DPWM. (b) Delay stage of the differential ring oscillator in the DPWM.

tap in the ring. The MUX is used to specify the tap in accord with the commanded duty cycle.

As mentioned in Section II, the output resolution is 10 b, the 5 MSBs of which are generated by the DPWM, and the 5 LSBs by the digital dither modulation process. The PWM signal generated by the hardware DPWM has a duty ratio range of 0%–100%, with a step size of 32 ns at 1-MHz PWM frequency.

## V. EXPERIMENTAL RESULTS

The complete dual-mode digitally controlled buck converter IC is implemented in a 0.25- $\mu\text{m}$  CMOS process. The die photograph of the chip is shown in Fig. 7. The total chip area is 4 mm<sup>2</sup>, out of which 2 mm<sup>2</sup> is the active area. A bandgap circuit to generate the reference voltage for the output is not included on this chip. According to [14], the reference circuit can be implemented with sub- $\mu\text{A}$  current consumption. The required pin count for the buck converter IC is 10, and all of the other pins

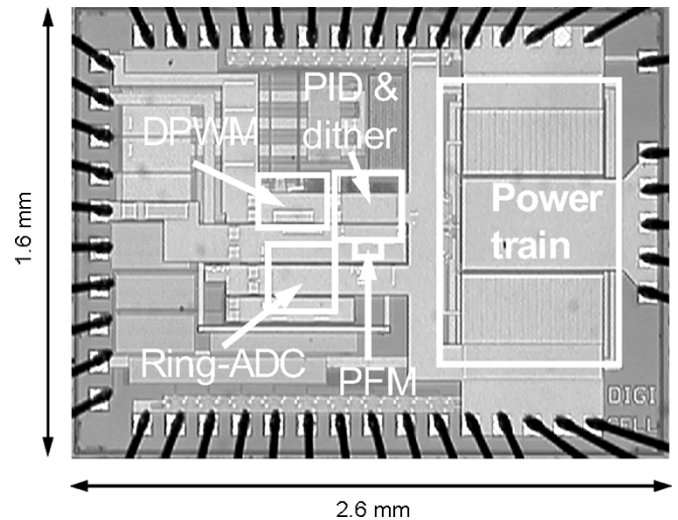


Fig. 7. Chip microphotograph.

TABLE I  
CHIP PERFORMANCE SUMMARY

Technology	0.25- $\mu\text{m}$ CMOS (Max. supply 2.75 V)
Input voltage range	5.5-2.8 V
Output voltage range	1.0-1.8 V
External LC filter	$L=10 \mu\text{H}$ , $C=47 \mu\text{F}$
Maximum load current	400 mA
PFM mode sampling frequency	600 kHz
PFM mode quiescent current	4 $\mu\text{A}$
PWM mode switching frequency	0.5-1.5 MHz
PWM mode dc output voltage precision	$\pm 0.8\%$
PWM mode output voltage ripple	2 mV
Active chip area	2 mm <sup>2</sup>

are for test purposes. Table I summarizes the application and the measured performance of the IC.

Experimental closed-loop load transient responses with a current load step of 100 mA for the PWM and PFM modes, respectively, are shown in Fig. 8. In the PWM mode, it can be seen that the dc voltages at high load and low load are within the zero-error bin of the ADC, which is 16 mV. In the PFM

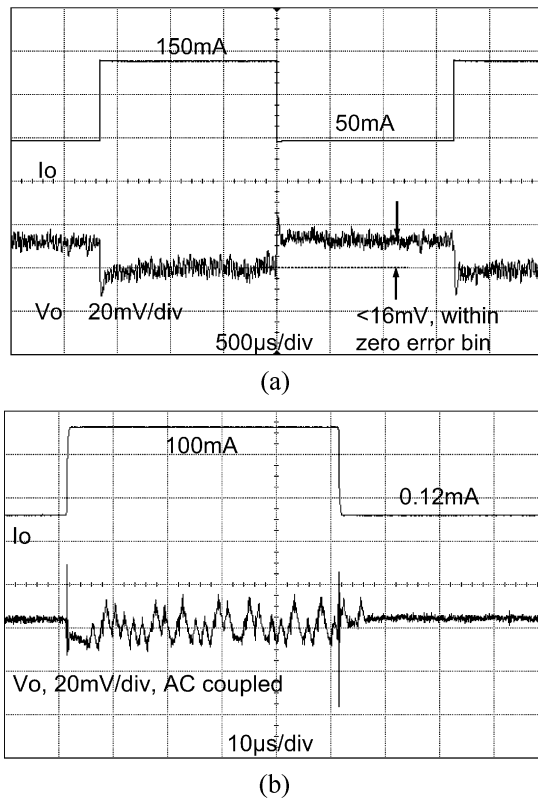


Fig. 8. Experimental load transient response with  $V_{in} = 3.2$  V,  $V_o = 1.2$  V. (a) PWM mode response with  $f_s = 1$  MHz. (b) PFM mode response with  $f_{s,PFM} = 600$  kHz.

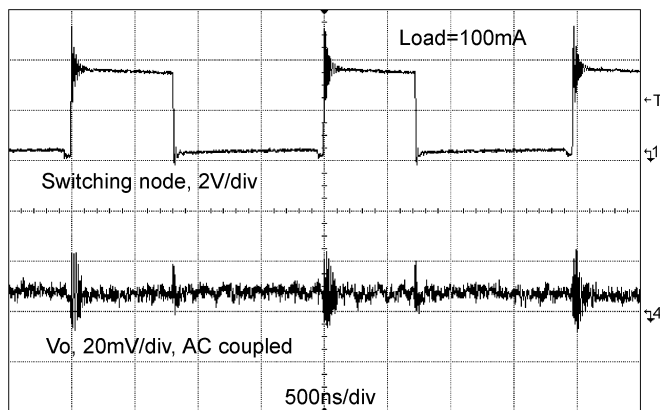


Fig. 9. Experimental steady-state response in PWM mode with  $V_{in} = 3.2$  V,  $V_o = 1.2$  V, and  $f_s = 500$  kHz.

mode, the voltage ripple is below 25 mV when the load current is 100 mA. Steady-state waveforms in the PWM mode are shown in Fig. 9. Efficiencies as a function of load current of the buck converter in both PWM mode and PFM mode are measured with  $V_{in} = 4$  V and  $V_o = 1.5$  V, as illustrated in Fig. 10. An efficiency of 92% is achieved in the PWM mode with a load current of 189 mA. It can be observed that 40 mA is the crossover point of the PWM and the PFM efficiency curves. Thus, when the load current is lower than 40 mA, the converter should be switched from PWM to PFM mode for better efficiency. Furthermore, over a 20–200-mA load current range, high efficiency (over 80%) can be observed in each mode, and thus it is easy

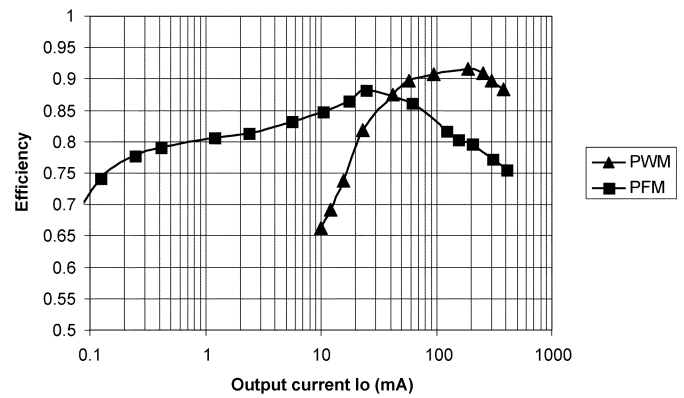


Fig. 10. Measured PWM and PFM mode converter efficiency as functions of output current, with  $V_{in} = 4$  V and  $V_o = 1.5$  V.

to implement a scheme to switch between the two modes due to the wide load range of overlapping high efficiency. A 47- $\mu$ F ceramic capacitor is used as the output capacitor in the experimental setup. A smaller capacitor can be used to reduce cost, with higher output voltage ripple as a tradeoff.

## VI. CONCLUSION

This paper describes an ultralow-quiescent-current dual-mode digital controller IC for high frequency dc–dc buck converters. Internal power management and power switch structures enable the use of a small feature size (0.25  $\mu$ m) CMOS process with voltages up to 5.5 V. The paper further demonstrates subthreshold operation of CMOS transistors as a viable very low-power option for analog–digital interface elements. The study illustrates the promise of implementing digital power management ICs in standard CMOS processes, with low power and small area, using a combination of digital processing and special purpose analog–digital interface structures.

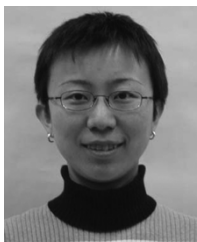
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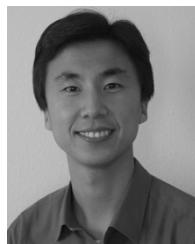


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