15.7 A 4μA-Quiescent-Current Dual-Mode Buck Converter IC for Cellular Phone Applications

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Digital control has been emerging as an option for high-frequency, low-power DC-DC converters [1-3]. This work is an effort to introduce digital control for a mass market power management application, i.e. cellular phones. When the phone is in talk mode, pulse width modulation (PWM) is used to achieve high quality regulation as well as good efficiency. However, in standby mode in which the load current is very low, PWM control leads to low efficiency due to excessive switching loss. To extend the standby time a cellular phone can sustain with each full charge of the battery, pulse frequency modulation (PFM) is used for light-load operation to achieve good efficiency. The quiescent power of the PFM mode is the fundamental limitation on light-load efficiency. We present a controller IC with 4μA quiescent current in PFM mode, compared to 15μA in state-of-the-art ICs [4]. As a result, the cellular phone standby time may be extended up to 3 times.

The system block diagram is shown in Fig. 15.7.1, in which the MODE pin is used to switch between the two modes. The PFM mode runs the converter in discontinuous conduction with variable switching frequency and fixed on-time. A clocked, zero-DC-current comparator [5] compares the output voltage V_o with the reference V_{ref}. When $V_o < V_{ref}$, the controller generates a constant duty ratio command word. A digital PWM (DPWM) module is used to convert duty ratio commands into pulses. Thus, a fixed-on-time pulse is generated to drive the high side switch to charge up the output capacitor. When $V_o \geq V_{ref}$, the converter is idling. A very low power DPWM based on a ring-oscillator-MUX structure is developed [6], in which the ring oscillator also generates all the clock signals for the entire controller.

The PWM mode runs the converter in continuous conduction mode. As shown in Fig. 15.7.1, the error voltage $V_e = V_o - V_{ref}$ is quantized by an ADC to provide a digital error signal D_e, and the digital PID compensation network generates a duty ratio command D. Digital dither is used in PWM mode to reduce hardware complexity of the DPWM, while maintaining high regulation precision [7]. Since V_o is regulated to be within a small window centered at V_{ref}, a full rail-to-rail quantization range of the ADC is not necessary. Instead, an ADC based on subthreshold-biased ring oscillators (Ring-ADC) is designed, realizing high resolution centered at V_{ref}. As shown in Fig. 15.7.2, the differential input voltage $V_e = V_o - V_{ref}$ is converted to a frequency difference by the input pair M_1-M_2 and the ring oscillators. Counters are used to capture the frequency of each oscillator, and the digitized error D_e is calculated accordingly. The Ring-ADC is nearly entirely synthesizable, and is robust against switching noise.

Small feature size processes with intrinsic low supply voltage are preferred to implement digital circuits. A 0.25μm CMOS process with highest allowable supply of 2.75V is used to implement the IC. The voltage from the battery in cellular phones is usually between 5.5V and 2.8V. As a result, internal power management is introduced to resolve the conflict of high input voltage and a low-voltage process, as well as to efficiently supply the low-voltage circuitry on the chip. As shown in Fig. 15.7.3, the power train switches are implemented with a cascode structure to sustain high input voltage. An intermediate voltage $V_m = V_{in}/2$ is needed to bias the cascode transistors MP2 and MN2, and also as proper supply to the digital circuits. A very low bias current class B regulator is used to provide a stable bias voltage V_m. The high-side gate driver works between supplies V_{in} and V_m, and the low-side gate driver works between V_m and ground. In each switching cycle, the average current I_p flowing into node V_m through the high-side gate driver is approximately twice the current I_n flowing out of V_m through the low-side gate driver, since the power train PMOS transistor has twice the width of the NMOS transistor in this design to optimize conduction loss. Thus, I_p is used to supply both the low-side driver and the control circuits. A total current saving of I_p is achieved in PWM mode.

The digitally-controlled buck converter IC is implemented in a 0.25μm CMOS N-well process. The die photo of the chip is shown in Fig. 15.7.4. The total chip area is 4mm^2, out of which 2mm^2 is the active area. The PWM and PFM mode closed-loop load transient responses for load current step of 100μA are shown in Fig. 15.7.5. The efficiency of the buck converter as a function of load current is plotted in Fig. 15.7.6. In PFM mode, approximately 1μA is drawn by the comparator, 2μA by the DPWM, and 1μA by the internal regulator, resulting in a total quiescent current of 4μA. Figure 15.7.7 summarizes the measured performance of the IC. This chip is implemented in a low-voltage digital process, demonstrating the possibility to integrate a power management unit with digital systems on the same die, resulting in significant cost reduction. This work indicates the promise of digital control as a high-performance, low-power, and low-cost alternative for power management.

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The authors greatly appreciate the guidance of Prof. Y. C. Liang of the National University of Singapore in the power train design during his visit from 2001 to 2002. We also thank National Semiconductor for the IC fabrication and Joe Emlano of National Semiconductor for chip packaging.

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[1] T. Burd et al, "A Dynamic Voltage Scaled Microprocesor Systems," *ISSCC Dig. Tech. Papers,* pp. 294-295, Feb. 2000.
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[3] G.-Y. Wei et al, "A Variable-Frequency Parallel I/O Interface with Adaptive Power-Supply Regulation," *IEEE J. Solid-State Circuits*, vol. 35, no. 11, pp. 1600-1610, Nov. 2000.
[4] Texas Instruments, "TPS62200 300mA High Efficiency Step-Down DC-DC Converter," data sheet, 2002.
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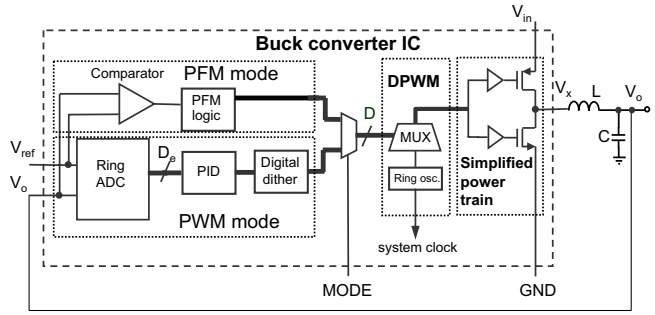

Figures 15.7.1: Block diagram of the dual-mode buck converter IC and external LC filter.

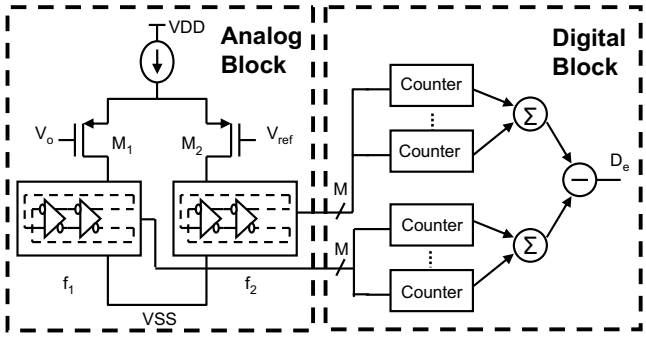

Figure 15.7.2: Block diagram of Ring-ADC.

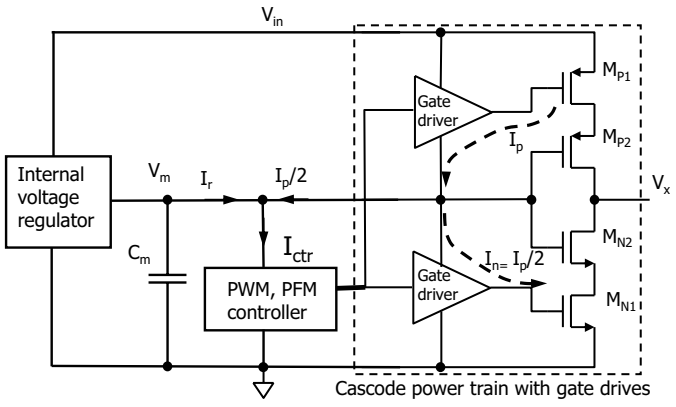

Figure 15.7.3: Block diagram of internal power management on the chip.

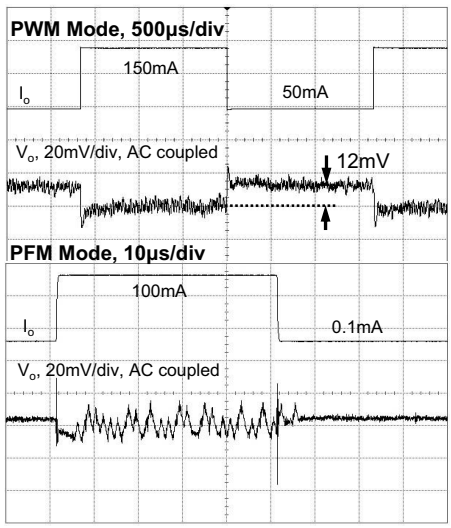

Figure 15.7.5: Experimental load transient response of PWM mode and PFM mode, with V_{in}=3.2V, V_o=1.2V.

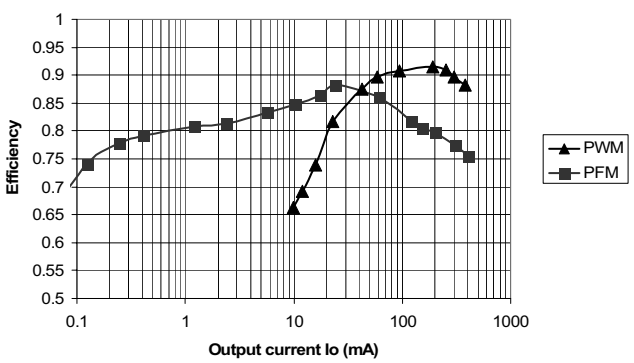

Figure 15.7.6: Measured PWM mode and PFM mode buck converter efficiency as a function of output current with V_{in}=4V and V_o=1.5V.

Technology	0.25µm CMOS (Max. supply 2.75 V)
Input voltage range	5.5-2.8 V
Output voltage range	1-1.8 V
External LC filter	L=10 µH, C=47 µF
Maximum output current	400 mA
PFM mode sampling frequency	600 kHz
PFM mode quiescent current	4 µA
PWM mode switching frequency	0.5-1.5 MHz
PWM mode DC output voltage precision	±0.8%
PWM mode output voltage ripple	2 mV
Active chip area	2 mm^2

Figure 15.7.7: Chip performance summary.

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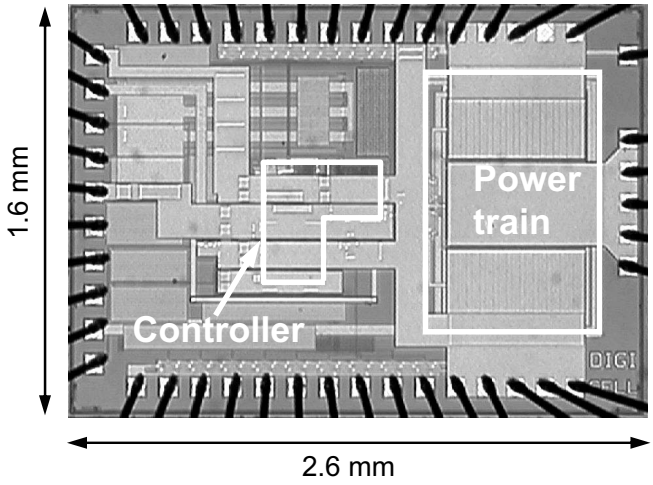
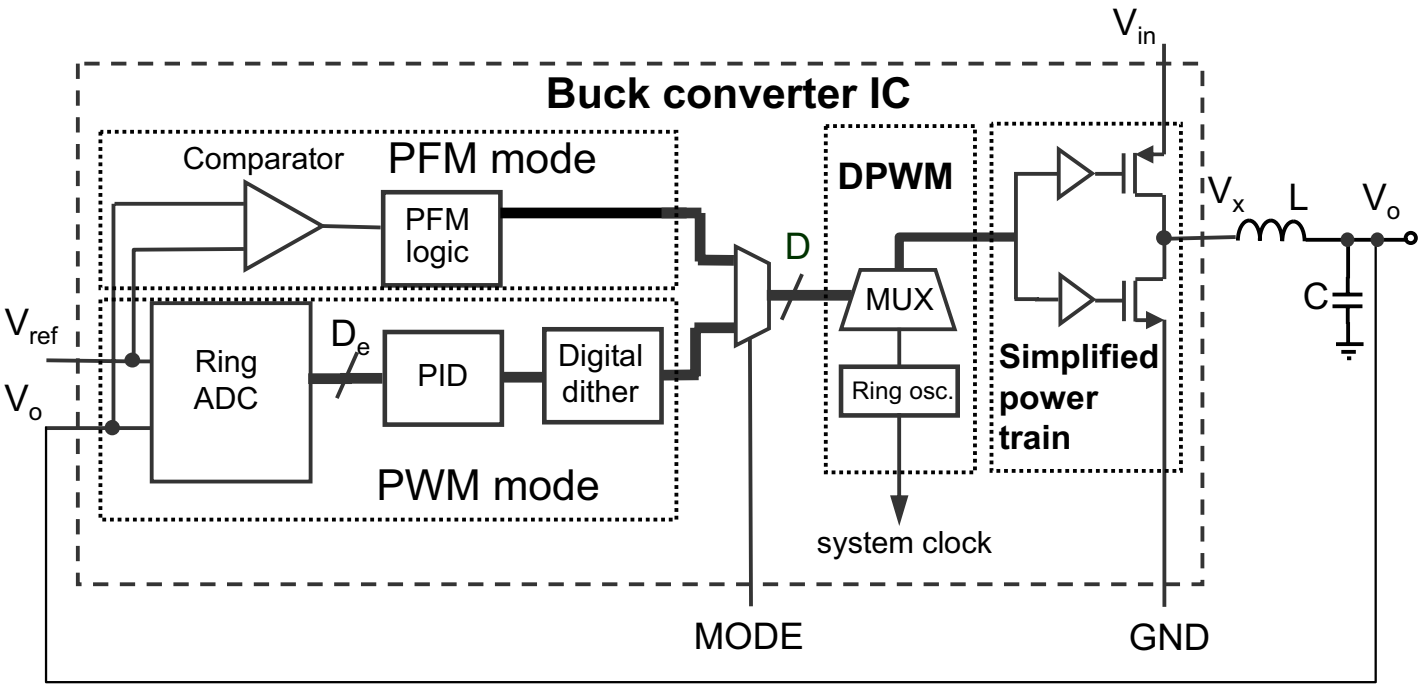


Figure 15.7.4: Chip micrograph.



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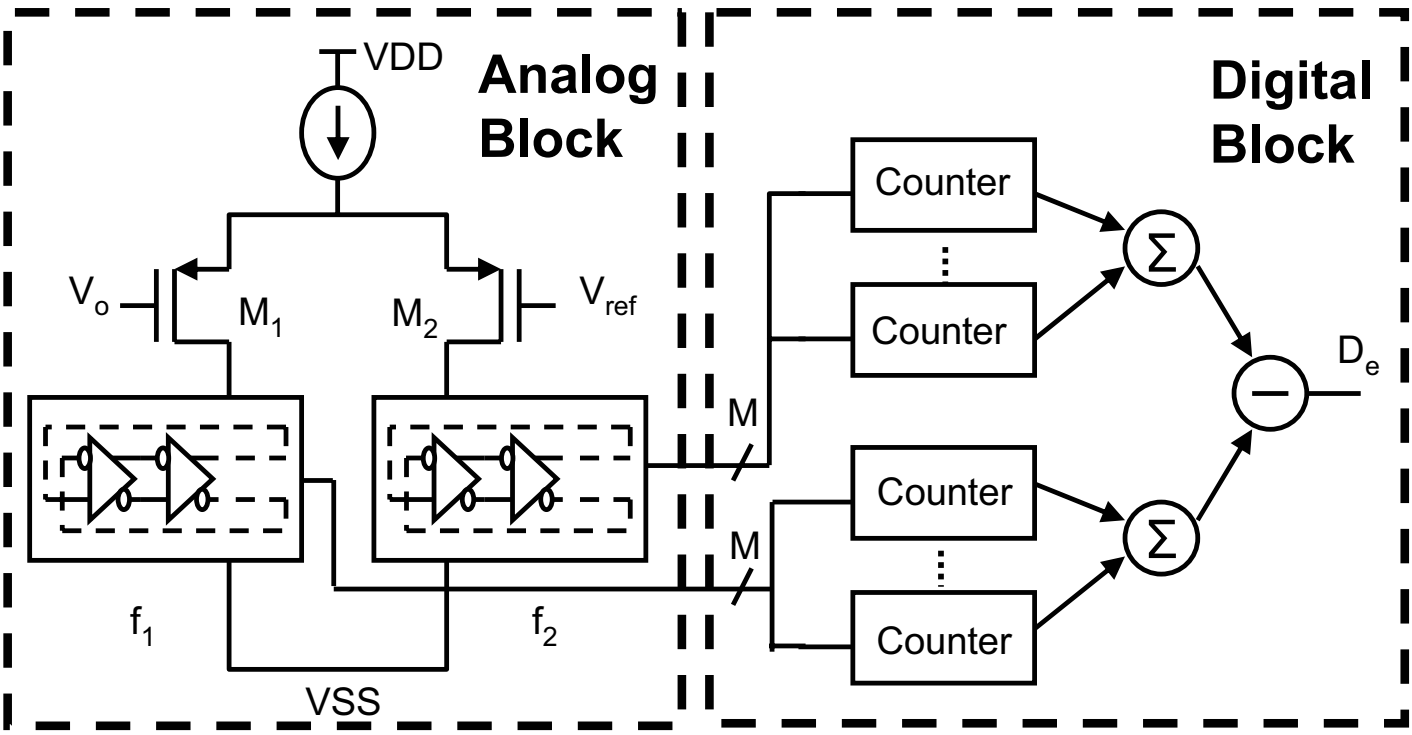

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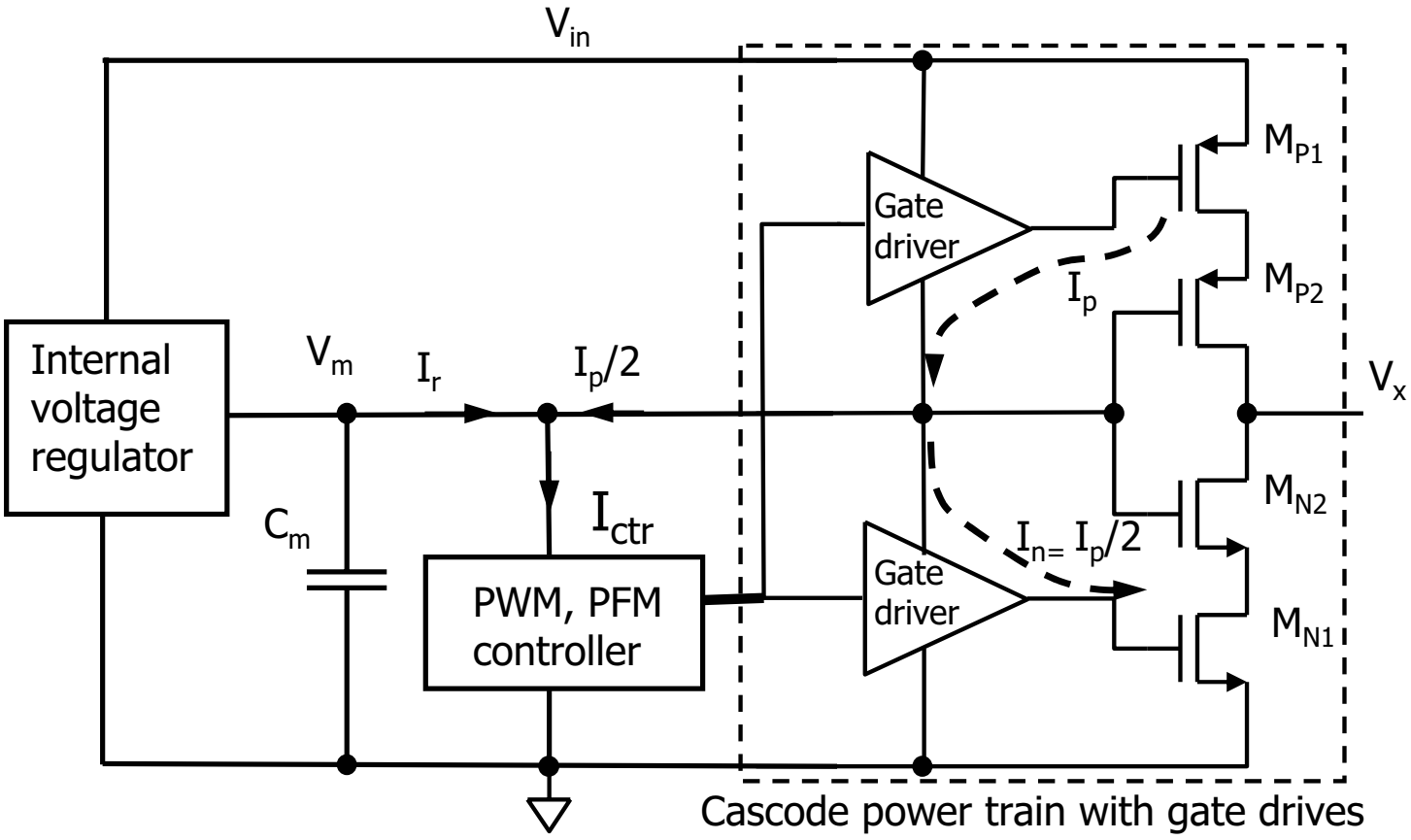

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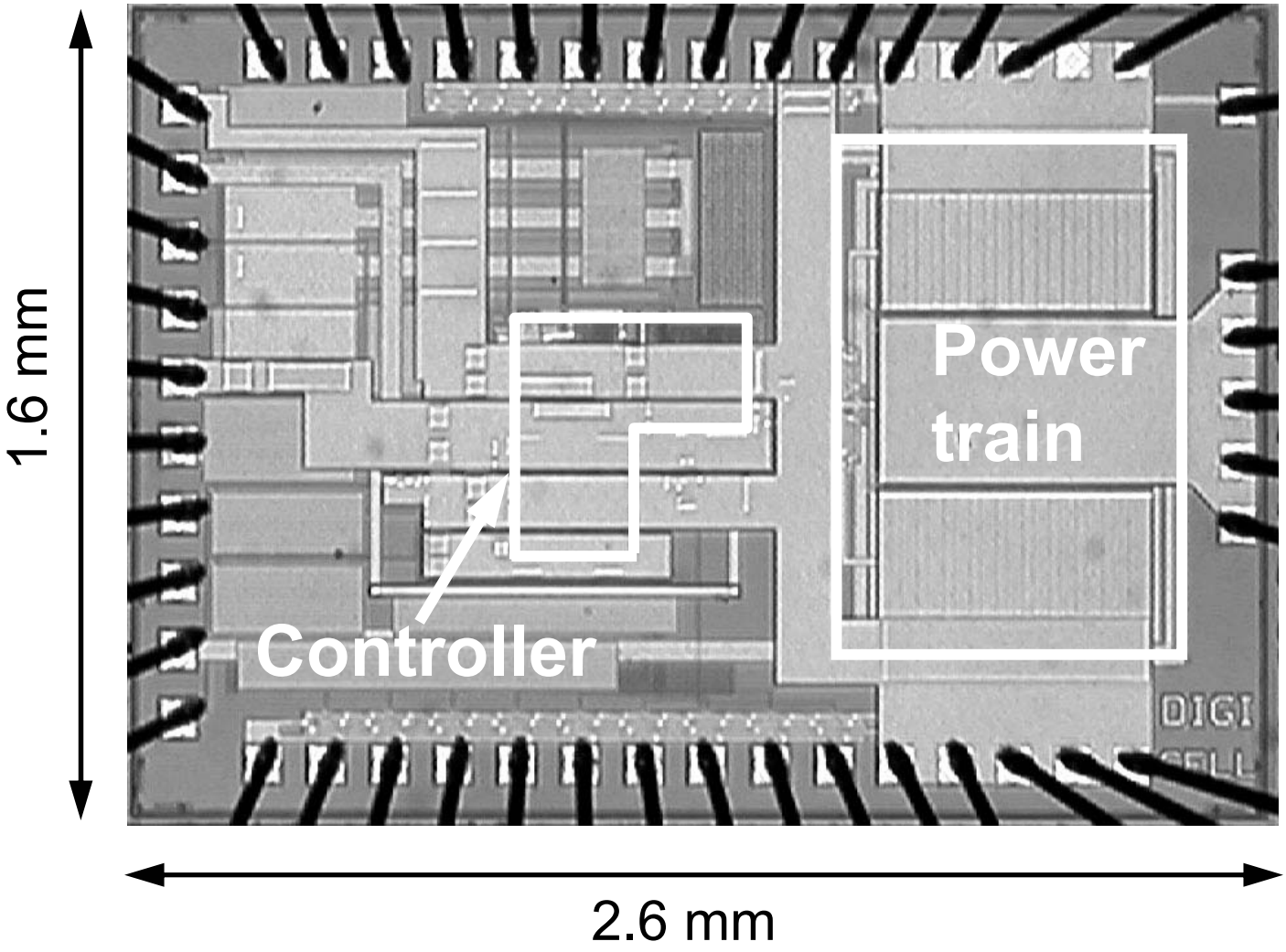

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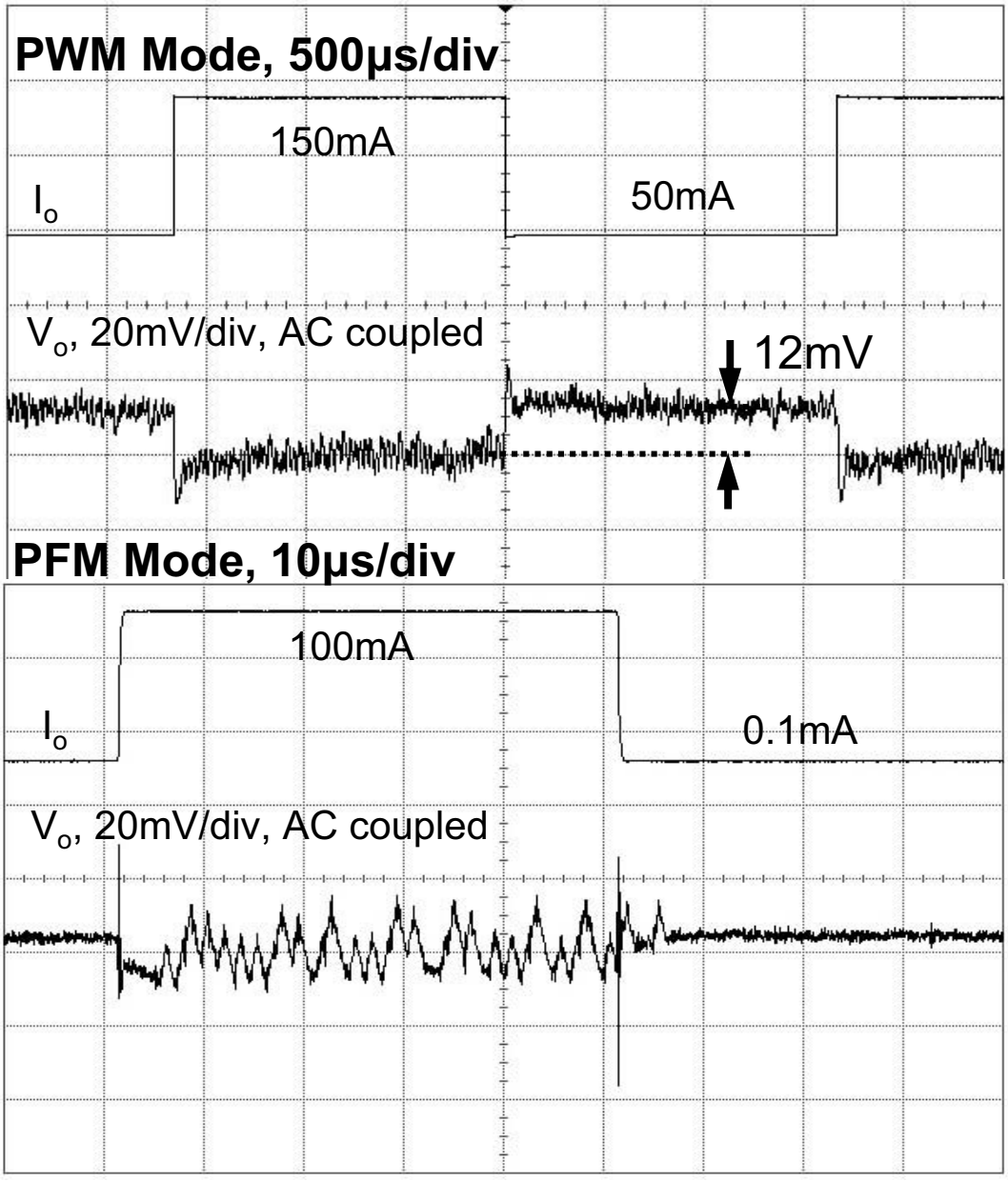

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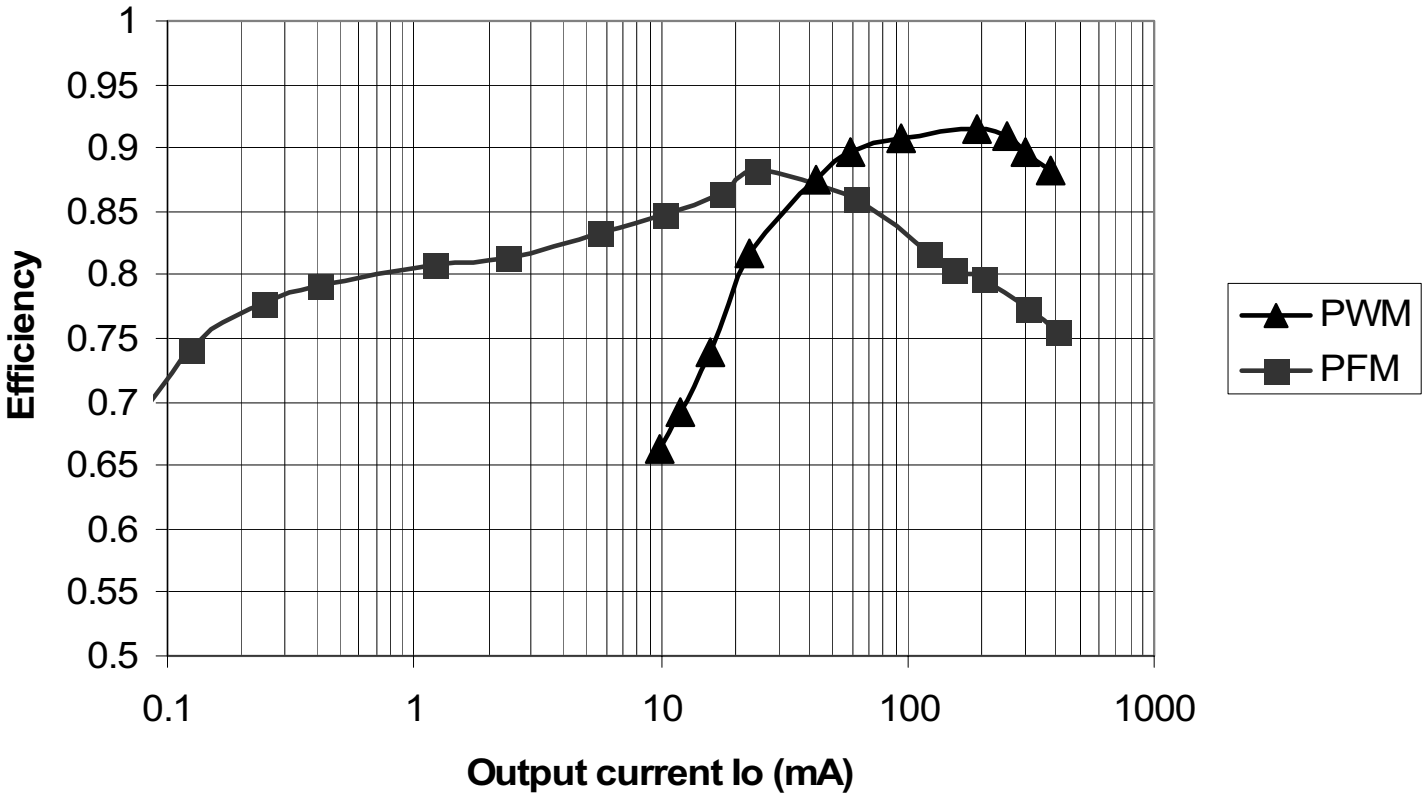

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