Digital PWM Control: Application in Voltage Regulation Modules

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1 Introduction

Conventionally, controllers for DC/DC converters have relied on analog circuit techniques for implementation. While analog based systems have proven successful, several reasons make digital control attractive. Digital control allows for the implementation of more functional control schemes. Digital circuits are potentially less susceptible to noise and parameter variations. With the recent explosion of cheap computing power, and availability of advanced integrated circuit design and synthesis tools, a digital controller design can be ported to new integrated circuit technology generations with little additional effort.

Current trends in microprocessor designs lead toward decreasing supply voltages and increasing current demands. Future microprocessors are projected to require between 30-60amps of static current and impose $\frac{di}{dt}$ requirements on the power supply on the order of 5 $\frac{A}{ns}$. In this paper, we focus on the design of a digital controller for an interleaved DC/DC Buck Converter to supply power for microprocessor loads. As will be seen, digital logic makes the generation of identical, but delayed, gate drive signals for the various phases of the interleaved converter simple.

2 Digital Control

2.1 Previous Work

In reviewing previous work in the area of digital controllers, it is evident that the majority of the work has been done in the control of medium or high power systems, such as line-interface inverters, variable speed drives, and UPS (uninterruptible power supply) systems([2], [3], [4]). The reason for this is obvious when one considers that cheap computational power is a recent development. Digital signal processing (DSP) chips have been used in the control of DC/DC converters([6],[7]). In these papers, the authors have been mainly concerned with proving that certain digital control schemes can work for power converters, and to a lesser extent, with practical circuit design issues, such as power consumption and achieving high switching frequencies. In fact, the switching frequencies for the applications considered in these efforts have been on the order of tens of kilohertz, or lower. One exception to this is in [8]. In this paper, an ultra low power control circuit for a PWM converter operating at 330kHz is designed, fabricated, and tested. A single bit analog-to-digital converter (ADC) is used to sample the output and adjust the duty cycle accordingly. The disadvantage of this approach is poor dynamic response.

2.2 Focus of Design

Our focus will be on the design of an integrated circuit digital controller requiring low bias power, and yet providing all the functionality needed in an advanced microprocessor voltage regulation module (VRM). Ultra low power designs (i.e. single bit digital systems) would not be adequate in supplying microprocessors due to poor transient response. We believe a reasonable solution can be based on an 8-, 9-, or 10-bit system, implementing feedback and feedforward control.

2.3 Application in Interleaved Buck VRM

The concept of interleaved converters was first introduced in [1]. A good treatment of the previous work in the area is given in [5]. The method has been applied in VRM applications in [9]. Figure 1 shows the typical waveforms of an interleaved buck converter with four phases. The gate drive signals are operated in quadrature as shown in the upper plot. The lower plot shows typical current waveforms through the four inductors, L_1 - L_4, and the total current, I_{total}. The fundamental frequency component of the current in L_1 - L_4 is canceled in I_{total}, which results in significant ripple reduction. In fact, the spectrum seen at either the output or the input contains only $4n$ harmonic components of the fundamental.

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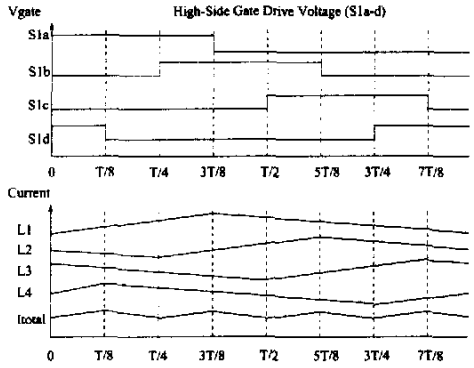

Figure 1: Waveforms of an Interleaved DC/DC Converter

Figure 2 shows an application diagram of the proposed controller. The justification for using an interleaved approach in this application is as follows. Since the design calls for maximum currents in the range of 30-60amps, there exists a necessity in using several power switches in parallel, each rated for a fraction of the total current. Thus, given that multiple switches will be used, by operating them in quadrature, we achieve the added advantage of ripple reduction. If n phases are used in a buck converter, the lowest frequency seen at the input and output is the n-th harmonic of the switching frequency. Thus, if voltage ripple is kept constant, the input and output capacitances can be reduced by a factor of n. To keep fractional ripple current invariant with respect to a reference single-phase design, one would actually need to increase each of the phase inductances by n. However, this may not be a constraint, and may be undesirable. In fact, to keep the output ripple voltage invariant, one could choose to use n inductors, each with inductance equal to that used in the single-phase reference circuit. With this choice, fractional ripple current is increased, but the total parallel inductance is reduced, along with the magnetic energy storage. This reduction allows for much faster transient response to step load variations, provided an override signal is provided so that all phases are activated under a large load transient condition. By using the interleaved topology, the amount of output capacitance needed is reduced to a point where only multilayer ceramic capacitors can suffice .

One key issue to consider is that of current sharing. At least two approaches exist to solve the problem. One is to actively enforce equal sharing of the total load current among the various phases of the converter. This can be accomplished by current sensing and/or estimation, followed by adjustment of the duty cycle of the different phases, on an individual basis, to correct for any mismatch. A second approach, that we follow here, relies on passive current sharing, also known as the "droop method". With passive current sharing, mismatches are generated by duty cycle mismatch and power train CDC resistance mismatch. Duty cycle mismatch can be reduced to negligible levels with digital control. On the other hand, power train dc resistance mismatch cannot be eliminated. The strategy here is to accept the dc current distribution imposed by the dc resistances of the various legs of the power train. It turns out that the resulting power dissipation is actually minimized. Specifically, the leg of the power train with lowest dc resistance takes the largest dc current, and so on. The positive temperature coefficient of the MOSFET devices and metallic conductors guards against the possibility of thermal current run-away.

2.4 Digital Controller Function

Figure 3 shows a block diagram of a prototype digital controller. The combined proportional-derivative (PD) and feedforward control law is as follows:

$$D_c(k+1) = KD_e(k)+\frac{KT_D}{T}(D_e(k)-D_e(k-1))+D_f(k) \quad (1)$$

where T is the period of the switching cycle, T_D and K are gain parameters, D_f is the feedforward duty cycle, D_e is the error voltage scaled by V_{in}, and D_c is the commanded duty cycle. Signal D_f is generated by connecting the input high pin of an analog-to-digital converter (ADC) to V_{in} and the input low pin to ground. The analog input pin is connected to V_{set}, the desired output voltage reference. Thus, D_f is approximately equal to V_{set}/V_{in} which is the desired feedforward duty cycle. The second ADC also has V_{in} and ground as input high and low pins, but has V_{out} as the analog input. The output of this ADC, D_{out}, is the output voltage scaled by V_{in}. Using D_f and D_{out}, the error in the duty cycle, D_e, is calculated. The derivative (finite difference) term is calculated by using the value of D_e from the previous cycle. Thus, combining these terms with some gain parameters yields the PD control with feedforward. Note that the two ADC functions here may be multiplexed with a single hardware ADC.

The sequence of operation is as follows: the ADCs sample the output and reference voltages once per switching cycle, the P-D(Proportional Derivative) block calculates the desired duty cycle for the next cycle, and the latches are used to apply the duty cycle to the D-PWM(Digital to PWM) blocks with the appropriate delay to insure quadrature operation.

2.5 Digital to PWM Block Design

Power consumption plays an important role in the design of the digital controller due to the presence of a high speed clock. In our design, we plan on using 8,9, or 10-bit modulation. Switching frequency is targeted to be in the range of 300kHz, and thus the fast clock needs to be 2^8, 2^9, or 2^{10} times this switching frequency, depending on the number of bits

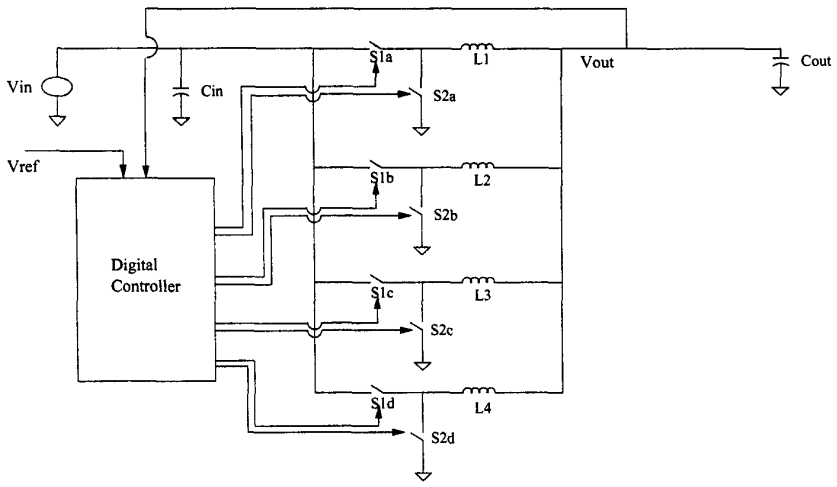

Figure 2: Functional Block Diagram of Converter and Digital Controller

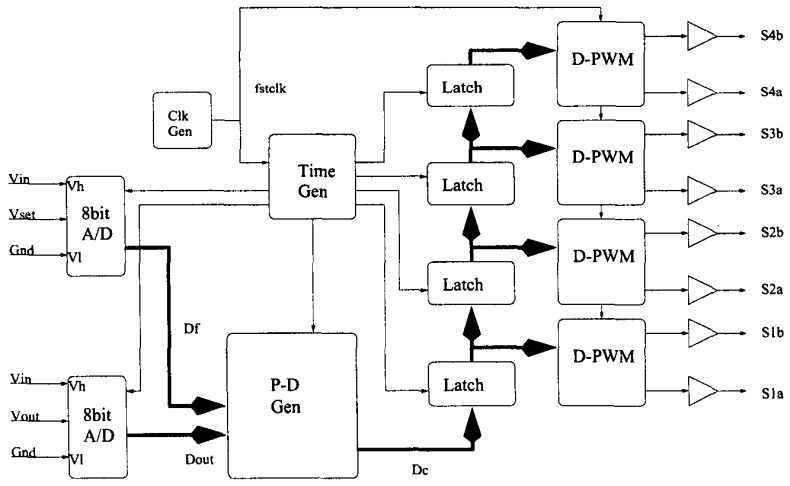

Figure 3: Block Diagram of Digital Controller

used. This fast clock needs to be distributed to all four D-PWM blocks in order to obtain the desired discrete duty cycle levels. Thus the design of a low power D-PWM block is important for achieving high efficiency, especially at light loads.

A novel circuit that accomplishes this, for an 8-bit system, is shown in Figure 5. This circuit does a sequential comparison of the commanded duty cycle, D_c to the output of an asynchronous counter, Q_7, Q_6, ..., Q_0. For example, if D_c = 11000000, then by observing that $D_7 = 1$, one knows that the duty cycle is greater than 50%. Thus the D-PWM circuit waits until Q_7 goes high, before allowing the enable signal to propagate to the next cell. Any cell that has $D_i = 0$ will be transparent to the propagating enable signal. Thus, only one bit of D_c is compared at a time. The output of the last cell is the PWM output. The worst-case timing path is for D_c = 10000001. Because $D_7 = 1$, the enable signal will wait for Q_7 to go high. When this happens, the enable signal must race down through the D_6-D_1 cells before Q_0 goes high to achieve the correct PWM output. Thus, the delay though the asynchronous counter plus the delay down the combinational logic chain must be less than one period of the fast clock. Note that only one cell of the D-PWM block is clocked with the fast clock, which is desirable in a low power design.

3 System Issues

A number of basic issues need to be addressed in the design of a digital control system. The resolution of the ADC and digital-to-analog (D-PWM) conversion processes need to be selected to meet the application requirements. With a 5V VRM input voltage, a 10-bit system allows for approximately 5mV of resolution, which should be adequate for many applications. However, it is not clear that an equal resolution should be applied in the ADC and in the D-PWM functions.

An important issue in digital control is the possibility of multiple switching period limit cycles and even non-periodic steady state behavior. This behavior occurs when there is not a quantized control value that exactly corresponds to the commanded quantized output variable. On the other hand, it is actually possible to have the digitally controlled system exhibit a steady state behavior analogous to that often achieved in analog controlled systems, namely a single switching period limit cycle. For this to be achieved robustly, it is necessary that the resolution of the digital-to-analog conversion process (D-PWM) have finer granularity than that of the ADC. In this case, it is generally possible that there will be a digitized PWM command that maps into the desired output quantization bin, which corresponds to exactly zero error after quantization. Then, it is also necessary that the digital controller maps this zero error value, in equilibrium, into one of the PWM command words that maps back to the zero error bin. Figure 4 illustrates the situation where multiple bits of the D-PWM process map into the zero error output bin. With a system designed as outlined here, a desired steady state corresponding to a constant sampled output is feasible. This behavior has been verified experimentally, as discussed in Section5.

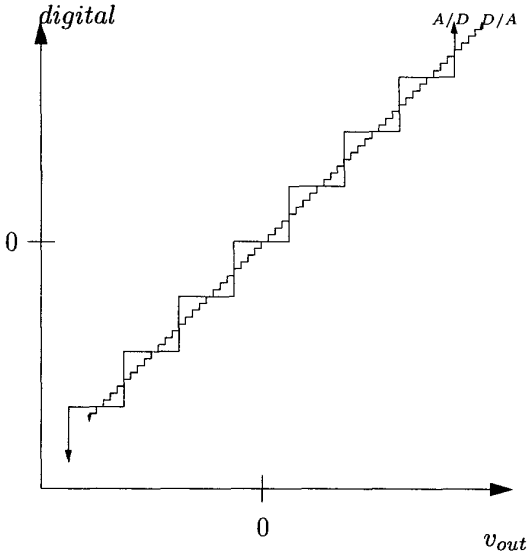

Figure 4: Limit-Cycle Map

Transients are normally governed by excursions that transcend many quantization levels, and thus the behavior may be analyzed by conventional continuous variable techniques, with the effect of the quantization acting roughly as a random noise source. With asymptotically stable behavior, the trajectory can converge to the desired operating quantization bin.

We believe issues concerning quantization and impact on steady state behaviors merits further study.

4 Simulation Results

Various blocks of the digital controller were simulated using Level 39 HSPICE models for an HP .5um, 3.3V CMOS process in order to test functionality and evaluate power dissipation . Power dissipation results are listed in Table 1. Note the low power dissipation of the D-PWM block. Had a synchronous logic approach been taken(i.e. fast clock driving all cells of the counter), this power number would be approximately eight times greater. Thus the total power dissipation of all four D-PWM blocks would be close to 12 mW and would be dominant. The D-PWM has the strictest timing constraints and is shown to function properly with this particular technology at a fast clock rate of 76.8MHz.

The entire digital controller has been designed in a

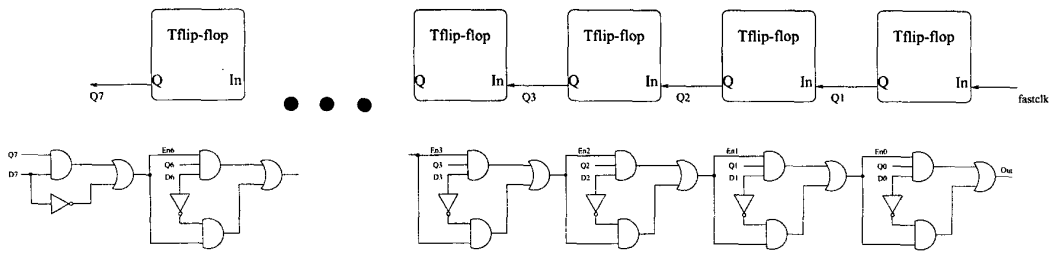

Figure 5: Diagram of D-PWM Block

Circuit Block	Power Dissipation
D-PWM Block	.4 mW (avg)
P-D Block	.8 mW
Time Gen	.8 mW

Table 1: Power Dissipation of Controller

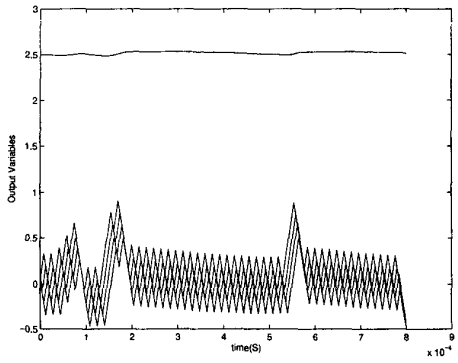

Figure 7: Matlab Simulation Exhibiting Non-Periodic Steady State. Top: Output Voltage. Lower: 4 Inductor Currents.

Hardware Description Language (Verilog HDL). Due to the flexible nature of using HDL in design, implementation in any technology is relatively simple. Figure 6 shows results obtained using a Verilog simulator. The waveforms from top to bottom are: feedforward term D_f, equivalent output duty cycle term D_{out}, calculated duty cycle D_c, and the four PWM signals operating in quadrature. The digital words are represented in hexadecimal format.

Matlab simulations were used to study both the dynamic and steady state behavior of the digital controller. A standard ODE solver is used to integrate the state equations between switch instances. All switching events are explicitly controlled. Figure 7 shows a Matlab simulation displaying a portion of non-periodic steady state behavior. The upper waveform is the output voltage, while the lower waveforms are the individual currents in the inductors.

5 Experimental Work

Since the Verilog HDL description is readily ported to many technologies, it is possible to carry out an experiment with a Field Programmable Gate Array (FPGA) implementation, which has been done. The chip used is the Xilinx XC4010-XL. Due to the speed constraints imposed by this Xilinx chip, the fastest rate of operation for the controller fast clock is approximately 16 MHz. This results in a switching frequency of 62.5 kHz for the converter, if eight bits are to be used in the D-PWM function. The inductors and input and output capacitors were also scaled for operation at this lower frequency. Inductors of $75uH$ were used, along with an output bulk capacitor of 1.5 mF. To allow for the possibility of single-period limit cycle behavior, the ADC used to sample the output voltage was only six bits, while that for the feedforward was eight bits. The D-PWM function allowed for eight bits of resolution.

Figure 8 shows the steady state operation at light load. A single-period limit cycle is seen. Voltage ripple is extremely small, on the order of a few millivolts. For this particular case, since the duty cycle is nearly 50%, almost perfect ripple cancellation occurs. Figure 9 illustrates a steady state behavior at 3.6A load. Note the multiple period limit cycle behavior. The upper traces are the phase-1 and phase-3 inductor currents, which are seen to track with nearly zero dc offset. Figure 10 shows the output voltage during a load transient from light load to 9.2 Amps. The lower trace is the output voltage at 100mV/div, and the upper trace shows one of the high side PMOS gate drive signals. Note that with only six bits of ADC sampling the output voltage, the entire voltage transient traverses only two or three LSB levels. This likely accounts for the appearance of erratic behavior. Recovery still appears to occur in a few switching periods.

6 Conclusions and Comments

With modern digital IC design tools, digital controllers for many PWM applications, previously addressed with mixed-signal IC technology, are now more easily realizable. Digital control does bring up

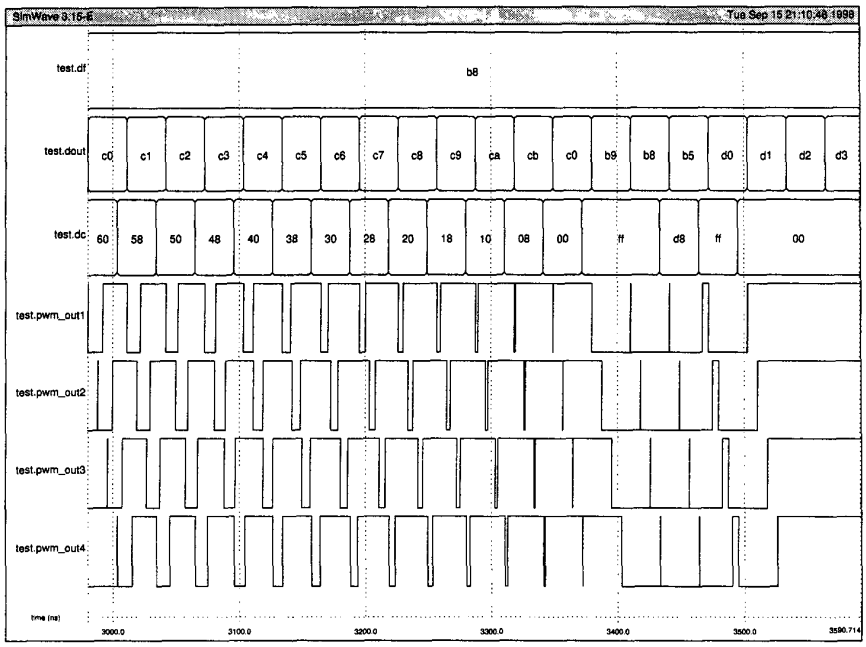

Figure 6: Verilog Simulation of Digital Controller. From the top: feedforward, digitized output voltage, digitized control (all in hexadecimal), followed by four-phase PWM signals.

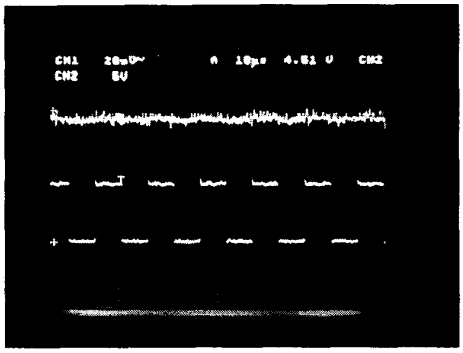

Figure 8: Steady State Operation at Light Load with Single-Period Limit Cycle. Top: output voltage at 20mV/div. Bottom: one of the gate drive signals.

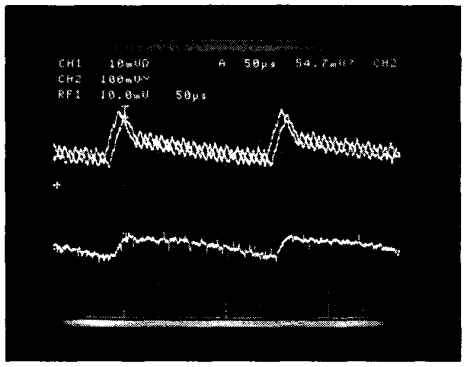

Figure 9: Steady State Operation at 3.6A Load. Behavior appears to correspond to a multiple period limit cycle. Lower trace: Output voltage at 100mV/div. Upper traces: Phase-1 and Phase-3 inductor currents at 0.5A/div.

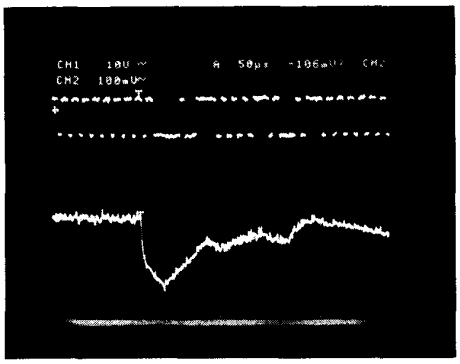

Figure 10: Transient Response from Light Load to 9.2Amps. Lower trace: Output voltage at 100mV/div. Upper trace is a high-side PMOS gate drive.

more complex system issues, such as limit cycle or even non-periodic behavior, both of which have been exhibited in our experiments. Further study of these issues are needed to more accurately predict and possibly design for these behaviors. We have successfully implemented a digital controller in an FPGA and a custom IC is currently under design.

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