Contactless USB - A Capacitive Power and Bidirectional Data Transfer System

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***Abstract*—This paper extends the Universal Serial Bus (USB) standard to the contactless domain by combining bidirectional data communication with a capacitive power transfer interface. This work first addresses the power transfer with analysis, simulations, and experiment, based on a secondary side phase feedback series resonant topology. This gives the advantage of simple circuitry to regulate output voltage over large parametric variations of the capacitive interface. Secondly this work presents the data communication analysis, simulations and experiment where differential mode voltage containing the data information rides on top of the larger power voltage. An experimental prototype was built to deliver 1.25W of power with 53% overall efficiency over a total of 300pF capacitance with an area of 52cm^2, also realizing 100Mb/s bidirectional data communication.**

I. Introduction

With the formation of the Qi standard[1], wireless charging of portable devices such as smartphones, ipads, and laptop computers is gaining momentum in changing the way we provide power to devices. The Qi standard is based on an inductive interface, shared between the power transmitter, such as powermat[2], and a portable device, such as a mobile handset. Power is transfered wirelessly through magnetic fields. However, another approach exists in the form of a capacitive interface, formed by two metal plates separated by a thin layer of isolation[3]. In comparison to an inductive interface, a capacitive interface is more limited in separation distance. With a receiving device resting directly on the charger, this need not be a limitation. In favor of capacitive charging, the capacitive interface has much reduced external fields, a single resonance, and no need for substantial reactive magnetizing current[4].

The main attractiveness of wireless charging is its unconventional way of charging, deviating from the mainstream of cables and wires. However, one important aspect still absent is the data communication. Existing capacitive power and data technology is either very near field with μm range for chip-to-chip applications[5] or for biomedical applications where the data rate is low[4][6]. This work fully extends the USB interface to the contactless domain. The USB port provides both power and data channels to devices. As such, this work accomplishes both aspects with similiar specifications to those of the USB standard, watts of power and hundreds of megabits to gigabits of data. A simplified block diagram of the power and data transfer is illustrated in Fig. 1. Here the differential mode voltage (DM) provides the data communication to the receiver while the larger common mode (CM) voltage delivers power. The top side circuitry transmits data from the primary side to the secondary side. At the same time, an independent data channel is on the bottom delivering data from the secondary side to the primary side.

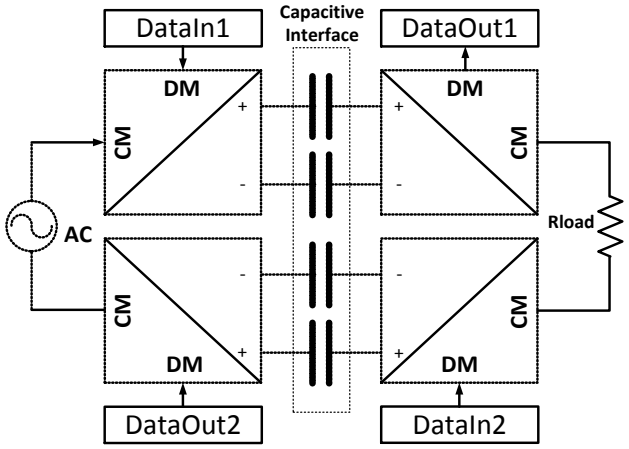

Fig. 1: Simplified Power and Data Transfer Block Diagram

Section II provides the analysis and the simulations of capacitive power transfer. Section III provides the analysis and the simulations of capacitive data communication. Section IV compares experimental work with previous analyses. Section V contains the conclusion.

II. Capacitive Power Transfer Analysis

Fig. 2 shows the detailed power and data transfer circuitry. Each part of the circuitry will be explained and analyzed in detail in the paper. The power transfer section is a series resonant converter (SRC) with active H-bridges on both the primary side and the secondary side. The primary side H-bridge has a low voltage supply of $5V$, compatible with the USB supply voltage. This is followed by a $(1:10)$ transformer to boost the voltage level to $50V$ to allow for efficient power delivery. The $(1:10)$ transformer contains large leakage inductance which is incorporated into the resonant inductance

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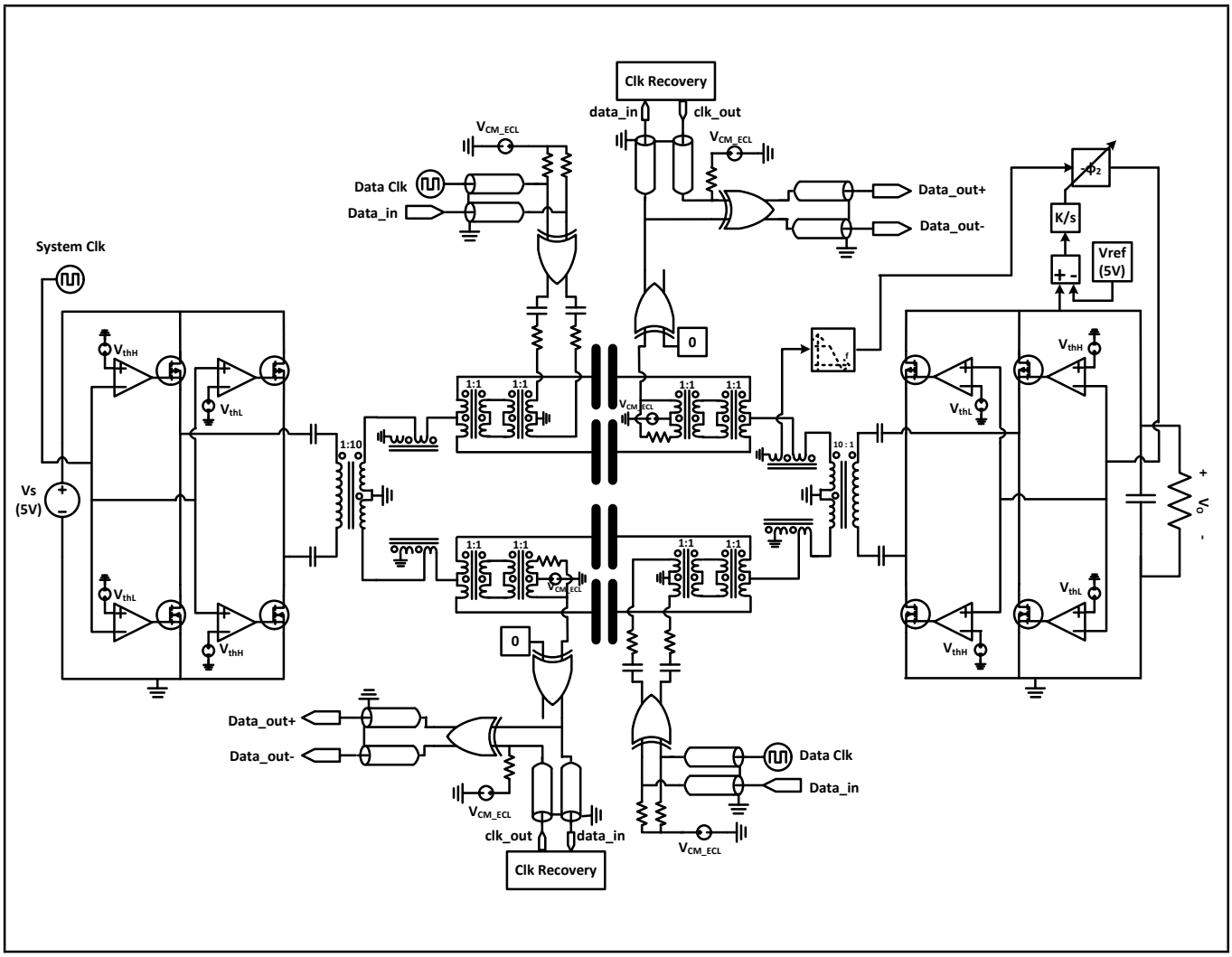

Fig. 2: Detailed Capacitive Power and Data Transfer

used to tune out the capacitive interface. This allows for a low impedance path along which ac current can flow to deliver power. With the resonant inductance as a parameter, the switching frequency and therefore the impedance of the capacitor can be adjusted in order to provide a safe voltage across the capacitive interface. The secondary side architecture is nearly identical to the primary side, except the H-bridge is connected to a load instead of to a supply voltage. Furthermore, separate independent inductors are incorporated into the secondary side. These independent inductors are used both for increasing the overall resonant inductance and for providing a method for sensing current. Current sensing in the inductor is done by low passing the secondary winding voltage on the inductor. With regard to the gate drive signal, the primary side gate drive is done by a system clock running nominally at 2.3MHz and the secondary side gate drive is phase delayed with respect to the tank current. The phase shift is denoted $-\phi_2$. The notation ϕ_1 is the phase difference between the phase of the primary side H-bridge and the tank current. Output voltage is regulated to $5V$ by sensing the output voltage and modulating $-\phi_2$. The analysis is divided into two subsections. Subsection II.A. contains the basic analysis of this secondary side phase feedback SRC circuit. Subsection II.B. contains the simulation results regarding power transfer.

A. *Fundamental Analysis*

A functional representation of the power transfer is illustrated in Fig. 3. Primary side H-bridge supply voltage is replaced by MV_S and the secondary side load voltage is replaced by MV_O, due to $(1 : 10)$ transformers. R_T is the equivalent series resistance in one half of the RLC tank. The total inductance in the tank is $2L$ which is a summation of both the leakage inductance in the two $(1 : 10)$ power transformers and the independent inductors used for current sense. The inductance $\frac{L}{2}$ is evenly distributed to make the functional diagram symmetrical allowing for simple analysis. The phase difference between the system clock and the tank current is denoted ϕ_1 and the phase difference between the output ac voltage and the tank current is denoted $-\phi_2$.

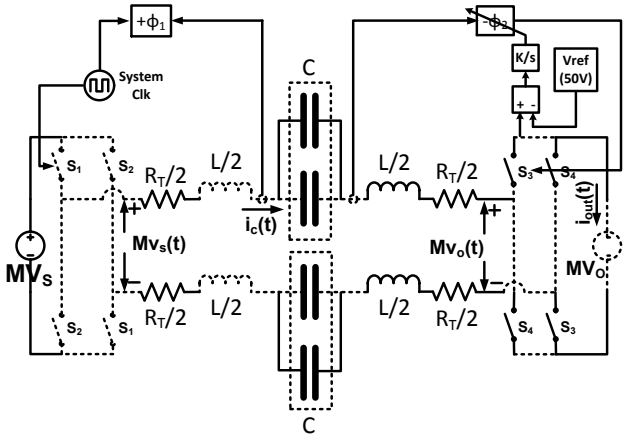

Fig. 3: Series Resonant Converter with Phase Feedback

A phasor plot of $Mv_s(t)$, $Mv_o(t)$ and $i_c(t)$ is illustrated in Fig. 4. to capture the steady state solution to the SRC system. Fig. 4 contains phasors $\frac{4}{\pi}MV_Se^{+j\phi_1}$, $\frac{4}{\pi}MV_Oe^{-j\phi_2}$ and I_A, assuming an operating point with negligible series drops and a current phasor as a reference with its phase equal to 0. Notice that under the ideal case when $R_T = 0$, the tank current is perpendicular to, and lagging the tank voltage.

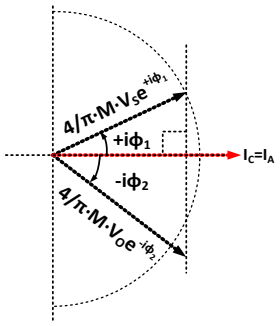

Fig. 4: Series Resonant Converter with Phase Feedback

According to Fig. 4, with X_T being the imaginary impedance formed by L and C,

$$I_A = M\frac{4}{\pi}\frac{V_Se^{+i\phi_1} - V_Oe^{-i\phi_2}}{2(R_T + iX_T)} \tag{1}$$

With some manipulation of Eqn. 1, we get an expression of V_O,

$$V_O = V_S\frac{X_T\cos\phi_1 - R_T\sin\phi_1}{X_T\cos\phi_2 + R_T\sin\phi_2} \tag{2}$$

Here we define the quality factor Q_T as,

$$Q_T = \frac{X_T}{R_T} \tag{3}$$

When $Q_T \gg 1$, $\phi_1 \leq 45^o$ and $\phi_2 \leq 45^o$,

$$V_O = V_S\frac{\cos\phi_1}{\cos\phi_2} \tag{4}$$

and I_A is simplified to,

$$I_A = M\frac{2}{\pi}\frac{V_Se^{+i\phi_1} - V_Oe^{-i\phi_2}}{iX_T} \tag{5}$$

$$= \frac{2}{\pi}\frac{1}{X_T}MV_S\frac{\sin(\phi_1+\phi_2)}{\cos\phi_2} \tag{6}$$

And P_{out} becomes,

$$P_{out} = \frac{8}{\pi^2}\frac{1}{X_T}M^2V_S^2\sin(\phi_1+\phi_2)\frac{\cos\phi_1}{\cos\phi_2} \tag{7}$$

Under output voltage regulation, $V_O = V_S$, which implies that $\phi_1 = \phi_2 = \phi$ from Eqn. 4. With this simplification, and I_A is simplified to,

$$I_A = \frac{2}{\pi}\frac{1}{X_T}MV_S\sqrt{2-2\cos(2\phi)} \tag{8}$$

And P_{out} becomes,

$$P_{out} = \frac{8}{\pi^2}\frac{1}{X_T}M^2V_S^2\sin 2\phi \tag{9}$$

B. Simulations Results

Fig. 5 shows the output voltage and the tank current versus time. The dark solid line is the output voltage V_O whose scale is on the right. It begins at $0V$, rises above $5V$, peaks around $6.2V$ and settles down to $5V$. Waveform $i_c(t)$ is shown by the dashed curve with scale to the left of the graph. At time $= 25\mu s$, the capacitive interface experiences doubling of capacitance. The total capacitance changes from $300pF$ to $600pF$. The output voltage drops to $4.5V$ and settles to $5V$ due to secondary side phase modulation. Fig. 6. shows the steady state time domain waveforms for the H-bridge current $10i_c(t)$, primary side ac voltage $v_s(t)$ and secondary side ac voltage $v_o(t)$. Waveform $10i_c(t)$ is used instead of $i_c(t)$ because $10i_c(t)$ is the actually current going through the H-bridge instead of the tank current due the (1:10) power transformer.

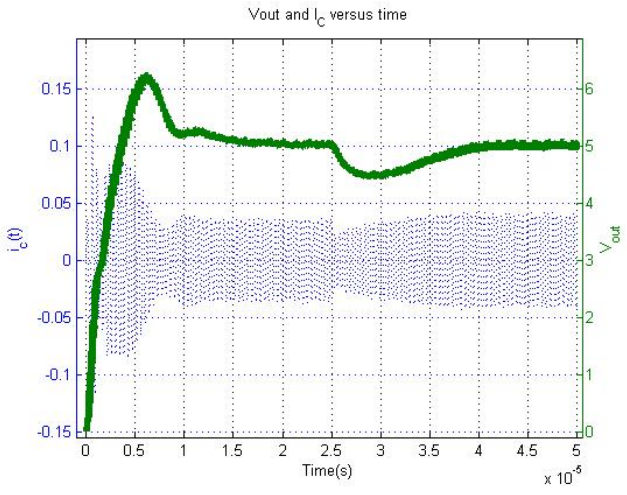

Fig. 5: Output Voltage $V_O(t)$ and Tank Current $i_c(t)$ during Startup, Settling, Capacitive Interface Change

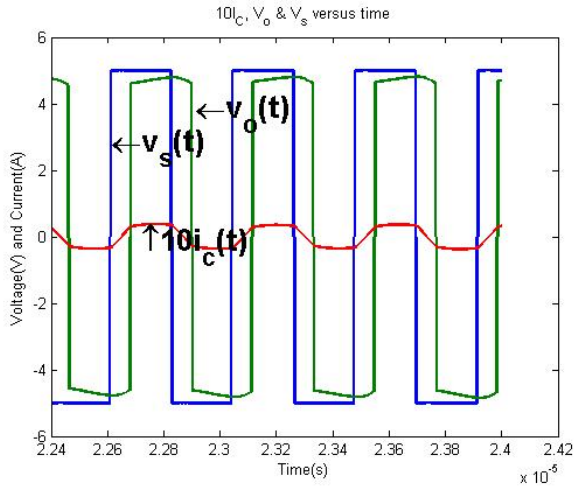

Fig. 6: $v_o(t)$, $v_s(t)$ and $10i_c(t)$ Steady State Simulation Results

III. Capacitive Data Communication Analysis

In this section, we discuss and analyze capacitive data communication through the power channel. The data communication circuitry is illustrated in Fig. 7.

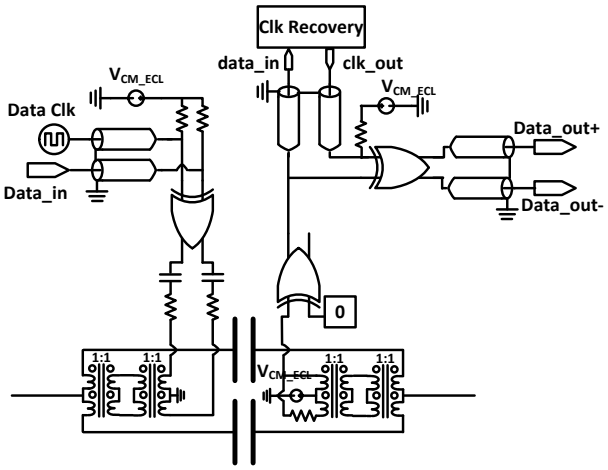

Fig. 7: Data Communication Circuitry

This circuitry is repeated again for the bottom half allowing data communication in the reverse direction. Data bits are streamed at 100Mb/s and then XORed with a 100MHz clock. This is done to implement manchester coding. The data transformer shown in Fig. 7 has two center tapped (1:1) transformers in series. Two transformers are used instead of one because one transformer is not adequent to reject the common mode voltage interference. One center tap is connected to a resonant inductor and the other center tap is connected to the digital ground. Manchester coding is necessary because the data transformer does not transmit DC voltage. Manchester coding effectly shifts the center of the data spectrum to 100MHz. On the receiver side, two (1:1) data transformers in are series connected in a similar fashion. One center tap is connected to a resonant inductor and the other tap is connected to the midrail of the XOR logic circuit. The transmitted voltage is sensed and buffered by a logic gate, implemented with a spare XOR gate. The clock recovery circuit extracts the 100MHz clock on the manchester coded data. Then both the manchester data and the extracted clock are XORed again to recover the original data.

A. Fundamental Analysis

The rest of the section analyzes the data channel. Fig. 8 shows the half circuit equivalent model from V_{dataIn} to $V_{dataOut}$. C_{bypass} is a large bypass capacitor which can be ignored. R is the series resistance in the network. L_{leak} is the leak inductance in the data transformer. C_P is the half-circuit parastic capacitance between the two bold capacitors in Fig. 7. L_M is the magnetizing inductance of the data transformer. With R_{load} selected to be large, the data channel is a bandpass system. Its low frequency corner is defined by C_{bypass} and L_M. Its high frequency corner is defined by $4L_{leak}$ and the network of capacitors C_p, C, and C_p as illustrated in Figure 8, and expressed in Eqn. 10.

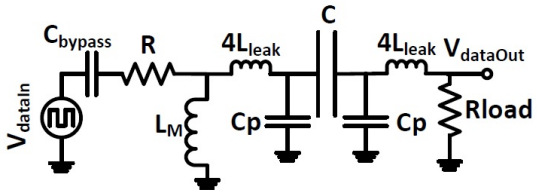

Fig. 8: Half Circuit Equivalent Model

The high frequency corner $f_{o,high}$ of the system is

$$f_{o,high} = \frac{1}{2\pi} \frac{1}{\sqrt{4L_{leak}C_p(1+\frac{C}{C+C_p})}} \tag{10}$$

With $L_{leak} = 5nH$, $C = 150pF$, and $Cp = 15pF$, $f_{o,high} =$ 210 MHz.

The low frequency corner $f_{o,low}$ of the system is

$$f_{o,low} = \frac{1}{2\pi} \frac{1}{\sqrt{L_M C_{bypass}}} \tag{11}$$

With $L_M = 0.1\mu H$ and $C_{bypass} = 1\mu F$, $f_{o,low} = 0.5MHz$

B. Simulations Results

Fig. 9. contains the data simulation results. In this graph, the eye diagrams of the input data and the output data are plotted. Bit 1 is indicated by an ideal square waveform with high voltage followed by low voltage. Bit 0 is indicated by an ideal square waveform with low voltage followed by a high voltage. Each bit is sent at a $10ns$ interval as shown in the time axis.

IV. Experimental Work

This section contains circuit parameters and experimental results of a capacitive power and data transfer prototype. This prototype has a geometry in size of the Iphone 5. An example design has specifications listed in Table I. Here a

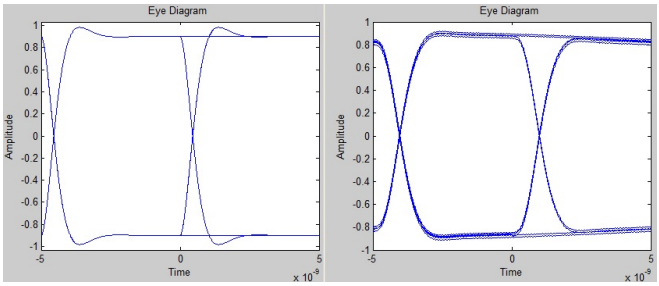

Fig. 9: $DataIn$ (Left) and $DataOut$ (Right) Eye Diagram Simulation Results

power train switching at 2.3MHz is able to deliver $1.25W$ of power over a total capacitor area of $52cm^2$. The switching frequency can be adjusted to take advantage of the unlicensed bands. This area of total capacitance is equivalent to $300pF$, separated into four capacitors, each part with $75pF$. Both the power supply voltage and the output voltage are $5V$. Furthermore, this experiment shows that the prototype is able to transfer $100Mbps$ bidirectional data. The experimental work is divided into two subsections. Subsection IV.A. contains the regulation of the output voltage. Subsection IV.B. contains the experimental work on data communication.

TABLE I: List of Important Experimental Parameters

Symbol	Description	Value
V_S	Supply Voltage	$5V$
V_O	Output Voltage	$5V$
f_s	H-bridge Switching Freq	$2.3MHz$
P_{out}	Output Power	$1.25W$
η	Power Efficiency	53%
M	Power Transformer Turn Ratio	10
$A_{cap,single}$	Area of Single Capacitor	$13cm^2$
$A_{cap,total}$	Area of Total Capacitor	$52cm^2$
C_{single}	Capacitance of Single Interface	$75pF$
C_{total}	Capacitance of Total Interface	$300pF$
L	Resonant Inductance Value	$35\mu H$
f_o	Resonant Frequency	$2.2MHz$
I_C	Capacitor AC Current Amplitude	$0.04A$
V_C	Capacitor AC Voltage Amplitude	$70V$
R_{load}	Load Resistor Value	20Ω
L_{leak}	Leakage Inductance	$5nH$
C_p	Parasitic Capacitance	$15pF$
R_{data}	2nd Order Low Pass Resistance	50Ω
$f_{o,data}$	2nd Order Low Pass Resonant Freq	$210MHz$
$Rate_{data}$	Data Rate	100Mb/s

A. Output Voltage Regulation

Here the regulation of output voltage is discussed. Regulation of output voltage is done by modulating the phase of $v_o(t)$ with respect to lowpass of $v_L(t)$, a representation of $i_c(t)$. When the output voltage is below $5V$, $v_o(t)$ will be delayed more with respect to $i_c(t)$ in order to increase output power. When the output voltage is below $5V$, $v_o(t)$ will be phase shifted less with respect to $i_c(t)$ in order to decrease output power. Fig. 10. shows the measured output voltage versus an additional capacitance added onto one of the capacitive interface. The capacitive interface nominally has a capacitance of $150pF$. Over the range of an additional $0pF$ to $200pF$, the phase control loop is able to regulate the output voltage close to $5V$. When the additional capacitance becomes $300pF$, the regulation is no longer effective. Fig. 11. shows the output voltage versus supply voltage V_S. The supply voltage is nominally at $5V$. Over the variations of $4.5V$ to $6V$, the output voltage is regulated to close to $5V$. When the supply voltage drops to $4V$, the phase control loop is no longer working adequately.

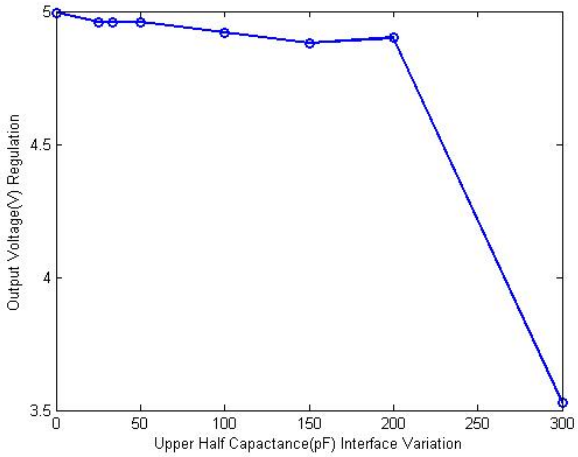

Fig. 10: Measured Output Voltage V_O Regulation vs Interface Capacitance Variations

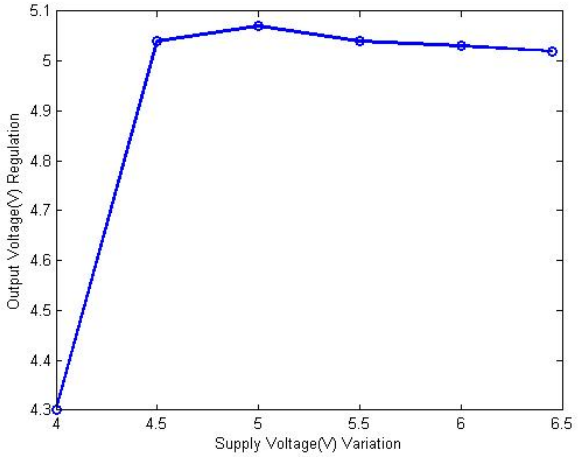

Fig. 11: Measured Output Voltage V_O Regulation vs V_S Variations

B. Data Transfer Experimental Results

This section contains the data transfer experimental results. Fig. 12. and Fig. 13. contain the eye diagrams of the input and output of the data channel when a 100Mb/s data is running through it while the power transfer is off and on. The output of the data channel becomes much noisier when the power

transfer is on in comparison with when it is off. In both cases, the output data shows enough voltage and timing margin for bit recovery.

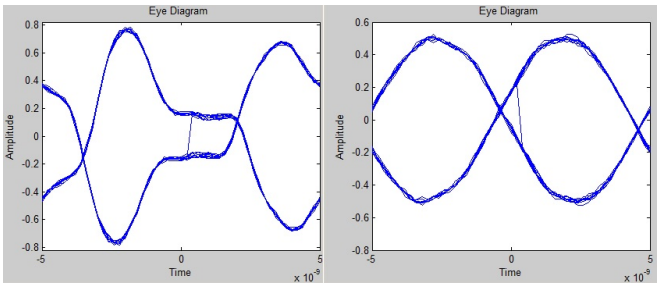

Fig. 12: Eye Diagram of 100Mb/s Data with no Power Transfer (Input on the Left; Output on the Right)

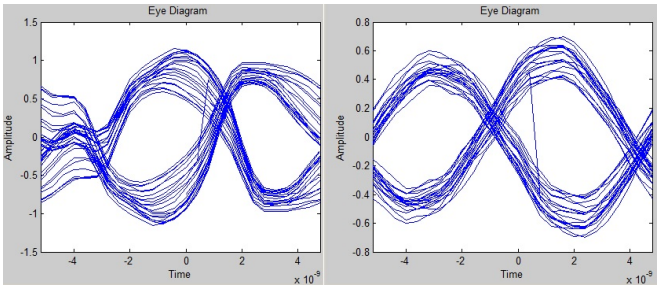

Fig. 13: Eye Diagram of 100Mb/s Data with Power Transfer (Input on the Left; Output on the Right)

V. Conclusion

This work presents a capacitive power and data transfer circuitry that delivers both power and data on the same channel. A prototype was designed and built to illustrate functionality. This prototype can interface with USB terminal with both the supply voltage and the output voltage being $5V$. It transfers 1.25W of power and has a power efficiency of 53%. Furthermore, a bidirectional data rate of 100Mb/s was illustrated. By building the circuitry on chip and allowing for equalization techniques, one can conceivably achieve higher efficiency with even higher data rate. This work extends the wireless charging technology by incorporating data into the power channel.

Acknowledgment

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