An Ultra-Low-Quiescent-Current Dual-Mode Digitally-Controlled Buck Converter IC for Cellular Phone Applications

by

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B.E. (Tsinghua University) 1997

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering-Electrical Engineering and Computer Science

in the

GRADUATE DIVISION

of the

UNIVERSITY of CALIFORNIA, BERKELEY

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Fall 2003

The dissertation of Jinwen Xiao is approved:

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University of California, Berkeley

Fall 2003

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Abstract

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This dissertation presents a low-quiescent-current dual-mode digitally-controlled buck converter IC for cellular phone applications. In cellular phones, the load current demanded by the on-board circuitry varies from below 0.1 mA up to a few hundred mA, reflecting operation in standby and active (talk) modes. Thus, high efficiency over a wide load range is of high priority for power management units, since the total energy is limited by the capacity of a single cell Li-ion battery. A dual-mode buck converter IC, implemented with a 0.25-μm CMOS process, takes 2 mm^2 active area and demonstrates equal or better regulation performance compared to state-of-the-art analog switchers. A very low quiescent current of 4 μA is achieved experimentally, resulting in a more than three-fold reduction compared to

the leading state-of-the-art analog controllers. Consequently, a high efficiency, exceeding 70%, is achieved over a wide load range between 0.1 and 400 mA.

Professor Seth R. Sanders
Dissertation Committee Chair

To my parents,

your love means the whole world to me.

Acknowledgements

First of all, I would like to express my gratitude to Professor Seth Sanders, for his patient guidance through my five years of graduate school life, for his unconditional support to my work, for his uncountable help in technical writing, and for being a wonderful role model. He is the most intelligent and unselfish person I have ever known, and I truly feel very fortunate to have had the opportunity to be his student.

Along with Professor Sanders, I would like to thank Professors Ali Niknejad, Borivoje Nikolic, and Paul Wright for serving on my qualifying exam committee. I would also like to thank Professors Sanders, Niknejad, and Wright for reading this thesis.

I would also like to thank my colleagues in Professor Sanders' group for their friendship and help over the years. Perry Tsao helped me many times on computer related problems with great patience. Angel Peterchev provided not only countless valuable technical discussions and ideas, but also shared his insight into art, and his talent for painting. Jianhui Zhang and his wife Rui Chen were a great couple to discuss any issue with. Artin Der Minassians, Matthew Senesky, Gabriel Eirea, and Wei Wang made 341 Cory Hall a fun place to work.

I greatly value the friendship and support from two other residents in 341 Cory Hall, Lixia Zhou and Jin Wang. Lixia always encouraged me when I was feeling down. She was also a very competitive company in swimming. Jin Wang helped me with valuable discussions in the area of communications and DSP, with incredible patience.

I also appreciate Tao Yang, a sincere friend since college, who provided important help

when I needed it most. Thanks to Zhanfeng Jia, Xiaotian Sun, and Jihua Huang, their friendship through the years made Berkeley a much more enjoyable place to live. I would also like to thank Weidong Cui, who helped me to gain so much insight about life. Mei Luo treated me with “Si Chuan Huo Guo” many times. Although most of the time the food was so spicy that I had to go home with a half-empty stomach, I am grateful for all the exciting conversations during the meals. Xinyan Deng is the most interesting friend I have ever known. It is unbelievable how much laugh we had together, we could have great fun even when watching the most boring movie “Northern Light”. Hanging out with her, I came to realize that there were so many beautiful things in the world that I did not notice before.

Special thanks to my parents Baozhu Xiao and Guifeng Zhao, and my brother Xiang Xiao and my sister-in-law Ling Pang, for their love and support. I could never made this far without it.

This work was supported by Linear Technology, Fairchild Semiconductor, National Semiconductor, and California Micro Program. The fabrication was performed by National Semiconductor.

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Chapter 1

Introduction

1.1 Motivation

This dissertation presents a low-quiescent-current dual-mode digitally-controlled buck converter IC for cellular phone applications. In cellular phones, the load current demanded by the on-board circuitry varies from below 0.1 mA up to a few hundred mA, reflecting operation in standby and active (talk) modes. Thus, high efficiency over a wide load range is of high priority for power management units, since the total energy is limited by the capacity of a single cell Li-ion battery. A dual-mode buck converter IC, implemented with a 0.25-μm CMOS process, takes 2 mm^2 active area and demonstrates equal or better regulation performance compared to state-of-the-art analog switchers. A very low quiescent current of 4 μA is achieved experimentally, resulting in a more than three-fold reduction compared to the leading state-of-the-art analog controllers. Consequently, a high efficiency, exceeding 70$\%$, is achieved over a wide load range between 0.1 and 400 mA.

In the evolution of modern portable electronic devices, digital data processing is taking an increasing role and a commensurate fraction of the power consumption. For example, in a second generation (2G) code division multiple access (CDMA) phone, the digital baseband and the memory circuit take about 10$\%$ of the total power that the handset chip set consumes. While in a third generation (3G) wide band CDMA (WCDMA) phone, this percentage is 30-50$\%$ of the overall power consumption, since functions associated with filtering and digital data streaming are now handled with digital circuitry. Thus, if the voltage regulator controller can be integrated on the same die with the digital system which it supplies, significant cost reduction can be expected. This digitally controlled buck con-

verter IC is implemented with a 0.25-μm CMOS N-well process, and demonstrates the possibility of integrating digitally controlled power management unit with its load circuit on a digital process.

1.2 Research Goals and Contributions

This work is the first effort to introduce digital control for a mass market power management application – cellular phones. The main contributions of this work are:

1. An ultra-low-quiescent-current dual-mode digitally-controlled buck converter IC is designed. The measured quiescent current in PFM mode is 4μA, which is a third of the leading state-of-the-art analog controllers [4]. Cellular phone standby time with each full charge of battery can be extended to up to three times, consequently.

2. An architecture employing internal power management is introduced to solve the conflict between the low voltage process and the high battery voltage in a cellular phone, enabling implementation of the digital controller in small feature size processes. A 0.25-μm CMOS N-well process is used to implement the chip, demonstrating that the power management unit can be implemented in a digital process. This also indicates the possibility to integrate the power management unit with other digital systems on the same die, which can result in significant cost reduction.

3. Dedicated analog and digital interface modules, particularly suited for dc-dc converter applications, are developed. A ring-oscillator based windowed-ADC (ring-ADC)

has the advantage of being nearly-entirely synthesizable, easily scalable and insensitive to switching noise. An ultra-low-power digital PWM (DPWM) module based on a ring-oscillator-MUX scheme (ring-MUX) is also developed.

1.3 Thesis Organization

An overview on DC-DC converters is offered in Chapter 2. Design challenges for portable applications are briefly discussed, and opportunities for digital control are presented.

Chapter 3 outlines system design issues relating to buck converters. Basics of continuous conduction and discontinuous conduction modes are reviewed as background information. The power train and output filter design is briefly discussed at the end of this chapter.

Chapter 4 addresses the architecture of the dual-mode buck converter IC. The PFM controller's quiescent power is the fundamental limitation on light-load efficiency when the cellular phone is in standby mode, and the details of the low-quiescent-current PFM controller are presented, followed by discussions on design of zero-DC-current comparators. Internal power management is presented as a solution to achieve voltage compatibility.

The analog to digital converter (ADC) and the digital PWM (DPWM) are used to provide the analog and digital interface between the digital compensation network and the buck converter. A general purpose interface element can be unnecessarily expensive in

terms of power consumption and chip area, thus the design of power and area efficient interface elements becomes the key challenge of making a high performance low power digital controller. A ring-ADC that is almost entirely synthesizable is presented in Chapter 5. And, a very low power ring-MUX DPWM is described in Chapter 6. A discussion on an alternative DPWM structure based on a counter-comparator scheme is also given in Chapter 6.

Ring oscillators are used in both analog and digital interface elements. Ideally more than one oscillation pattern can appear in a ring oscillator depending on initial conditions. However, only the fundamental pattern with one transition edge is observed in experiments. A hypothesis explaining the global stability of the fundamental pattern in ring oscillators is proposed in Chapter.7.

A test IC is built with a 0.25-μm standard CMOS N-well process, and 4μA quiescent current is achieved experimentally in PFM mode. More experimental results are presented and conclusions are drawn in Chapter 8.

Chapter 2

Overview of DC-DC Converters for Cellular Phone Applications

2.1 Overview of DC-DC Converters for Portable Applications

2.1.1 Increasing Battery run-time with voltage regulators

For battery operated devices, inserting a voltage regulator between the battery and the CMOS digital circuits or switch-capacitor-based mixed-signal circuits significantly enhances battery run time. This is true even when using regulators with relatively low efficiency. This can be explained with the following example.

Assume a cell phone handset has 50% power dissipated in digital circuitry when the battery is fully charged, and the other 50% is dissipated in analog circuitry which has a supply-independent bias current. A single cell Li-Ion battery is used which has a maximum fully charged voltage V_{max} of 4.2 V, and an end-of-charge voltage V_{min} of 3.6 V. The digital circuit is clocked at frequency f to meet the throughput requirement. Assume the minimum supply voltage to meet the throughput requirement is 1.8 V. Thus, the dynamic loss of the digital circuit can be modeled by a equivalent resistance of value

$$R_{eff} = \frac{1}{fC} \tag{2.1}$$

where the C is the total effective switching capacitance. The power consumption in the digital circuitry P_d and current consumption I_d is given by

$$P_d = fCV^2, \tag{2.2}$$

$$I_d = \frac{P_d}{V} = fCV, \tag{2.3}$$

where V is the supply voltage to the mixed-signal circuit. The analog circuit can be modeled by a load with constant current load I_a, thus the power consumed in the analog session is

$$P_a = I_a V. \tag{2.4}$$

If the analog and the digital power consumptions balance at $V = V_{max}$, from equation (2.2) and (2.4), I_a can be written as

$$I_a = fCV_{max}. \tag{2.5}$$

For the present, neglect the supply voltage compatibility of the digital circuit and assume the circuit runs directly from the battery without hardware damage. Then the total power drawn from the battery when the battery voltage is V_{batt} is

$$P_{batt} = P_a(V_{batt}) + P_d(V_{batt}) = fC(V_{batt} + V_{max})V_{batt}. \tag{2.6}$$

Assume a linear regulator is inserted between the battery and the digital circuit, and the output voltage of the regulator V_o is 1.8V. The efficiency of the linear regulator η_{lin} is approximately $\frac{V_o}{V_{batt}}$. The power delivered from the battery is

$$P_{Lin} = (P_d(V_o) + P_a(V_o))/\eta_{lin} = fC(V_o + V_{max})V_{batt}. \tag{2.7}$$

By comparing (2.6) and (2.7), power saving by having a linear regulator can be calculated. Consider the battery discharge range between 4.2 V and 3.6 V. When the battery is fully charged, a overall power saving of 28.6% is achieved. When the battery is at end-of-charge, the overall power saving is 12.5%.

A linear regulator is relatively simple to implement. However, the major draw back is that the efficiency scales roughly with the ratio of output voltage and input voltage. As technology development pushes digital circuitry to be implemented with processes with feature size 0.18-μm and below, the allowable supply voltage also drops. The efficiency limit of the linear regulator becomes a more serious problem. Replacing a linear regulator with switching regulator for better efficiency is necessary in many cases.

If a switching regulator is inserted between the battery and the load circuit, the power saving is more significant. Assume a 90% efficiency of the switching regulator, the power drawn from the battery is then

$$P = (P_d + P_a)/0.9 = 1.11fC(V_o + V_{max})V_o. \tag{2.8}$$

The overall power saving is 66$\%$ in the fully charged battery state and 57.3$\%$ in the minimum charged state. More detailed analysis on run time enhancement is given in [5].

Besides the main task of improving battery life, inserting regulators also helps to isolate different circuit blocks that might potentially disturb each other via supply lines. The power amplifiers in cellular phones draw large pulse current and can cause a battery voltage excursion of up to 0.5 V due to inductive effects and equivalent series resistance (ESR) of the battery. The power supply rejection ratio of the voltage regulator significantly reduces the supply transient seen by the phone circuits [6].

2.1.2 Design Challenges for Portable Applications

For portable devices such as cellular phones, all of the energy is drawn from the limited source of a battery. The load current of the voltage regulator in a cellular phone may vary from hundreds of mA in run time to below 0.1 mA in standby time. To extend both system run time and standby time, given the same power dissipation in the baseband and RF circuit, the efficiency of the voltage regulators must be increased. Switching regulators operated in pulse width modulation (PWM) mode are preferred to linear regulators for run time. The PWM controller runs the DC-DC converter in continuous conduction mode, and high regulation quality as well as high efficiency can be achieved at high load. Cellular phone systems may stay in standby mode for most of the total operation time, and the load current in standby mode is very low. As shown later in Chapter 3, when the load becomes light, the PWM mode leads to poor efficiency due to excessive switching loss. Instead, pulse frequency modulation (PFM) can be used to achieve high efficiency at light load. In PFM mode, the converter runs in discontinuous conduction mode, and the switching frequency is proportional to the load current, resulting in reduced switching activity at light load. Most loss components of the PFM mode converter, except the quiescent power of the controller, scale roughly with the load current when the load is very light. Thus, the PFM controller quiescent power becomes the limiting factor on light load efficiency. Therefore, the design of an ultra-low quiescent current PFM control mode is the most challenging objective in cellular phone applications.

2.2 Digital Control for DC-DC Converters

Digital control is gaining increasing popularity as a candidate for DC-DC converters due to many advantages over analog control [7]–[14]. With most data processing done in the digital domain, digital controllers are insensitive to noise and parameter variations that might lead to inaccuracies in analog circuits. Powerful computation capability makes digital control ideal for advanced control schemes such as adaptive control and on-line self-optimizing control which improve converter performance. Digital controllers can directly communicate with other digital function blocks and feedforward can be easily implemented which makes the controller respond faster and enables the converters to have smaller output capacitors. In fact, in some applications the controller can be embedded on the same die as the system processor whose voltage it regulate. Technology scaling enhances the already vast signal processing capability of digital controllers with faster speed and lower power consumption, while it does little for the analog counterpart. Furthermore, the design automation of digital controllers is well supported by available synthesis and layout tools, and migrating an existing design to a different process needs much less modification than in the analog approach.

Chapter 3

System Design of Controller IC for Cellular Phone Applications

3.1 Overview of Buck Converter Operation

3.1.1 Basics of Buck Converter

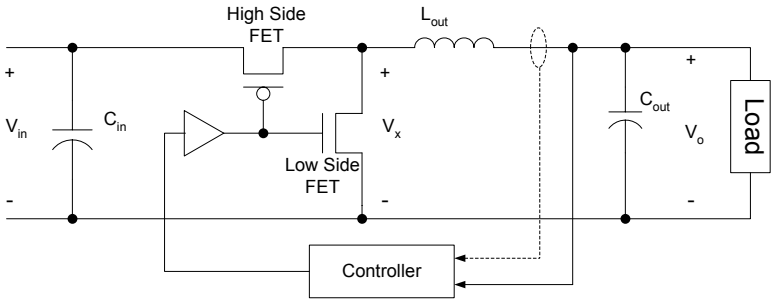
A buck converter is also called a step-down converter, which produces a lower average output voltage V_o than the DC input voltage V_{in}. Fig. 3.1(a) shows a synchronous buck converter system. Both the high side and the low side switching devices are implemented with FETs in a synchronous converter. The input voltage from the battery gets chopped by the power switches and the average input voltage is thus reduced. Assuming ideal switches, the chopped voltage V_x at the switching node is a square wave with duty ratio $D = t_{on}/T_s$ as shown in Fig. 3.1(b). A second order LC low pass filter is used to pass the DC component of V_x while attenuating the AC component to an acceptable ripple voltage. Neglecting the loss in the converter, the DC output voltage V_o is given by [15]

$$V_o = V_{in} \cdot D. \tag{3.1}$$

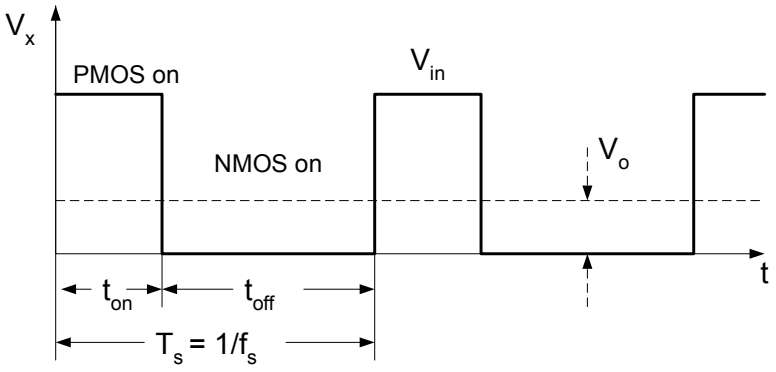
By varying D, V_o can be controlled. The corner frequency f_c of the LC filter is chosen to be much lower than the switching frequency f_s so that the output voltage ripple is small.

3.1.2 Continuous Conduction Mode

If the inductor current remains positive, or is allowed to reverse by the high-side and the low-side switches, the dc-dc converter is said to operate in continuous conduction mode. A converter in continuous conduction mode is shown in Fig. 3.2(a), and switching node voltage V_x, inductor current I_L and output current I_o are shown in Fig. 3.2(b). The inductor



(a)



(b)

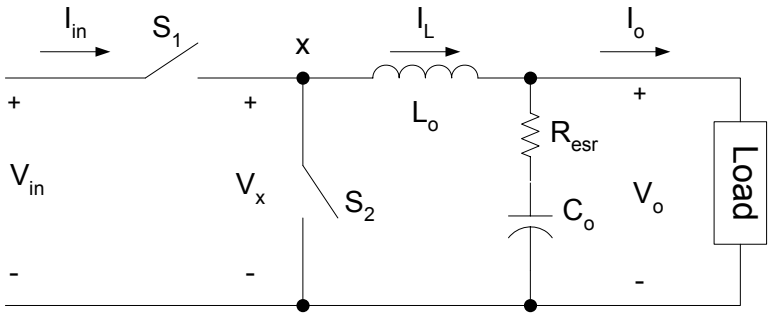
Figure 3.1: (a) Buck converter schematic, (b) switching node voltage waveform V_x at steady-state.

current ripple ΔI_L is give by [15]

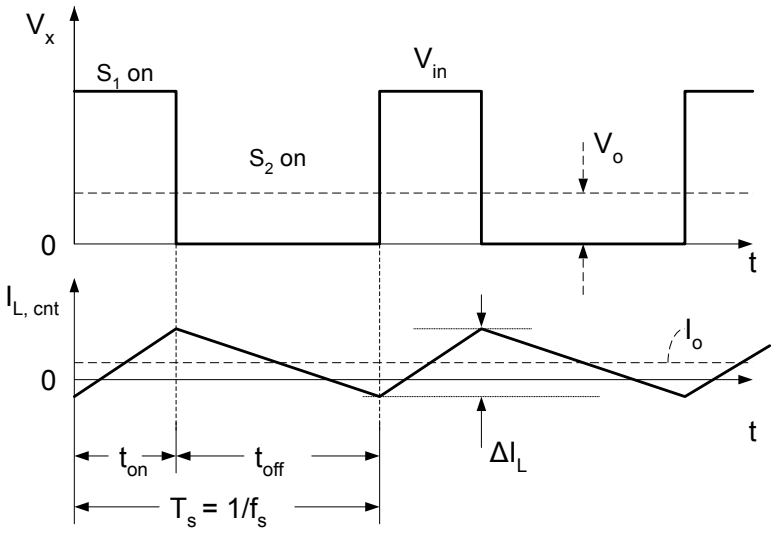
$$\Delta I_L = \frac{V_o \cdot t_{off}}{L_o} = \frac{V_o}{L_o} \cdot (1 - D) \cdot T_s, \tag{3.2}$$

where T_s is the switching period.

In steady-state, the average output voltage is given by (3.1), and the output current I_o equals the DC component of inductor current I_L. When I_o is greater than $\Delta I_L/2$, the inductor current remains positive during the entire cycle. When I_o is less than $\Delta I_L/2$, the



(a)



(b)

Figure 3.2: (a) Synchronous converter, (b) voltage and current waveforms in continuous conduction mode.

inductor current becomes negative momentarily in the switching cycle, which corresponds to the converter discharging the output capacitor C_o through the inductor. As long as I_L flows continuously, the converter is considered to be in continuous conduction mode.

There are two ripple components in the output voltage, due to output capacitor C_o and its equivalent series resistance (ESR) R_{ESR} respectively. Let R_{ESR} be zero for now, the output voltage ripple ΔV_o can be calculated by estimating the total charge accumulated on C_o when I_L is higher than I_o.

$$\Delta V_o = \frac{\Delta Q}{C_o} = \frac{1}{2}\frac{\Delta I_L}{2}\frac{T_s}{2}\frac{1}{C_o} = \frac{1}{8}\frac{\Delta I_L \cdot T_s}{C_o}. \tag{3.3}$$

Substituting ΔI_L from equation (3.2) yields

$$\Delta V_o = \frac{1}{8} V_o \cdot (1-D)\frac{T_s^2}{L_o C_o}. \tag{3.4}$$

Since switching frequency $f_s = 1/T_s$, and LC filter cut-off frequency f_c is $f_c = \frac{1}{2\pi\sqrt{L_o C_o}}$, $\Delta V_o / V_o$ can be expressed as

$$\frac{\Delta V_o}{V_o} = \frac{\pi^2}{2}(1-D)\frac{f_c^2}{f_s^2}. \tag{3.5}$$

Equation (3.5) shows that the output voltage ripple can be reduced by selecting the LC cut-off frequency f_c to be much lower than the switching frequency f_s of the converter.

With non-zero R_{ESR}, the output voltage ripple is higher than with zero R_{ESR}. It can be shown that, assuming the ripple current is piecewise linear, for $D < 50\%$, the voltage

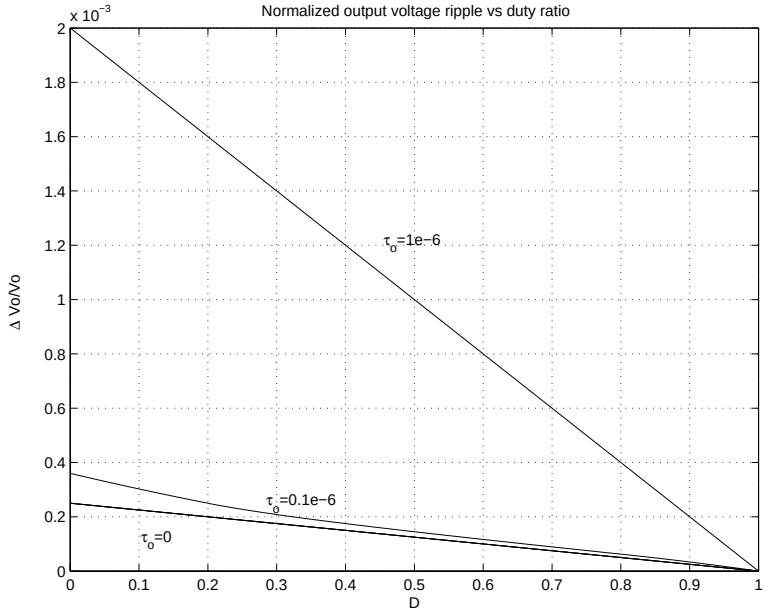


Figure 3.3: Converter output voltage ripple with different output capacitor time constant values.

ripple ΔV_o is

$$\Delta V_o = \begin{cases} \frac{\Delta I_L T}{8C} + \Delta I_L R \frac{\tau_o}{2T}(\frac{1}{1-D} + \frac{1}{D}) & \text{for} \quad \tau_o \leq \frac{1}{2}DT, \\ \frac{\Delta I_L}{8C}(1-D)T + \Delta I_L R \frac{\tau_o}{2(1-D)T} + \frac{\Delta I_L}{2}R & \text{for} \quad \frac{1}{2}DT < \tau_o \leq \frac{1}{2}(1-D)T, \\ \Delta I_L R & \text{for} \quad \tau_o > \frac{1}{2}(1-D)T; \end{cases} \tag{3.6}$$

and for $D \geq 50\%$

$$\Delta V_o = \begin{cases} \frac{\Delta I_L T}{8C} + \Delta I_L R \frac{\tau_o}{2T}(\frac{1}{1-D} + \frac{1}{D}) & \text{for} \quad \tau_o \leq \frac{1}{2}(1-D)T, \\ \frac{\Delta I_L}{8C}DT + \Delta I_L R \frac{\tau_o}{2DT} + \frac{\Delta I_L}{2}R & \text{for} \quad \frac{1}{2}(1-D)T < \tau_o \leq \frac{1}{2}DT, \\ \Delta I_L R & \text{for} \quad \tau_o > \frac{1}{2}DT, \end{cases} \tag{3.7}$$

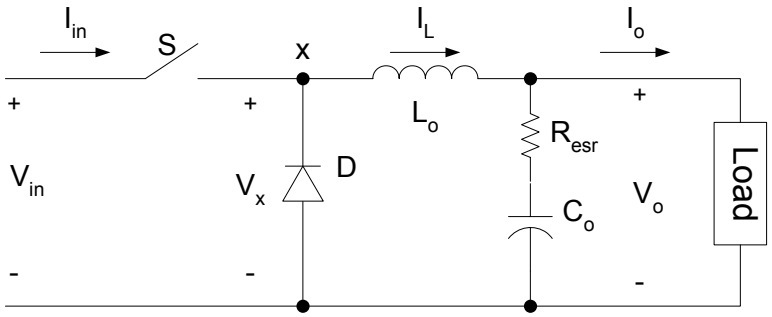
where τ_o is the time constant of output capacitor defined as $\tau_o = RC$. The derivation

and verification of this equation is in Appendix.A. For a given capacitor technology, τ_o is approximately a constant for various capacitance values. For example, the time constant is usually in the range of 0.1 to a few μs for ceramic capacitors, and 1 to 10 μs for tantalum capacitors. Fig. 3.3 shows the plots of normalized output voltage ripple as a function of steady-state duty ratio, corresponding to different output capacitor time constant values. It can be noticed that smaller output voltage ripple can be achieved by choosing output capacitors with lower time constant values.

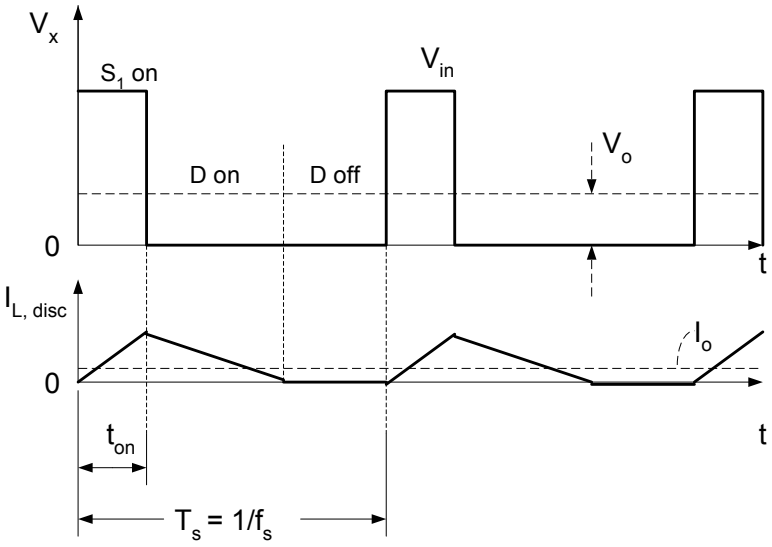
3.1.3 Discontinuous Conduction Mode

Replacing the low side switch S_2 in the synchronous converter with a diode D results in a conventional buck converter as shown in Fig. 3.4. When output current I_o is higher than $\Delta I_L/2$, the inductor current flows continuously and the converter still works in continuous conduction mode, with V_o satisfying (3.1). When I_o is lower than $\Delta I_L/2$, the diode conducts while the inductor current decreases. The inductor discharges stored energy to the output capacitor until the current drops to zero. The diode then blocks the reverse current and the inductor current remains zero until the next switching cycle. This operation mode is called discontinuous conduction mode because the inductor current is identically zero for finite intervals.

In discontinuous conduction mode, the output voltage of the converter V_o does not



(a)



(b)

Figure 3.4: (a) Schematic of a conventional buck converter, (b) switching node voltage and inductor current waveforms in discontinuous conduction mode.

satisfies (3.1). Instead, the new expression of D is given by [15]

$$D = \frac{V_o}{V_{in}} \sqrt{\frac{I_o / I_{LB,max}}{1 - V_o/V_{in}}}. \tag{3.8}$$

where $I_{LB,max}$ is the maximum value of average inductor current at the edge of continuous conduction mode I_{LB} if V_o is constant:

$$I_{LB,max} = \frac{T_s V_o}{2L} \tag{3.9}$$

3.2 PWM Mode Power Loss Analysis

Dc-dc converter losses include conduction loss, switching loss, controller quiescent power, inductor core loss, stray inductance loss, etc. Conduction loss and switching loss are usually significant in PWM mode. Assume the input voltage is V_{in}, the output voltage is V_o, and the output current is I_o. Let D be the steady state duty ratio, and f_s be the switching frequency of the converter, the different loss components are elaborated below.

3.2.1 Conduction Loss

The conduction loss is mainly due to the finite on-resistance of the high side and the low side switches, denoted by $R_{dson,h}$ and $R_{dson,l}$ respectively, and the series resistance of the output inductor R_L.

Let R_{dson} be the equivalent on-resistance of the power switches seen by the inductor current, it can be given by the sum of the on-resistance of the power switches, weighed by

conduction time:

$$R_{dson} = R_{dson,h}D + R_{dson,l}(1 - D). \tag{3.10}$$

In steady state, the average inductor current equals the load current I_o. Assume the inductor current ripple is small compared to the average inductor current, the conduction loss can then given by

$$P_{hl} = (R_{dson} + R_L)I_o^2. \tag{3.11}$$

To avoid the shoot through current between the high side and the low side switches, deadtime must be inserted in the PWM signals that controls the two switches, to make sure the two switches are not on simultaneously. During the deadtime, both power switches are off, and the continuous flow of inductor current is relying on the body diodes of the switches. Assume the voltage drop across the diode junction is 0.7 V when the diode is on, the conduction loss on the diode , denoted by P_D, is

$$P_D = \frac{0.7I_o t_{deadtime}}{T_s} \tag{3.12}$$

where $t_{deadtime}$ is the total deadtime in one switching cycle. If the deadtime is designed properly, the conduction loss from the diode should also be small compared to P_{hl}.

3.2.2 Switching Loss

The power switches conduct momentarily in saturation mode during the turn-on and turn-off transient. The high voltage across the power device and the inductor current that flows through it can cause significant loss. This is often referred to as hard switching. The

switching loss in a dc-dc converter is mainly the loss due to hard switching, and the loss in gate drives.

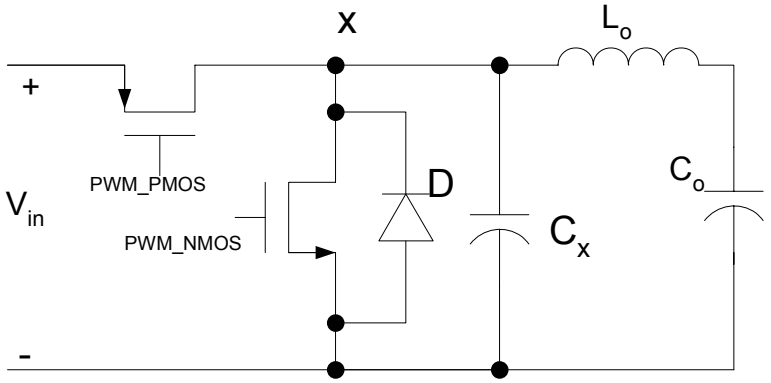
Hard Switching Loss

The loss due to hard switching is associated with the parasitic capacitor C_x lumped at the switching node, as shown in Fig. 3.5(a). The capacitor C_x is composed of the junction capacitance of each power switch, and the parasitic capacitance from the package, the inductor and PCB trace. Idealized transient waveforms of the drain current I_d and the drain-source voltage V_{ds} of the high side PMOS is shown in Fig. 3.5(b). The simulated turn-on and turn-off transient waveforms of the same switch is given in Fig. 3.6. For simplicity, in the analysis here, the inductor current ripple is neglected and thus $I_L = I_o$ in steady state. The finite on-resistance of the power switches are also ignored.

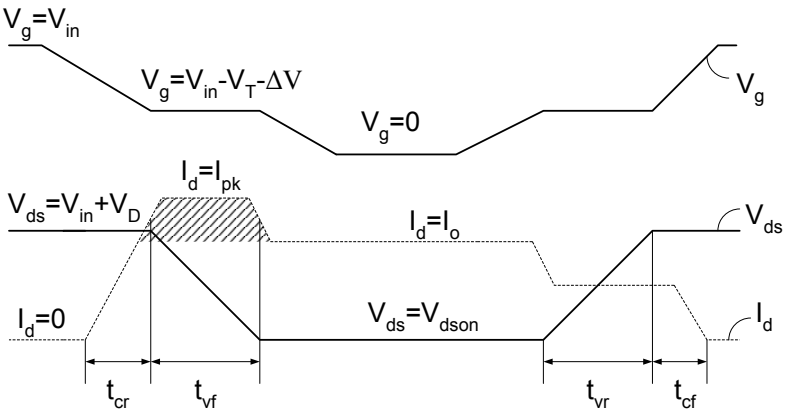
During the deadtime before the PMOS is on, the inductor current shifts to the body diode of low side switch, V_{ds} of PMOS equals V_{in}. When V_g drops to approximately one threshold below the input voltage, the PMOS starts to turn on, the inductor current starts to shift to the high side switch. Drain-source voltage V_{ds} remains equal to V_{in} until I_d is close to I_o, because of the exponential relation between diode voltage and current. Gate drive current I_G charges the miller capacitor $C_m = C_{gd}(1 - A)$, where A is the small signal gain of the PMOS. The large miller capacitor forces gate voltage to plateau at

$$V_g = V_{in} - V_t - \Delta V, \tag{3.13}$$

where V_t is the PMOS threshold voltage.

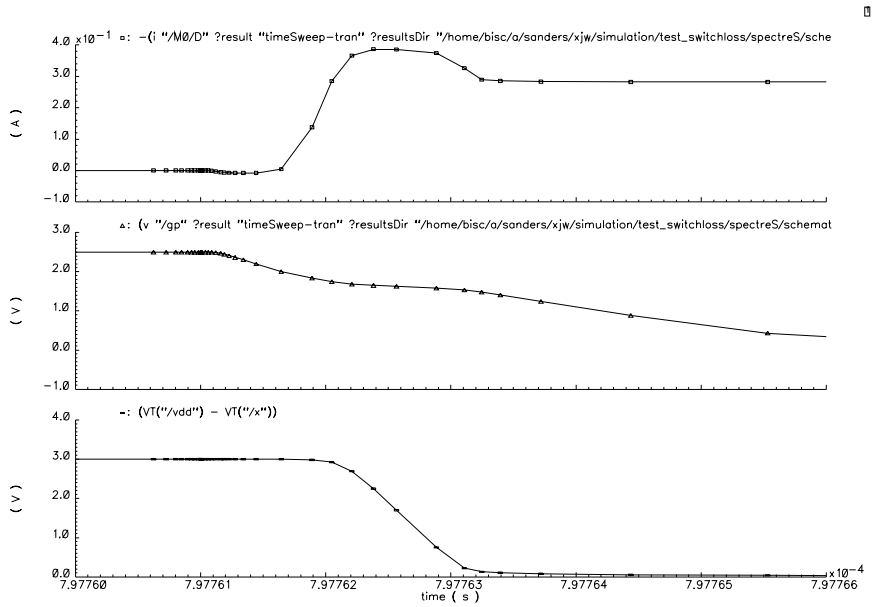


(a)

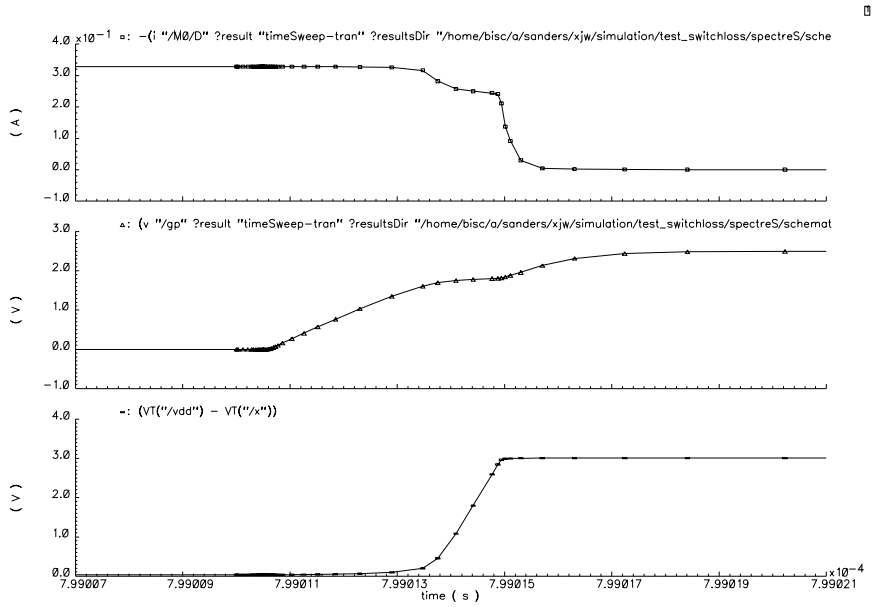


(b)

Figure 3.5: (a)Schematic of buck converter with parasitic capacitor C_x at the switching node, (b)hard switching transient waveforms in PMOS.



(a)



(b)

Figure 3.6: Simulated transient waveforms of PMOS, the top curve being I_d, middle curve $-V_g$, bottom curve $-V_{ds}$ in each sub-figure (a) turning-on transient, (b) turning-off transient.

The drain current I_d continues to increase to the peak value I_{pk}. The current difference $I_{pk} - I_o$ charges up C_x, and V_{ds} of the PMOS decreases until $V_{ds} = 0$. The PMOS enters the linear region and the miller transient has passed. The gate voltage continues to ramp up to V_{in}, the voltage V_x across the capacitor C_x settles to V_{in}, and I_d falls back to I_o, at the end of the transient. The turn-off transient is analogous.

The total charge accumulated on C_x during the turn-on transient can be calculated by integrating the I_d waveform in the shaded area in Fig. 3.5(b). Since the PMOS is in the saturation region during most of the transient, its gate-drain capacitor C_{gd} is just the gate-diffusion overlap capacitor, thus C_x is much greater than C_{gd}. Let Q_x be the charge stored on C_x at the end of turn-on transient. Define I_{C_x} to be the current exceeding I_o to charge the switching node, it can then be calculated as

$$I_{C_x} = I_{pk} - I_o = \frac{Q_x}{t_{vf}} = \frac{C_x V_{in}}{t_{vf}}, \tag{3.14}$$

where t_{vf} is the V_{ds} falling time, as shown in Fig. 3.5(b). The total energy dissipated in the PMOS during the turn-on transient can be calculated as

$$\begin{aligned} E_{t,on} &= \frac{1}{2}(I_o + I_{C_x})V_{in}t_{cr} + \frac{1}{2}V_{in}(I_o + I_{C_x})t_{vf} \\ &= \frac{1}{2}V_{in}(I_o + I_{C_x})(t_{cr} + t_{vf}). \end{aligned} \tag{3.15}$$

The energy stored on C_x is transfered to the output during the NMOS turn-on transient, and shall not be counted as loss. Thus the switching loss at turning-on transient of the PMOS is

$$P_{sw,on} = \frac{E_{t,on}}{T_s} = \frac{V_{in}(I_o + I_{C_x})(t_{cr} + t_{vf})}{2T_s}. \tag{3.16}$$

Similarly, the loss at the turning-off transient of the PMOS $P_{sw,off}$ can be calculated as

$$P_{sw,off} = \frac{V_{in}(I_o - I_{C_x})(t_{vr} + t_{cf})}{2T_s} \tag{3.17}$$

The switching loss in the PMOS $P_{sw,p}$ can be calculated by summing (3.16) and (3.17). Assume the turn-on and turn-off times are equal, one obtains

$$P_{sw,p} = \frac{V_{in}I_o(t_{vr} + t_{cf})}{T_s} \tag{3.18}$$

The switching transient time is mainly decided by the speed of the gate driver to charge the miller capacitor. A stronger gate driver results in a faster turn-on and off transient, hence lower switching loss. However, when the turn-off of the high side PMOS is too fast, the low side NMOS might turn on to some extent due to capacitive coupling to the NMOS gate. In many cases it may be necessary to design the high side gate driver weaker in pulling down the PMOS gate voltage for a slower PMOS turn-on transient. A strong pull down transistor in the low side gate driver may also be helpful to alleviate the NMOS gate voltage variation during turn-off transient of the PMOS.

As mentioned earlier, to avoid the momentary shoot-through current when both the PMOS and the NMOS are on, a deadtime is usually inserted between the control signals of the two power switches. If the deadtime is designed properly, the drain-source voltage of the NMOS is zero while the NMOS is turned on, resulting in zero loss. This is often referred to as the soft switching.

Gate Drive Loss

The power dissipation in the gate drives is mostly dynamic power used to charge and discharge parasitic capacitors of the power switches. Two processes are important in understanding this kind of loss: the charging of gate-source capacitor C_{GS}, and charging of the miller capacitor C_{GD}. The charge accumulated on C_{gs} when the transistors turn on is

$$Q_{GS} = (\Delta V_{GS})C_{GS}, \tag{3.19}$$

and the charge delivered to the miller capacitor is

$$Q_m = (\Delta V_{GD})C_{GD}, \tag{3.20}$$

where ΔV_{GS} and ΔV_{GD} are the gate-source and gate-drain voltage change respectively during turning-on transient. Thus, $\Delta V_{GS} = V_{in}$, and $\Delta V_{GD} = 2V_{in}$. Therefore, the gate drive power loss can be given by

$$P_g = f_s(Q_{GS} + Q_{GD})V_{in} = f_s(C_{GS} + 2C_{GD})V_{in}^2 \tag{3.21}$$

The loss in gate drives is usually smaller than the hard switch loss when the load current is high. However, the hard switch loss has dependency on the load current. The gate drive loss, on the other hand, is independent of load current. Thus, the gate drive loss can become the dominant component in switching loss when the load is light.

3.2.3 Stray Inductance Loss

The stray inductance L_s in the loop formed by input decoupling capacitor and power switches has a power dissipation that equals to [5]

$$P_{Ls} = \frac{1}{2T_s} L_s I_{max}^2, \tag{3.22}$$

where I_{max} is the maximum inductor current.

The value of L_s depends on the PCB layout, packaging, etc and can be reduced by minimizing the loop that contains the high current.

3.2.4 Controller Quiescent Power

The equivalent bias power the controller of the dc-dc converter dissipates is called controller quiescent power. Typically, the quiescent power of the PWM controller is much lower than the sum of the switching and the conduction losses of the converter in continuous conduction mode.

3.2.5 PWM Mode Efficiency

Considering only the conduction loss P_c, the switching loss P_s, and the controller quiescent power P_q, the efficiency η of a dc-dc buck converter in PWM mode can be given by

$$\eta = \frac{P_o}{P_o + P_s + P_c + P_q}. \tag{3.23}$$

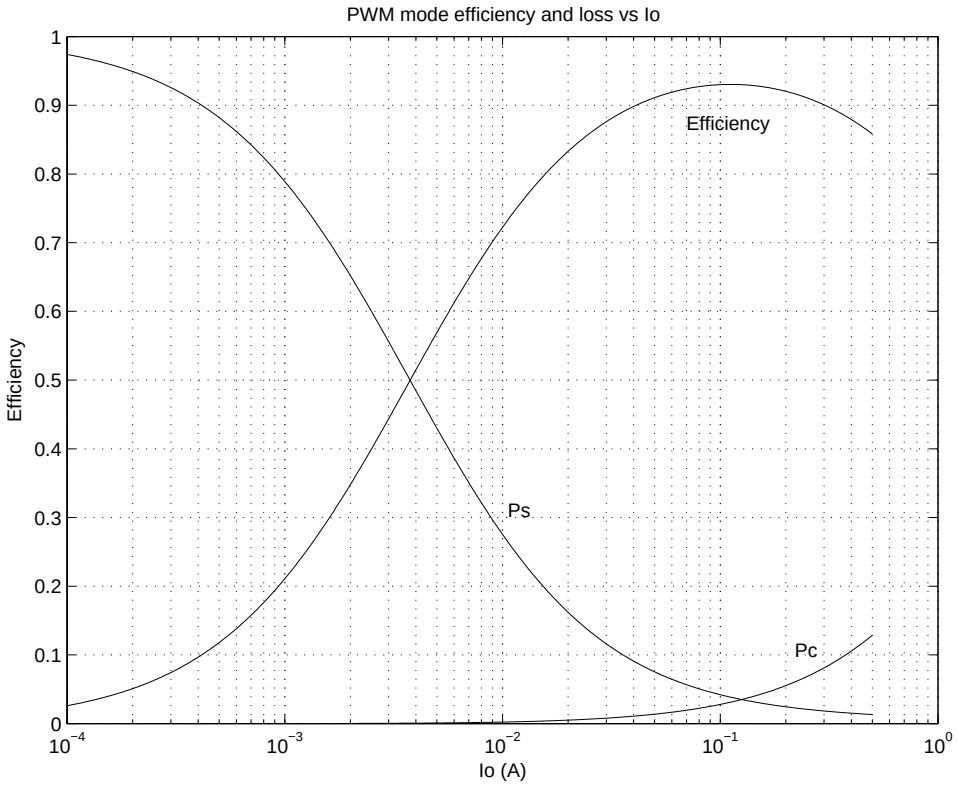


Figure 3.7: Efficiency and loss versus I_o, switching loss P_s and conduction loss P_c is each normalized to input power.

An efficiency curve of a dc-dc converter is plotted in Fig. 3.7. The normalized switching and conduction losses, P_s/P_{in} and P_c/P_{in} respectively, are also given. The corresponding input voltage is 4.5 V and output voltage is 1.5 V. It shows that the converter efficiency is higher than 80$\%$ when the load is higher than 14 mA, and it bends down significantly at light load ($I_o < 1mA$) due to the increasing portion of switching loss in the total input power.

For cellular phone applications, the system works in the standby mode most of its operation time. The load current is very low when the phone is in standby mode. If the voltage regulator continues to operate in PWM mode when the load is light, the efficiency of the

regulator will be poor. To extend the standby time a cellular phone can sustain with each full charge of the battery, the efficiency of the dc-dc converter has to be improved in light load conditions. For this reason, the controller is switched to pulse frequency modulation (PFM) mode control for light load operation.

3.3 PFM Mode Power Loss Analysis

The PFM mode runs the buck converter in discontinuous conduction mode. The switching frequency of the converter scales with the load current. At very light load, the switching activity is greatly reduced, resulting in significant switching loss reduction.

Fixed-on-time control is implemented in the PFM mode in this work. The output voltage is sampled at a fixed frequency, so that when it is detected to be lower than the reference, the PFM controller generates a fixed-on-time pulse to charge the output node. Then the converter is idle until a low V_o is detected again. The PFM mode waveforms of sampling clock, PWM signal, inductor current and output voltage are shown in Fig. 3.8.

Let V_{in} and V_o be the input and output voltage respectively, I_o be the load current and ΔI_L be the peak inductor current. Assume the fixed on-time is t_{on}. Assume the load current is very low. The total charge Q transfered to the output node in each switching cycle can be estimated by integrating the inductor current in one switching cycle, which results in

$$Q = \frac{\Delta I_L}{2} t_{on} \frac{V_{in}}{V_o}. \tag{3.24}$$

Neglecting the jitter due to discrete sampling of V_o, the switching frequency f_s at load I_o

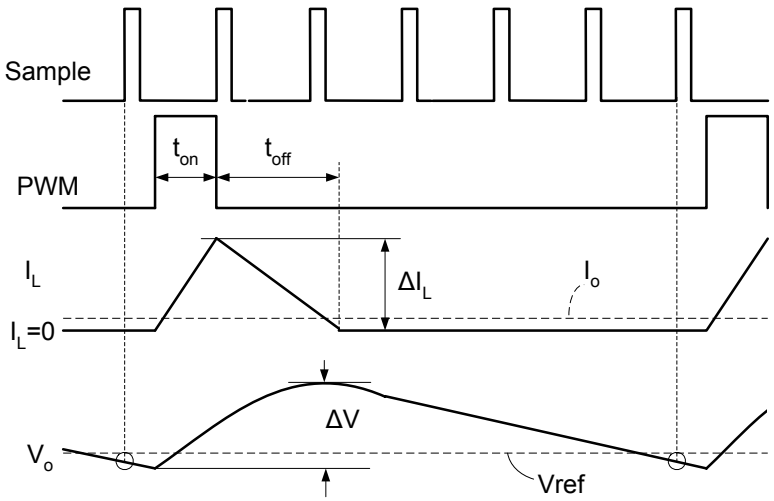


Figure 3.8: Voltage and current waveforms in buck converter in PFM mode.

can be approximated by

$$f_s \approx \frac{I_o}{Q} = \frac{2I_o}{\Delta I_L} \frac{1}{t_{on}\frac{V_{in}}{V_o}}. \tag{3.25}$$

Therefore the switching frequency at PFM mode is roughly proportional to the load current.

3.3.1 Conduction Loss, Switching Loss, and Stray Inductive Switching Loss in PFM Mode

The time during which the inductor current is non-zero is $t_{on} + t_{off}$, which equals to $t_{on}V_{in}/V_o$. In steady state, the conduction loss in PFM can be written as

$$P_c = f_s R \int_0^{t_{on}\frac{V_{in}}{V_o}} I_L(t)^2 \, \mathrm{d}t. \tag{3.26}$$

where R is the equivalent total series resistance. Similarly, switching loss and stray inductance loss in PFM mode is the total energy dissipated each switching cycle times the switch-

ing frequency. Therefore, in PFM mode, conduction loss, gate drive loss, hard switching loss and stray inductance loss are all proportional to the switching frequency and hence load current.

3.3.2 PFM Controller Quiescent Power

The PFM controller quiescent power is the equivalent static power of the controller and thus is independent of the load current. When the load is very light, all the other kinds of loss scale with the load current, and controller quiescent power becomes the dominant limiting factor on the efficiency of the PFM mode converter. Therefore, low controller quiescent power is essential to achieve high efficiency at very light load.

3.4 DC-DC Converter System Design

3.4.1 Digital Controller System Specifications

Some of the main specifications of the buck converter for cellular phone and hand-held ratio applications are listed in Table.3.1.

3.4.2 Output Filter Design

The output filter in a buck converter is typically a second order LC filter. As shown by equations (3.5), (3.6) and (3.7), the output voltage ripple could be capacitance dominated, equivalent series resistance (ESR) dominated, or have significant components due to each.

Table 3.1: Dc-dc converter specifications for mobile phone and hand-held ratio applications.

Symbol	Parameter	Min	Typ	Max	Units
$I_{o,max}$	Maximum load current		400		mA
V_{in}	Input voltage	2.8		5.5	V
V_o	Output voltage	1.0		1.8	V
I_{lim}	Switch peak current limit		1000		mA
$\Delta V_o/V_o$	PWM mode DC output voltage precision		2%		
V_{ripp}	PWM mode output voltage ripple		2		mV

In the capacitance dominated case, the voltage ripple is quadratically dependent on the ratio of LC filter cutoff frequency and the converter switching frequency. For a specified output voltage ripple and a given switching frequency, the product of the two filter components' values can be determined. And the specific L and C values can be decided by constraints of current ripple, cost and profile requirements of output capacitors. A ceramic capacitor is usually preferred in cellular phone applications to tantalum capacitor or electrolytic capacitor due to its smaller time constant τ_o, smaller capacitor physical profile, and higher reliability. As shown previously in Fig. 3.3, a smaller capacitor time constant leads to reduced output voltage ripple. The time constant of ceramic capacitor is about 0.1 to a few μs. The ceramic capacitor used in this work has a τ_o value of 1 μs, and the resulting output voltage ripple is 2 mV. Thus, the output voltage ripple can be still be reduced by choosing capacitor with smaller time constant.

3.4.3 Power Train Design

An optimal power loss can be achieved by making conduction loss and switching loss approximately the same [5]. However, this implies large transistors for both power switches which becomes expensive in terms of die area. In this work, the size of PMOS and NMOS are chosen to achieve a compromise between chip area and power loss. As such, the conduction loss dominates the switching loss at full load.

3.4.4 Summary

To meet the specifications in Table 3.1, some of the important system parameters are summarized in Table3.2.

Table 3.2: Some system parameters derived for application specification in Table.3.1.

Symbol	Parameter	Value	Units
f_s	Switching frequency at PWM mode	0.6–1.5	MHz
L	Inductor	10	μH
C	Output capacitor	47	μF
$R_{dson,P}$	On-resistance of power train PMOS	0.6	Ω
$R_{dson,N}$	On-resistance of power train NMOS	0.6	Ω

Chapter 4

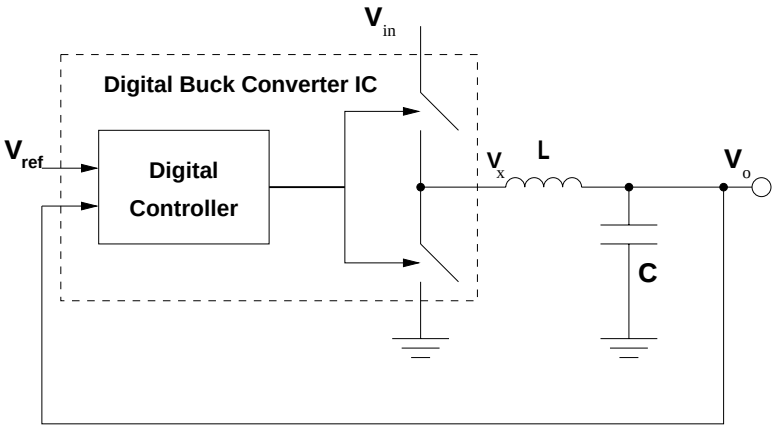
Architecture of the Dual-Mode Buck Converter IC

4.1 System Architecture

This chapter describes the architecture and voltage compatibility solution for the dual-mode ultra-low-power digitally-controlled buck converter IC for cellular phone applications. Fig. 4.1(a) is a buck converter system composed of the designed IC (in the dashed box) and the external LC filter, and Fig. 4.1(b) shows details of the dual-mode buck converter IC with power train and gate drivers on the same die.

As discussed in the previous chapter, the PWM control achieves good regulation quality and high efficiency at high load. But the efficiency becomes poor when the load goes low. So at light load, it is beneficial to switch to PFM control. The designed IC supports PWM mode for heavy load and PFM mode for light load. The pin MODE in Fig. 4.1(b) is used to switch between the two modes. In PWM mode, the error voltage $V_e = V_o - V_{ref}$ is quantized by the ADC to provide an error signal in the digital domain $D_e = (V_o - V_{ref})/V_b$, where V_b is a reference voltage and often takes the value of V_{in} or V_o depending on control purpose. The digital PID control block generates a duty ratio command D to feed into the digital PWM (DPWM) module which generates the pulses. The PFM mode, as a contrast, runs the converter in discontinuous conduction mode with variable frequency and fixed-on-time. The quiescent power of the PFM controller is the limiting factor for efficiency at ultra-light load. An ultra-low-quiescent-power PFM controller is designed to solve the problem.

For the digital implementation, smaller feature size processes with lower supply voltage are preferred to implement the controller to achieve smaller die area, higher speed and lower power. In cellular phone applications, the power supply of the buck converter system is



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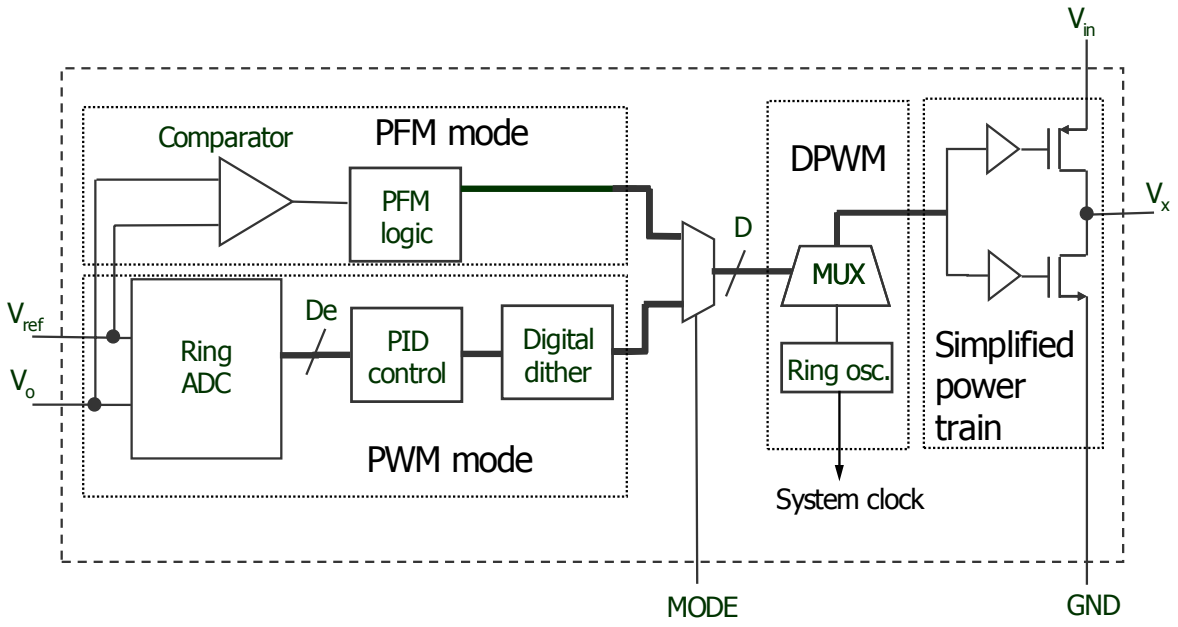


(b)

Figure 4.1: (a) System diagram of a digitally-controlled buck converter, (b) block diagram of digitally controlled buck converter IC for cellular phone applications.

typically a single cell Li-ion battery, which is commonly used in a discharge range between 4.2 V and 3.6 V. However, when the cellular phone sits in the charger, the supply voltage can go up to 5.5 V. Combine these voltage range and reliability considerations, the input voltage range of the DC-DC converter is usually specified to be from 5.5 to 2.8 V. Thus the input voltage of the converter may be higher than the allowed supply voltage of the process. A solution that resolves the voltage conflict can be of great interest, because it would allow the digital controller of the DC-DC converter with high input voltage to be implemented with low voltage process, making it possible to integrate power management unit with the load circuits on the same die. Significant cost reduction can be achieved consequently. Internal power management is introduced to resolve the conflict of high input voltage and a low voltage process, the details of which are presented in Section 4.4.

4.2 PWM Mode

4.2.1 Limit Cycling and Quantizer Resolution

Limit cycles exist in many sample-data systems due to signal amplitude quantizers such as ADCs and DACs. In digitally controlled buck converter systems, limit cycles may appear as steady-state oscillation of V_o and other system variables at a frequency lower than f_s. Limit cycles might lead to unpredictable voltage variations and thus are undesirable. Since the oscillation amplitude and frequency could be hard to predict, it is difficult to analyze and design for limit cycle operation. Sufficient conditions to eliminate limit cycles are

given in [16], which require the resolution of the DPWM to be greater than the resolution of the ADC.

In this work, due to required DC output voltage precision, the ADC quantization bin size is chosen to be 16 mV, which corresponds to 8.3-bit resolution under 5.5 V input voltage. And the DPWM has a step size of 5.4 mV, or equivalently a 10-bit resolution under 5.5 V input.

4.2.2 ADC and DPWM

The ADC and DPWM are used to provide the analog and digital interface between the digital compensation network and the buck converter. The design of power and area efficient interface elements is the key challenge of making a high performance low power digital controller. The DPWM runs in both PWM and PFM modes, hence a very low power DPWM is desirable for quiescent current consideration in PFM mode. A ring oscillator-multiplexer (Ring-MUX) based DPWM module is presented in Chapter 6, and also reported in [13]. The DPWM not only generates PWM signals, but provides clocks for the compensation network while in PWM mode, and for the sampling comparator while in PFM mode.

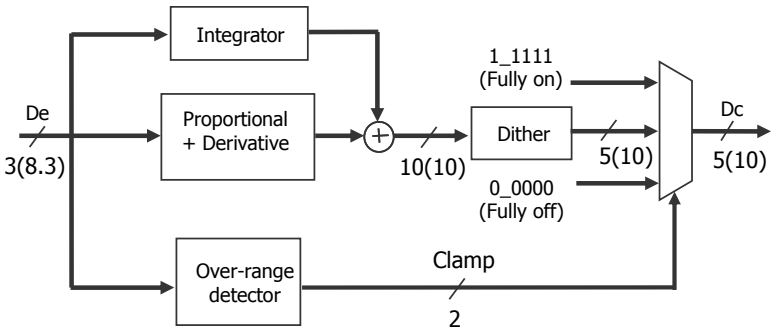
A general purpose ADC can be unnecessarily expensive in terms of power consumption and chip area. In PWM mode, an ADC with rail to rail quantization range is not required in the buck converter application since the output voltage V_o varies only within a small window centered at reference V_{ref}. A windowed-ADC scheme that gives high resolution only in the small window that contains the maximum possible V_o range is proposed, and a

novel averaging ADC implementation based on ring oscillators is presented in Chapter 5.

4.2.3 Digital Compensation Network

Fig. 4.2(a) shows the digital compensation network in PWM mode. When V_o is within the specified vicinity of V_{ref}, in this work a 80 mV window centered at V_{ref}, a digital PID control law is used to calculate the duty ratio command D for next switching cycle. In the unexpected case when V_o goes beyond the window range, the over range detector will activate the the clamping function which saturates the duty ratio command to fully on or off for a fast response. The PID compensation network continues to calculate for the appropriate duty ratio, and gets its output ready to replace the saturation function. Once V_o comes back within the specified window, the clamping function is deactivated and the PID network resumes the control of the converter through its output.

To avoid the stress on external components during the converter start-up, soft start is integrated in the digital controller. During start up, the proportional and derivative terms, as well as the over range detection are disabled. A startup counter that is clocked by the internal clock from the DPWM module gives a start up sequence and slews the integrator to the reach the appropriate steady-state value. At the end of soft start process, the proportional, derivative and the over range detector are enabled, and the PWM controller works with PID control with the saturation function previously discussed. The pin EN is used to start the soft start process. The complete digital compensation path with soft-start is shown in Fig. 4.2(b).



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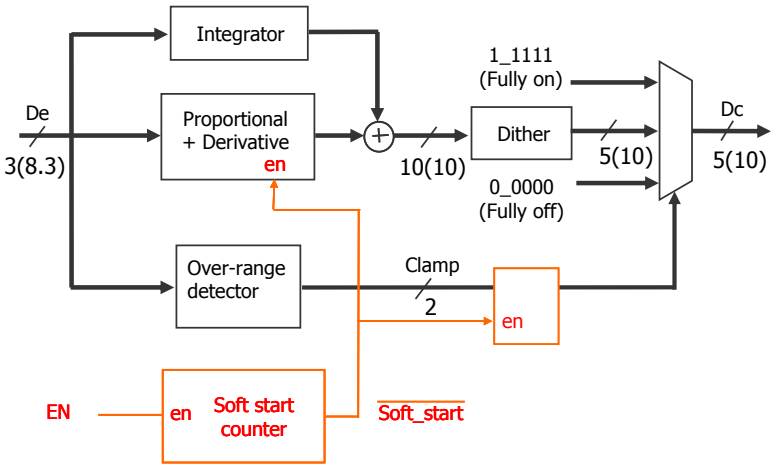


(b)

Figure 4.2: (a) PID compensation network, (b) compensation network with soft-start function. The number in front of the bracket is the actual number of bits of the signals, and the number in the bracket is the effective bits of resolution.

4.2.4 Summary of PWM Mode

Some parameters of the PWM mode controller are summarized in Table4.1.

Table 4.1: PWM mode parameters.

Parameter	Value	Units
ADC quantization step size	16	mV
Windowed ADC quantization range	80	mV
DPWM step size	5.4	mV
Effective ADC resolution	8.3	Bit
Effective DPWM resolution	10	Bit

4.3 PFM Mode

4.3.1 Ultra-Low-Power PFM Architecture

To improve the converter efficiency at light load, the controller runs in PFM mode when the cellular phone is in standby mode. That is, the buck converter runs in discontinuous conduction mode with a variable frequency and fixed on-time. As shown in Chapter 3, the total loss in PFM mode is composed of losses that are proportional to the load current, and the controller quiescent power which is independent of load current. At ultra light load, the controller quiescent power is the dominant term. In this work, the PFM mode controller includes a clocked comparator, a small logic block, and the DPWM, as shown in

Fig. 4.1(b), to achieve low quiescent power. A very low power internal voltage regulator is also running in PFM mode, which is discussed later.

Idealized operation of the fixed-on-time PFM controller as well as the output voltage and inductor current waveforms were shown in Fig. 3.8 of Chapter 3. When the cell phone is in standby mode and the load I_o is close to zero, $I_L - I_o \approx I_L$. Ignoring the jitter due to discrete sampling, the peak output voltage ripple ΔV_{max} at very light load can be calculated, and is given by

$$\Delta V_{max} = \begin{cases} \frac{\Delta I_L}{2C} t_{on} \frac{V_{in}}{V_o} + \frac{\Delta I_L}{2C} \frac{\tau_o^2}{t_{off}} & \text{for} \tau_o \leq t_{off}, \\ \frac{\Delta I_L}{2C} t_{on} + \Delta I_L R & \text{for} \tau_o > t_{off}, \end{cases} \tag{4.1}$$

where τ_o is the time constant of the output capacitor, ΔI_L is the peak inductor current, and t_{off} is the duration in which the inductor current decreases. Let t_{on} be the duration of PMOS conduction, or equivalently, the duration in which the inductor current increases. Duration t_{off} can then be given by

$$t_{off} = t_{on} \frac{V_{in} - V_o}{V_o}. \tag{4.2}$$

Table 4.2 lists the performance specification of the PFM mode.

Compared to the comparator, the DPWM, and the internal voltage regulator, the PFM logic involves only some very simple combinatorial logic and its power consumption can be neglected. The design of the low power internal regulator and the DPWM is illustrated in Section 4.4.3 and Chapter 6 respectively. Ultra-low-power comparators that sample in the mega-hertz frequency range are explored in the next section.

Table 4.2: PFM mode parameters.

Symbol	Parameter	Value	Units
t_{on}	Fixed on-time	1.3	μs
$f_{s,PFM}$	Sampling frequency in PFM mode	600	kHz
ΔV_{max}	Maximum voltage ripple at light load	90	mV

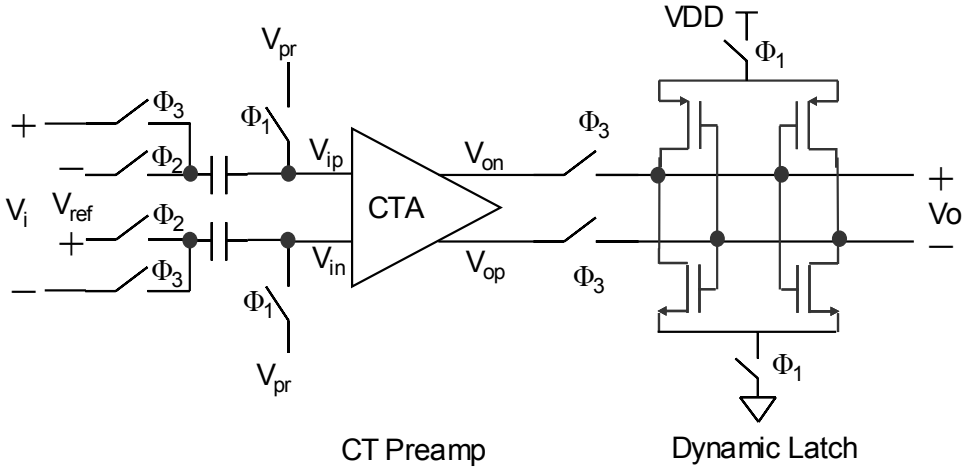
4.3.2 Ultra-Low-Power Comparator Design

A low-power comparator is used in the PFM controller to monitor the output voltage. In this section, two new zero-DC-current comparators are designed and another zero-DC-current comparator and a pulsed comparator are also discussed.

Pseudo Differential Charge Transfer Comparator

Based on a single-ended CMOS charge-transfer (CT) comparator in [17], a pseudo differential CT comparator is developed as shown in Fig. 4.3. The operation of the comparator involves a 3-phase clock, the timing diagram of which is shown in Fig. 4.4.

The core of the the pseudo differential CT comparator is a CT preamplifier. The operation of the CT preamplifier can be illustrated by considering the half circuit containing M_1 and M_3. During Φ_1, each storage capacitor C_T is reset to zero voltage. In Φ_2, the reference voltage is applied to the gate of M_1 and M_3, and the output node of the preamplifier is connected to a precharge voltage V_{pr}. The source of M_1 is thus precharged to one threshold voltage below corresponding reference voltage, and M_1 is cut off. Similarly, the source of



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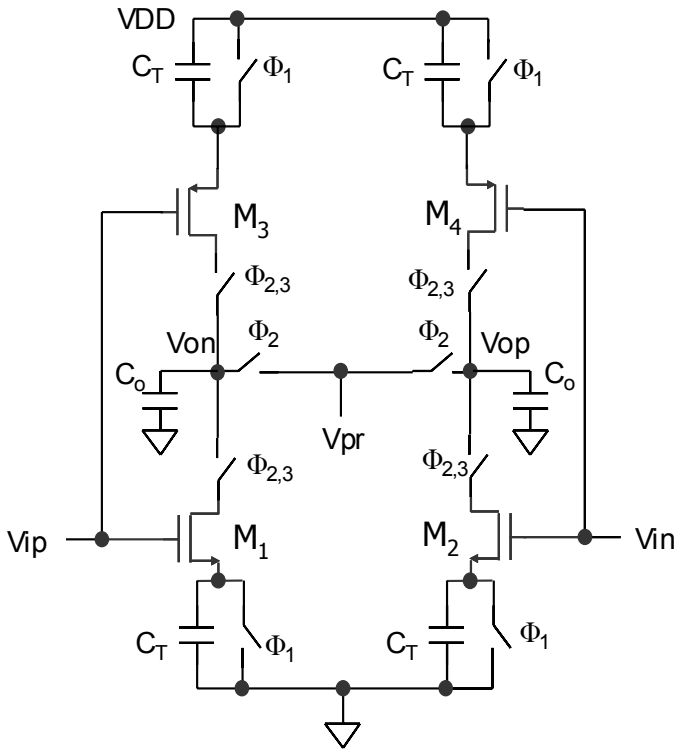
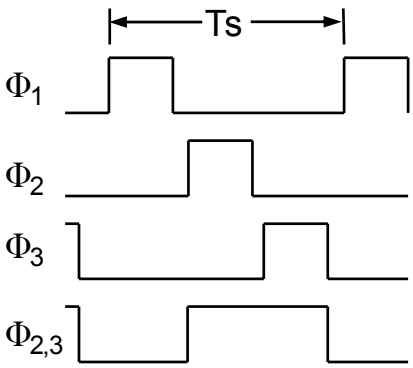


(b)

Figure 4.3: Pseudo differential CT comparator, (a) CMOS CT preamplifier and dynamic latch, (b) schematic of the CT preamplifier.



	Φ_1	Φ_2	Φ_3
CTA	Reset	Precharge	Amplify
D-Latch	Latch	Reset	Transfer

Figure 4.4: Timing diagram of the pseudo differential CT comparator.

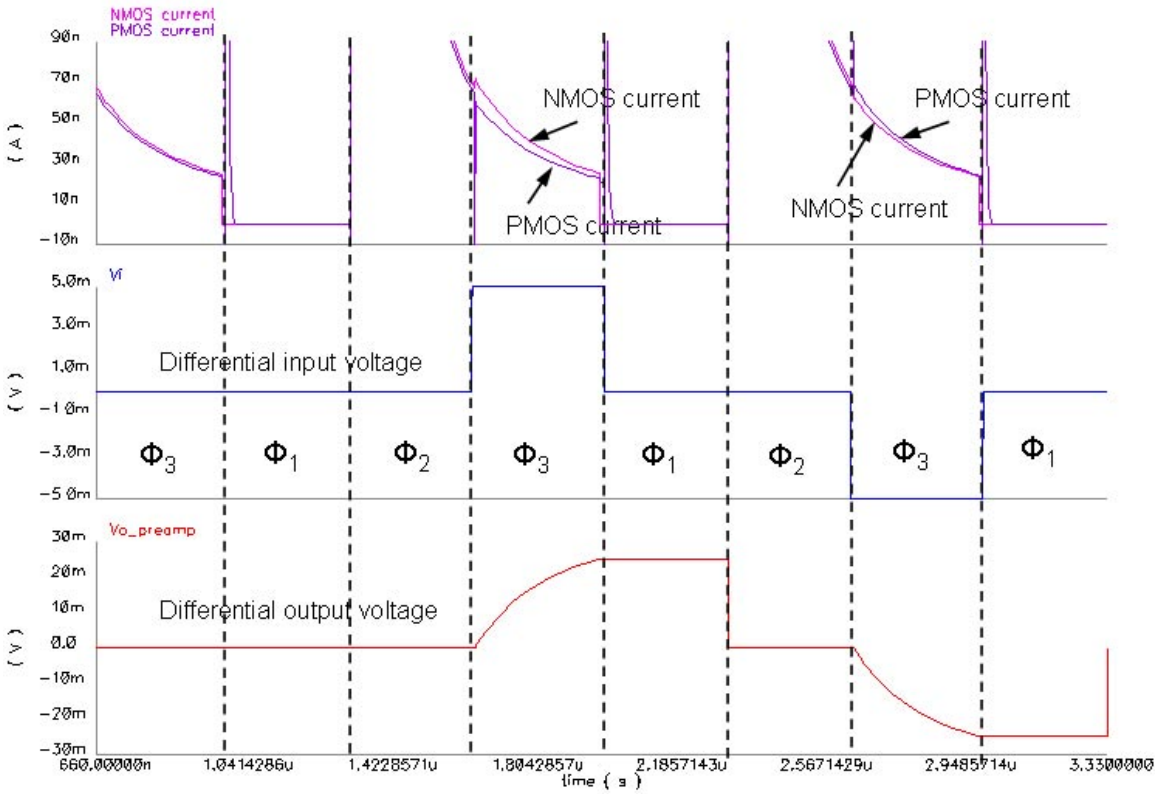


Figure 4.5: Simulated waveforms of the pseudo differential CT preamplifier.

M_3 is precharged to one threshold above the reference voltage. During Φ_3, which is the amplifying phase, the input voltage is applied to the gates of M_1 and M_3, instead of the reference voltage. If the input voltage is ΔV higher than the reference, some charge on C_o is transfered to C_T through M_1 until the source voltage of M_1 is raised by ΔV and M_1 is cut off again. The total charge transferred from C_o to C_T is $C_T \Delta V$, resulting in a voltage drop on the output node with value of $\Delta V C_T / C_o$. Thus, the gain of the preamplifier is set by the ratio of the storage capacitor and the output capacitor C_T / C_o. If the input voltage is lower than the reference, transistor M_3 conducts and the output voltage increases. The simulated waveforms of the CT preamplifier is shown in Fig. 4.5. Finally, after the amplifying phase, the dynamic latch regenerates and latches the output signals. The simulated current consumption of the pseudo differential CT comparator is 0.69μA/MHz.

The single-ended CT comparator reported in [17] has a potential problem of large offset voltage due to subthreshold current mismatch between NMOS and PMOS devices. After the precharge phase, the voltage across C_T continues to change even if $V_i = V_{ref}$ since subthreshold current still flows in both the NMOS and PMOS. Mismatch between the two currents results in significant offset voltage. By using the pseudo differential structure in Fig. 4.3, this offset is canceled with differential output, and the substhreshold current matching between NMOS and PMOS is replaced by the matching between the same type of transistors, which can be much better controlled. Thus, the offset fluctuation is greatly reduced by using the pseudo differential structure. The draw-back of the CT type of comparators is that a 3-phase clock is required.

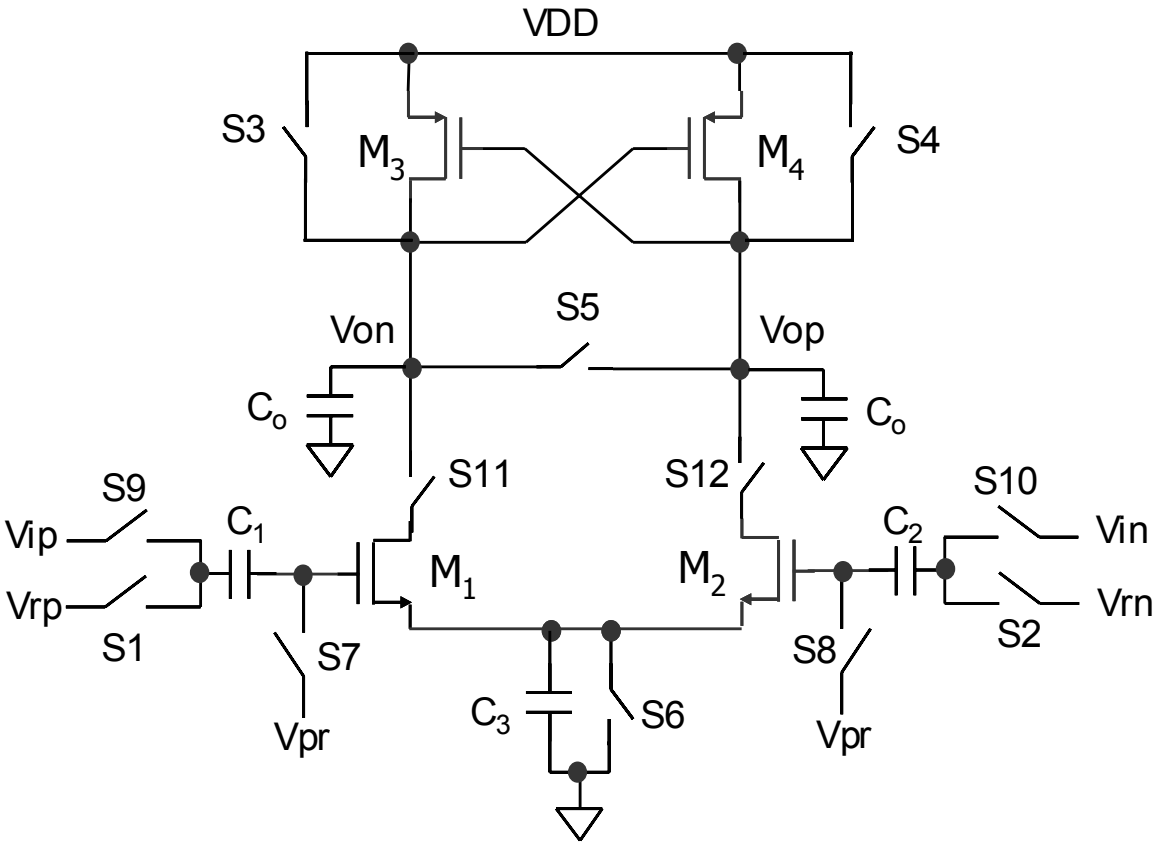


Figure 4.6: Schematic of the differential zero-DC-current comparator.

Differential Zero-DC-Current Comparator

A differential zero-DC-current comparator with AC coupled input is developed with schematic shown in Fig. 4.6. The simulated waveforms of this comparator with timing diagram are shown in Fig. 4.7.

The operation of this comparator involves a two-phase non-overlapping clock Φ_1 and Φ_2. During the preset phase Φ_1, switches $S1 - S8$ are on, $S9 - 12$ are off. Each output node, loaded with the capacitance C_o, is tied to VDD. The capacitor C_3 is shorted to ground. Differential reference voltage pair V_{rp} and V_{rn} is used to bias the input coupling capacitors.

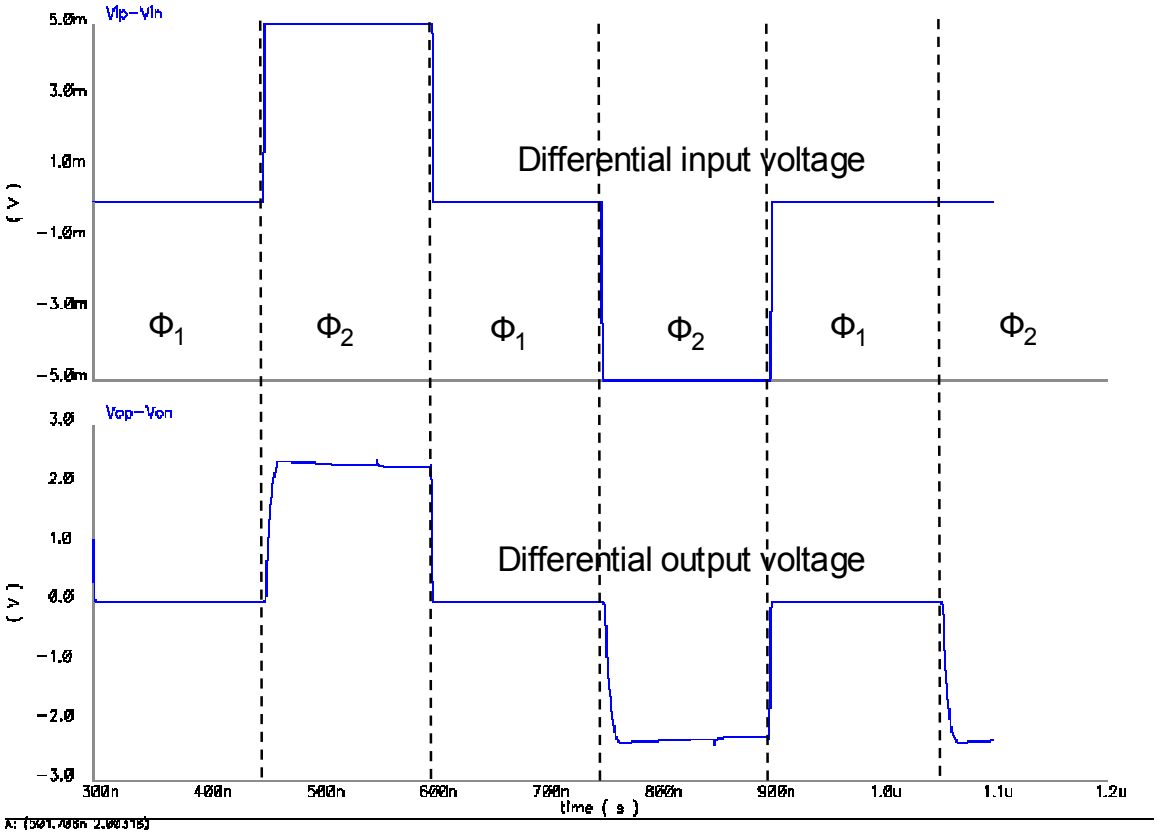


Figure 4.7: Simulated waveforms of the differential zero-DC-current comparator.

At the beginning of the evaluation phase Φ_2, $S1 - S8$ are off, and $S9 - S12$ are on. Since V_{on} and V_{op} were precharged to VDD, M_3 and M_4 are initially off. The error voltage $V_e = (V_{inp} - V_{inn}) - (V_{rp} - V_{rn})$ is AC coupled to the gates of differential pair M_1 and M_2. Differential current flows through M_1 and M_2 and develops a differential voltage across output nodes before the cross-coupled latch turns on. Then M_3 and M_4 regenerate the differential voltage to much higher swing. At last, a dynamic latch (not shown in Fig. 4.6) is used to fully regenerate the output signal to rail to rail swing and hold the logic level. The amplification process of this comparator is elaborated below.

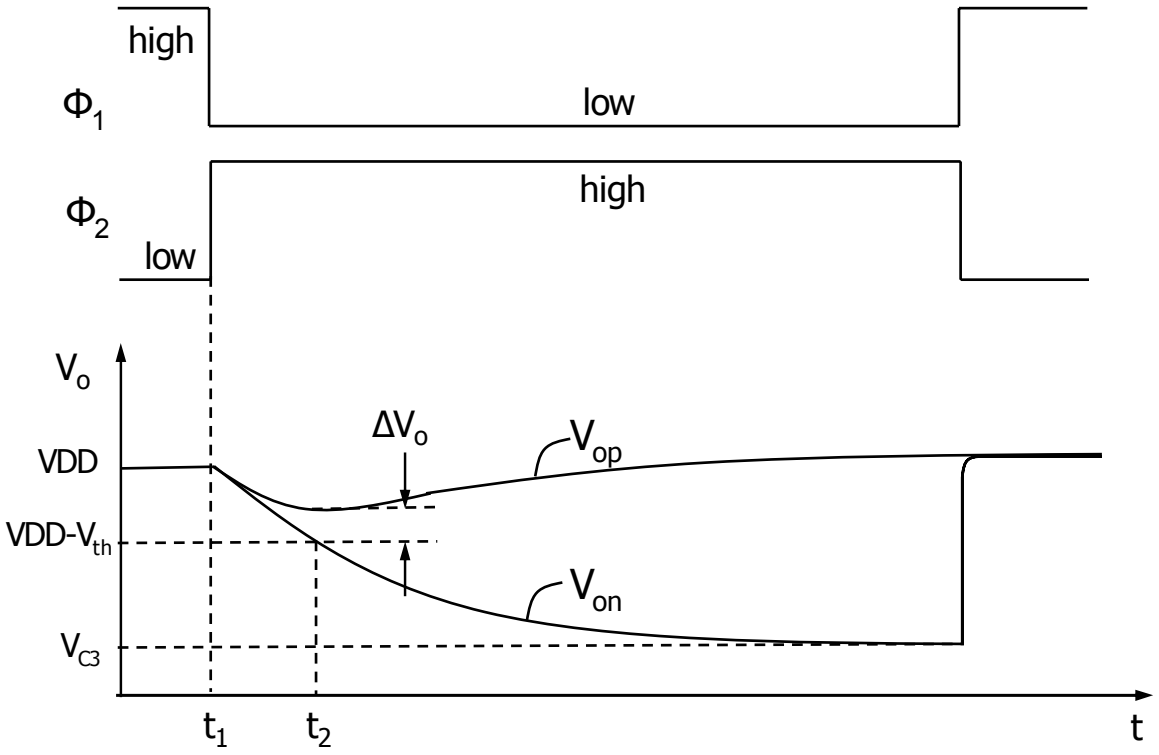


Figure 4.8: Conceptual voltage waveforms at the output nodes in the differential zero-DC-current comparator.

Without losing generality, assume $V_{ip} > V_{in}$, and the input differential voltage $\Delta V_i = V_{ip} - V_{in}$. The 2-phase clocks and the conceptual voltage waveforms of the output nodes are shown in Fig. 4.8, focusing on the amplifying process while Φ_2 is high. Let t_1 be the time when Φ_2 is on, and t_2 be the time when V_{on} drops to one threshold below VDD and thus M_4 starts to turn on. Therefore, the time interval (t_1, t_2) is the duration of the amplification in the comparator. The differential voltage developed across the output nodes at t_2 is $\Delta V_o = V_{op} - V_{on}$. Let ΔV be the overdrive voltage on M_1 and M_2, and ΔV is approximately a constant during the amplification moment if C_3 is much greater than C_o. Assume the threshold voltage of all the transistors is V_{th}, and the transistor aspect ratio of

the NMOS devices is W/L.

As shown in Fig. 4.8, at t_2, V_{on} drops to $VDD-V_{th}$, and V_{op} drops to $VDD-V_{th}+\Delta V_o$. Since during the interval (t_1, t_2), both M_1 and M_2 are in saturation region, it can be found that

$$C_o V_{th} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\Delta V^2(t_2 - t_1), \tag{4.3}$$

$$C_o(V_{th} - \Delta V_o) = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(\Delta V - \Delta V_i)^2(t_2 - t_1), \tag{4.4}$$

where μ_n is the electron mobility of the NMOS, and C_{ox} is the oxide capacitor.

Assuming $\Delta V_i \ll \Delta V$. Subtracting (4.4) from (4.3) results in

$$\begin{aligned} C_o\Delta V_o &= \tfrac{1}{2}\mu_n C_{ox}\tfrac{W}{L}\Delta V_i(2\Delta V - \Delta V_i)(t_2 - t_1) \\ &\approx \mu_n C_{ox}\tfrac{W}{L}\Delta V_i\Delta V(t_2 - t_1). \end{aligned} \tag{4.5}$$

Dividing (4.5) by (4.3), ΔV_o is given by

$$\Delta V_o = \Delta V_i \cdot 2\frac{V_{th}}{\Delta V}. \tag{4.6}$$

Thus if the overdrive voltage on the NMOS differential pair is designed to be a fraction of threshold voltage of PMOS, the comparator can have a well-defined voltage gain, and reasonably large differential voltage can be developed across the output nodes before the cross-coupled latch turns on.

This comparator has zero static power since the current flows only momentarily at the beginning of Φ_2. When C_3 is charged up to one threshold below the gate voltage of M_1

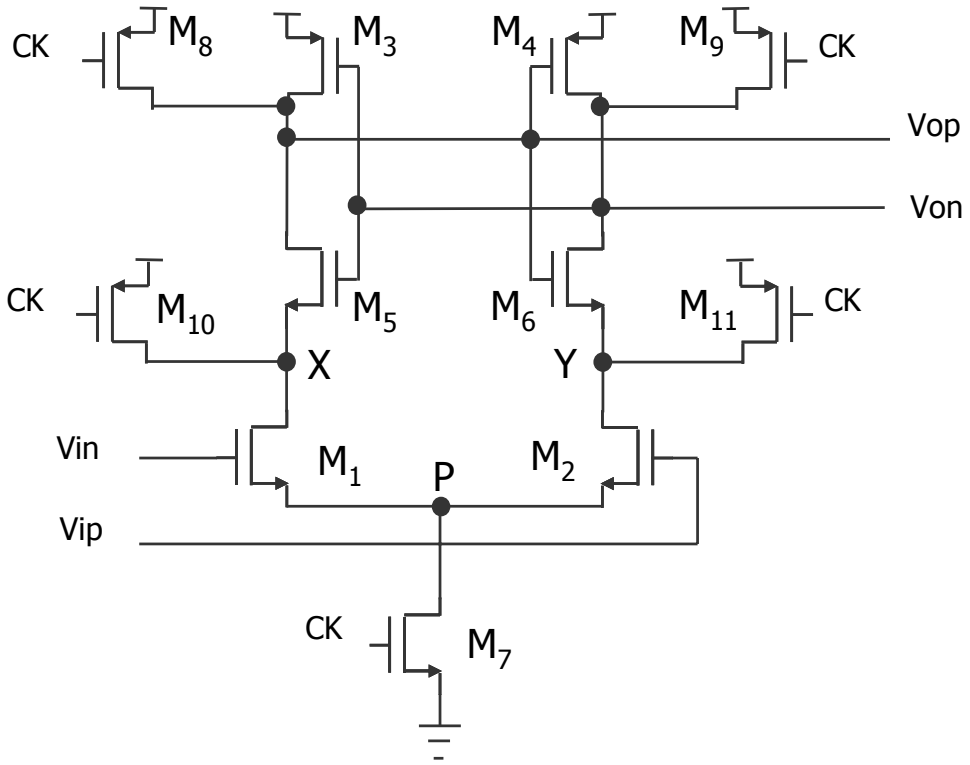


Figure 4.9: Schematic of zero-DC-biasing current comparator. [2]

and M_2, the main differential pair is turned off and the comparator does not take any more power from the supply. The simulated current consumption of the circuit is 1.4 μA/MHz.

Differential Zero-DC-Current Comparator 2 [2]

Another zero-DC-current comparator was reported in [2], the schematic of which is shown in Fig. 4.9. It involves only a single phase clock. When the clock signal CK is high, the comparator is in reset mode. Nodes V_{op}, V_{on}, x and y of the comparator are precharged to supply voltage by $M_{11} - M_{14}$, and node P is discharged to ground by M_7. When CK goes low, the comparator goes into evaluation and regeneration mode. Input pair

M_1 and M_2 resolve the input voltage, and like the previous one-shot comparator, a voltage difference is developed before the cross-coupled latch turns on. Then, the latch transistors $M_3 - M_6$ regenerate the amplified output signal swing to rail to rail . After the output signal is fully regenerated, the cross-coupled inverter pair holds the logic levels without taking any power. Very low power is consumed in the comparator since only dynamic current flows through the input pair and the regeneration pair during evaluation transient, and once the output signals are fully established, there is no DC current flowing in the comparator.

Compared to the previous differential comparator, this comparator has the advantage of using only a single phase clock, which simplifies the clock generation function. For this reason, this comparator is chosen to be used in the PFM controller. The current consumption of this comparator is also 1.4 μA/MHz.

Pulsed Comparator

For all the three zero-DC-current comparators discussed above, it is difficult to apply auto-zeroing schemes, except using chopper stablization. When used for high resolution applications in which offset cancelation is a must, comparators with continuous bias should be used. To reduce the power consumption in the continuously biased comparators, pulsed operation can be used.

In this work, the offset requirement for the PFM mode comparator is moderate, and the differential comparator of Fig. 4.9 without auto-zeroing is used.

4.4 Voltage Compatibility

In this work, the digital controller is implemented with a 0.25-μm CMOS process, with highest allowed supply being 2.75 V. In cellular phones, the input voltage specification is from 5.5 V to 2.8 V. Thus the input voltage of the converter is higher than the allowed supply voltage of the process. Internal power management is introduced to resolve the conflict of high input voltage and a low voltage process.

4.4.1 Cascoded Power Train

The power train is integrated on the same die as the controller chip. To protect both the high side and the low side switches from oxide breakdown caused by excessive gate-drain voltage, a cascode structure is used to implement each switch. The schematic of the cascoded low side switch is shown in Fig. 4.10. A constant internal reference voltage $V_m = V_{in}/2$ is developed to bias the cascode transistor M_1. The switch M_2 is driven by a PWM signal with a swing between V_m and ground. As for the high side switch, the cascode transistor is also biased with V_m. The difference is that the switch transistor on the high side is gated by a PWM signal with a swing between V_m and V_in. When the input voltage reaches maximum of 5.5 V, V_m is 2.75 V, which is safe for this process.

When the low side switch is on, the voltage on switching node SW is close to ground, so that each transistor sees gate-source voltage and gate-drain voltage of approximately V_m. When the low side switch is off, node SW is pulled up by the high side switch to close to V_{in}, M_1 sees the drain-gate voltage of $V_{in} - V_m$, and the source is charged to about

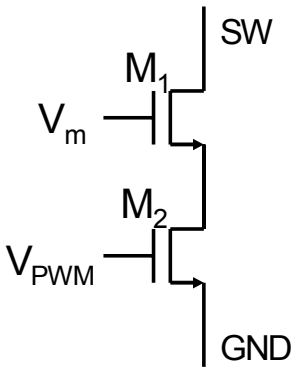


Figure 4.10: Cascode structure for low side switch.

$V_{in} - V_{th}$. The drain-gate voltage of M_2 is thus clamped to $V_{in} - V_{th}$. Therefore, both M_1 and M_2 are protected from seeing excessive voltage drops over their respective gate and diffusion region.

The measured breakdown voltage is 7.3 V for the cascoded NMOS and 7.9 V for the cascoded PMOS, respectively.

4.4.2 Internal Power Management

In addition to providing a proper gate bias for the cascoded power train transistors, V_m also serves as the internal power supply for the controller circuitry. A pair of linear regulators is used to provide a stable internal supply voltage V_m. The block diagram of the internal power management scheme is shown in Fig. 4.11.

The high side gate drive works between supplies V_{in} and V_m, and the low side gate drive works between V_m and ground. In this work, the high side PMOS and the low side NMOS are designed to have approximately the same equivalent on-resistance. Thus, the transistor

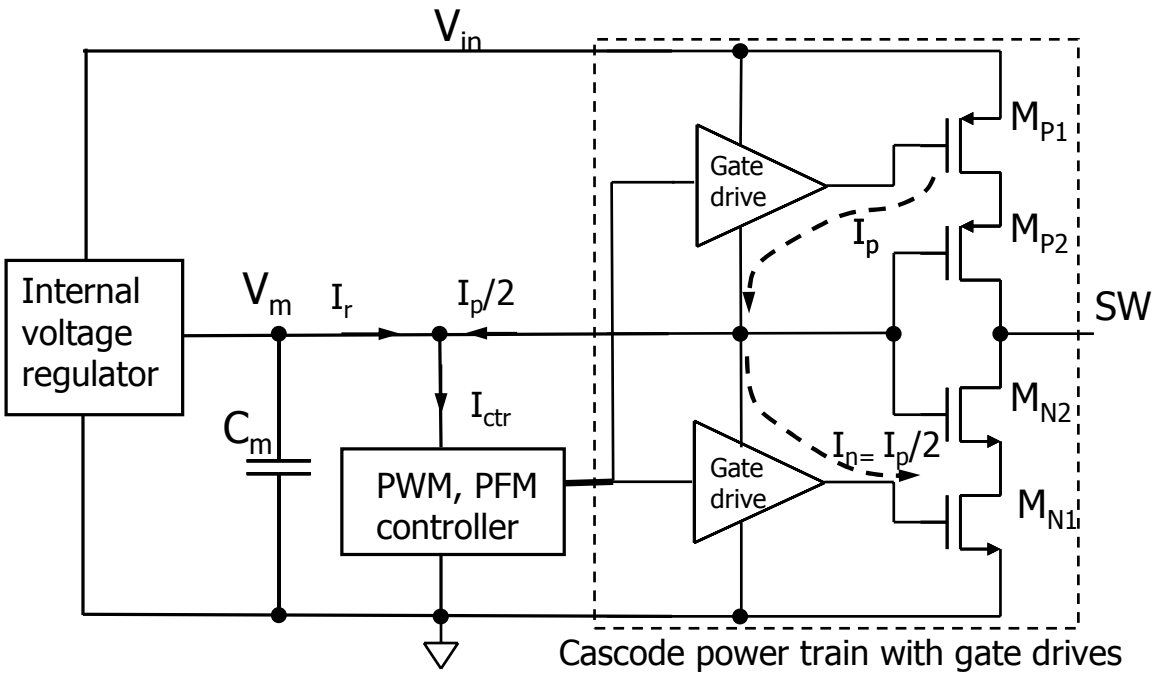


Figure 4.11: Block diagram of internal power management

aspect ratio of the PMOS is twice the ratio of the NMOS. With the same channel length, the gate capacitor of the PMOS is twice the gate capacitor of the NMOS, i.e. $C_{g,p} = 2C_{g,n}$. In each switching cycle, the average current I_p flowing into node V_m via the high side gate drive circuit is approximately twice the current I_n flowing out of node V_m via the low side gate drive circuit, since the power train PMOS transistor has twice the width of the NMOS transistor. The difference current $I_p - I_n$ can be used as a partial or complete supply for the digital controller. The total current consumed by the controller and the gate drivers can be calculated by summing the equivalent DC current that flows into the ground node. If the internal power management scheme is not employed, the total current would result in $I_p + I_n + I_{ctr}$, where I_{ctr} is the equivalent DC current drawn by the controller.

With the internal power management, the overall current consumption reduces to $I_n + I_{ctr}$, given that the DC bias current in the class B internal regulator is more than two orders of magnitude lower than I_{ctr} alone and thus can be neglected. Therefore, a current saving of I_p is achieved in PWM mode by using the internal power management scheme.

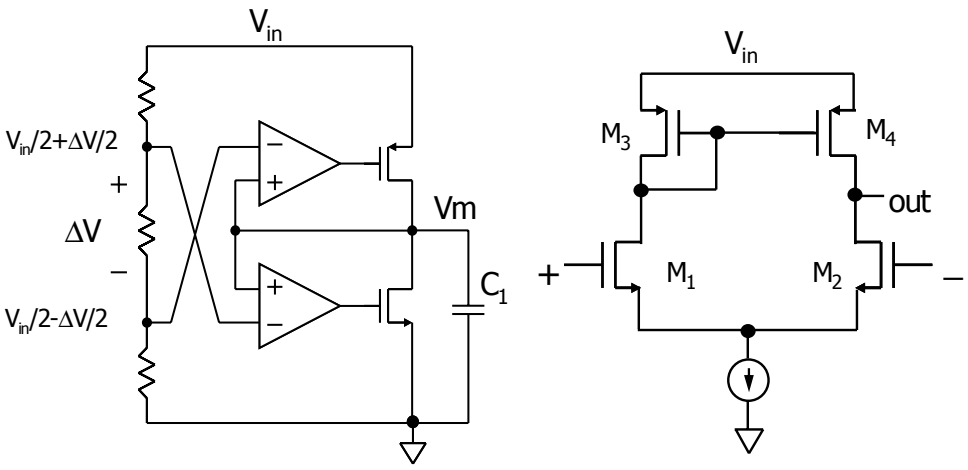
4.4.3 Internal Regulators

Two linear regulators are used to provide a stable V_m. The block diagram of the internal regulators are shown in Fig. 4.12(a), with schematic of the simple differential amplifier used in the regulators shown on the right. The reference voltage of the pull-up regulator is set ΔV lower than that of the pull-down regulator, thus V_m is regulated within a window of ΔV around $V_{in}/2$.

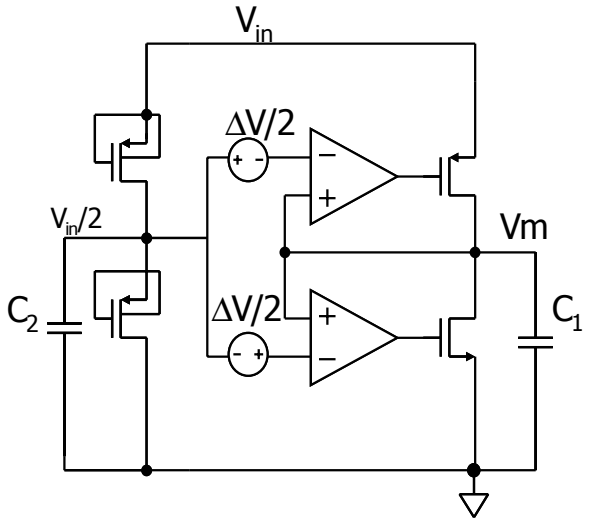
Since the internal regulators are always on to provide proper supply voltage level for the control circuits, the power dissipation of the two regulators must be very low to achieve low quiescent current in PFM mode. Building the reference voltages of $V_{in}/2 \pm \Delta V/2$ takes large chip area if a resistor divider is used. Thus, it is desirable to have a low-power single reference V_{in}/2 to which both linear regulators are referred, and have the threshold difference ΔV built into the regulators. The offset voltage in the CMOS differential pair shown in Fig. 4.12(a) is given by [18]

$$V_{OS} \approx V_{t1} - V_{t2} + \frac{V_{ovN}}{2}\left(\frac{V_{t3} - Vt4}{\frac{|V_{ovP}|}{2}} + \frac{\Delta(W/L)_P}{(W/L)_P} - \frac{\Delta(W/L)_N}{(W/L)_N}\right). \tag{4.7}$$

In this work, the threshold difference of ΔV between the two regulators is achieved by implementing an offset of $\Delta V/2$ on each of the linear regulators by varying the aspect ratio



(a)



(b)

Figure 4.12: Block diagram of internal voltage regulators (a) two linear regulators with different references, and the schematic of the amplifier used in the regulators, (b) two linear regulators with one reference and build-in threshold difference.

of the input transistors and load transistors, as shown in Fig. 4.12(b). Low power voltage reference V_{in}/2 can be implemented by using two identical MOSFET in cut-off region. Another possible implementation of the V_{in}/2 reference is by using a switched-capacitor circuit.

The simulated total bias current of the two linear regulators is $1\mu A$. Each regulator has a 40 kHz bandwidth. The allowed variation window around V_{in}/2 is 50 mV.

4.4.4 Voltage Interface: Level Shifters

Since the high side gate drive needs an input with voltage swing between V_{in} and V_m for safe operation, a level shifter must be used to convert the pulse signal from a swing of 0-V_m up to the desired range. Two possible ways to implement this level shifter are described in this section.

Level Shifter Concept 1: Bootstrap Circuit

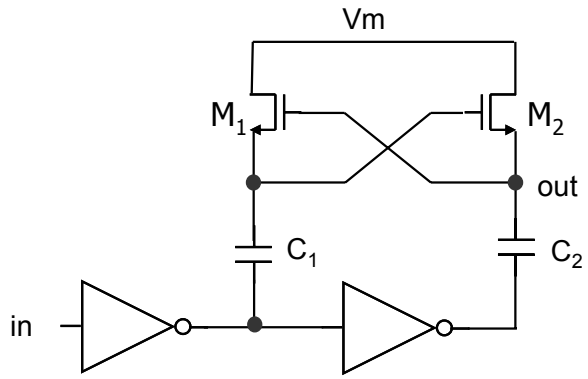


Figure 4.13: Schematic of a bootstrap circuit.

A bootstrap circuit is often used to implement level shifters. The schematic of a simple bootstrap circuit is shown in Fig. 4.13. A problem with bootstrap level shifters is its reliance on the storage capacitors to hold the voltage level. When the input voltage goes from high to low, capacitor C_2 gets recharged. When the input voltage goes from low to high, capacitor C_1 gets recharged. Thus, if the input signal flips frequently enough, each of the capacitor will get sufficient recharge to compensate for the charge loss due to the leakage. If the bootstrap circuit is left idling for a sufficiently long time, the leakage will discharge the capacitors until the voltage on each capacitor collapses. In the cell phone application, when the controller is in PFM mode and the load is light, the switching activity is rare and there is high risk of voltage collapsing on the capacitors. Thus this kind of level shifter is not appropriate for the cellular phone power management application.

Level Shifter Concept 2

Fig. 4.14 shows the level shifter used in this work to convert the pulse signal from the voltage swing of $0 - V_m$ to $V_m - V_{in}$. The output level is held by static logic and there is no risk of voltage collapse due to long term idling. This level shifter takes differential input voltage, and M_1 and M_2 are the input transistors. Transistors M_7 and M_8 form the latch. The gates of devices M_5 and M_6 are biased with V_m, and the output swing is therefore limited between V_{in} and V_m. Cascode NMOS devices M_3 and M_4 are inserted to protect the NMOS devices M_1 and M_2 from seeing excessive gate-diffusion voltage.

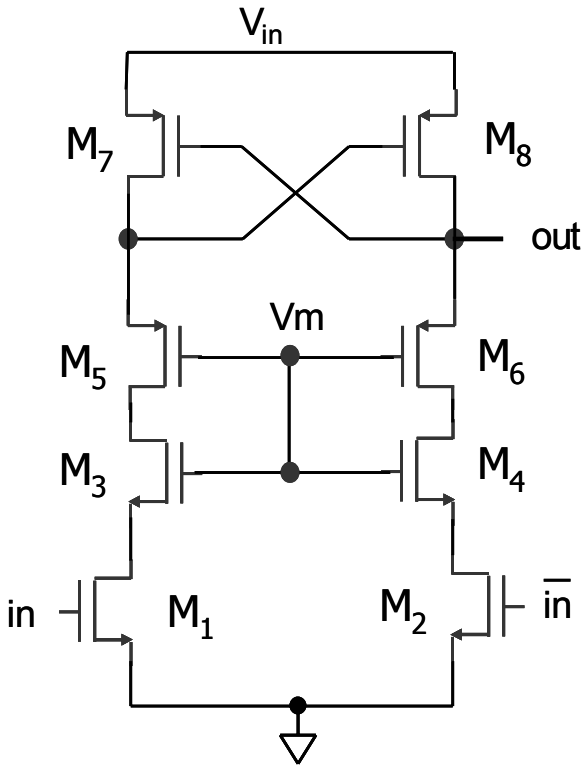


Figure 4.14: Schematic of the level shifter.

Chapter 5

Analog-to-Digital Converter Based on Ring Oscillators

5.1 Windowed ADC

In PWM mode, converter output voltage V_o is compared to reference voltage V_{ref} and the error voltage V_e is quantized to provide an error in the digital domain, $D_e = (V_o - V_{ref})/V_b$, where V_b is a reference voltage and often takes the value of V_{in} or V_o depending on control purpose. Since V_o is regulated to be in the vicinity of V_{ref}, using a high resolution ADC that covers the full range between ground and V_{in} will demand excessive power and silicon area. Rather, an ADC topology which has high resolution only in a small window around V_{ref} is desirable. A windowed ADC is proposed in this section.

The main idea is to reduce the quantization window to the possible V_o variation range, which is usually a window of tens of millivolts centered at V_{ref}. Due to switching activities of the power train switches, noise of switching frequency can be observed on V_o. An averaging ADC that realizes windowed quantization and also is robust against switching noise is desirable.

Synthesizable ADC's based on VCO or delay-line structures have been reported [8], [14]. In this work, an averaging windowed ring-ADC which is nearly entirely synthesizable is developed. This ring-ADC has 16 mV quantization bin size with a total quantization window of 80 mV, and takes 0.15 mm^2 chip area. At 600 kHz sampling frequency, the measured current consumption of this ADC is 37 μA. Compared to ADC's based on VCO or delay-line, this ring-ADC has invariant resolution under different reference voltage levels due to the common mode rejection capability of the differential pair, thus is suitable for a wide range of applications. Furthermore, the resolution of the ring-ADC can be controlled

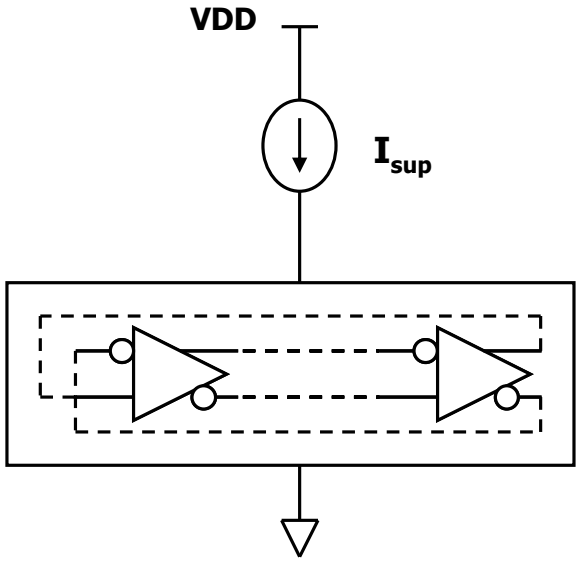
through the bias current, which can be made either constant or adjusted for automatic gain control. For example, the biasing current on the differential pair in the ring-ADC can be made a function inverse to input voltage, thus when the input voltage reduces, the gain of the ADC and hence the controller is raised, resulting in stabilized loop gain. In summary, the ring-ADC has low power and small area, and its resolution can be designed with high flexibility depending on application requirements. The quantization resolution of the ring-ADC can be scaled by changing the number of stages in the ring, or by varying the bias current of the differential pair.

5.2 Ring-ADC

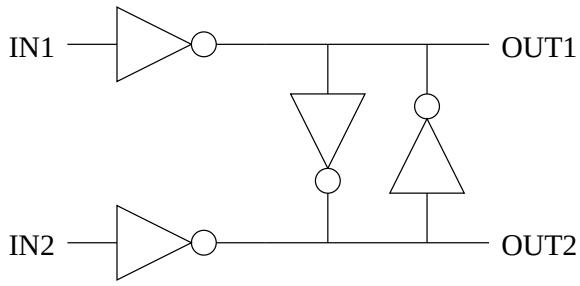
5.2.1 Frequency-supply current dependency

The design of a ring-oscillator ADC (ring-ADC) is based on the following observation on oscillation frequency and bias current of a ring oscillator. A differential ring oscillator as shown in Fig. 5.1(a) is biased with a current source I_{sup}. The delay stage in the ring oscillator is a pair of inverters with outputs cross-coupled by a latch as shown in Fig. 5.1(b). The supply current is low, forcing the oscillator to run in current starved mode with voltage swing below threshold of the MOSFET. A good linear dependency of the oscillation frequency on the supply current can be observed in Fig. 5.2. The empirical relation between the oscillation frequency f and supply current I_{sup} satisfies

$$f = k_1 \cdot I_{sup} + b, \tag{5.1}$$



(a)



(b)

Figure 5.1: (a)A 4-stage differential ring oscillator biased by a current source, (b) the delay cell in the differential ring oscillator.

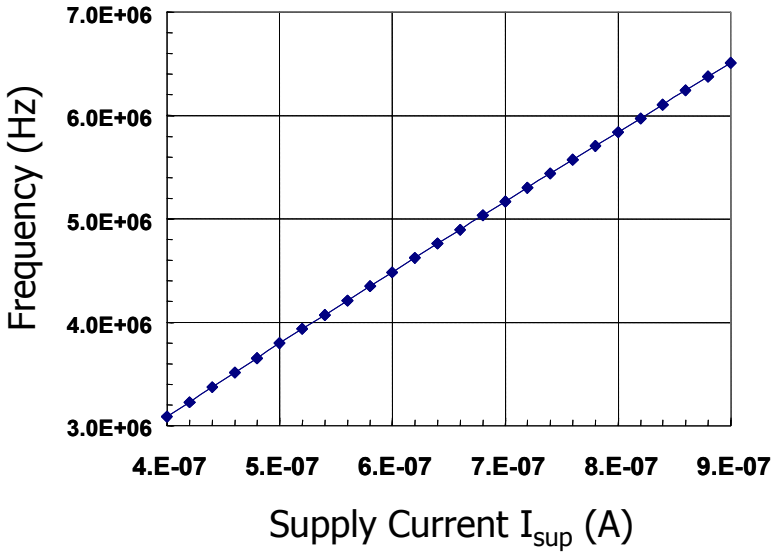


Figure 5.2: Simulated frequency-current dependency of the ring oscillator in Fig. 5.1(a).

where k is the frequency-current sensitivity index, the value of which depends on the ring oscillator structure and load conditions, and b is an offset, which is very small compared to the oscillation frequency f. Ignoring the offset b, a simple model can be used to describe the frequency-current dependency. For a MOSFET operated below threshold, the drain current is exponentially dependent on the gate source voltage. Thus, in a ring oscillator biased in subthreshold region, the short-circuit current is very low and the total power consumption approximately equals to the dynamic loss. Assume N is the number of taps in a ring oscillator, C is the lumped capacitance on each tap, and V_{swing} is the voltage swing in the ring, the dynamic loss equals to $NCV_{swing}^2 f$. Therefore, the total bias current I_{sup} can be calculated by deviding the dynamic loss by the voltage swing, resulting in

$$I_{sup} = NCV_{swing} f. \tag{5.2}$$

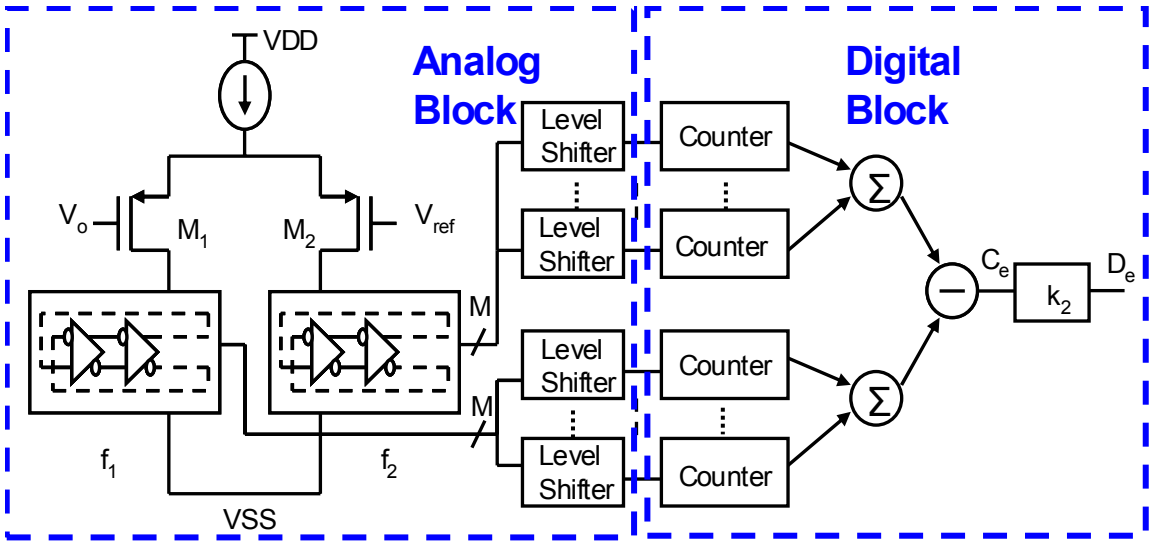


Figure 5.3: Block diagram of ring-ADC.

Thus, the frequency-current sensitivity index k is given by

$$k = \frac{1}{NCV_{swing}}. \tag{5.3}$$

In this work, the calculated value of k based on above model is 6.48e12, which is very close to the empirical value of 6.83e12 from the frequency-current curve. Similar linear frequency-current dependency can be observed in single-ended ring oscillators, too.

5.2.2 Ring-ADC Architecture

The block diagram of the ring-ADC is shown in Fig. 5.3. The ADC has a simple analog block and a digital block. The digital block is completely synthesizable.

A differential input pair M_1 and M_2 drives two identical N-stage differential ring oscillators as a matched load. The bias current is such that the voltage swing on the ring

oscillator is always below threshold. The error voltage v_e develops differential current in the two branches that results in instantaneous differential frequency at the two oscillators. The frequency of each oscillator is captured by a counter that is reset at the beginning of each sampling cycle. At the end of the cycle, one counter output is subtracted from the other, based on which, the quantized error D_e is calculated.

Let the biasing current in the tail current source be $2I_0$, and the frequencies of both oscillators be f_0 when input error voltage is zero. Assume $v_e = V_o - V_{ref}$ is the error voltage that goes to the input of the differential pair, Δf is the resulting frequency difference, and g_m is the transconductance of the input transistors. Since the swing on each ring oscillator is below threshold, each of the two ring oscillator's frequency and bias current has the linear dependency

$$f_i = k \cdot I_i + b, \quad i = 1, 2. \tag{5.4}$$

And, the differential frequency Δf is

$$\Delta f = f_1 - f_2 = k\Delta I. \tag{5.5}$$

At the end of the sampling period, ignoring the quantization error and output code uncertainty which is elaborated in the next section, the differential counter output is

$$\begin{aligned} C_e &= C_1 - C_2 \\ &= \Delta f \cdot T_s \qquad (5.6) \\ &= k\Delta I T_s. \qquad (5.7) \end{aligned}$$

Assuming the input pair has good linearity over possible v_e range, the differential cur-

rent $\Delta I = I_1 - I_2$ can be calculated through the small signal model of the differential pair

$$\Delta I = g_m \cdot v_e. \tag{5.8}$$

Substituting (5.8) into (5.7), C_e has the following expression

$$C_e = k g_m T_s v_e. \tag{5.9}$$

Substituting k with equation (5.3), C_e is given by

$$C_e = \frac{g_m T_s}{N C V_{swing}} v_e. \tag{5.10}$$

The final error voltage represented in a digital format D_e equals C_e divided by the gain from the signal path.

5.2.3 Output Range and Monotonicity of the Ring-ADC

Due to initial phase uncertainty in the oscillator waveforms at the beginning of the sampling period, each individual counter output $C_i (i = 1, 2)$, and the differential output $C_e = C_1 - C_2$ have uncertainties, too. When the error voltage v_e is zero, neglecting the mismatch between the differential pair and between the two ring oscillators, the frequency of the two oscillators are identical. Let f_0 be the oscillator frequency under zero input error voltage, then f_0 can be written as

$$f_0 = (n + x) f_s, \tag{5.11}$$

where f_s is the ADC sampling frequency, which equals the converter switching frequency in this case, n is an integer and $x \in [0, 1)$. With zero input error voltage, the counter

output at the end of each sampling period can be either n or n+1 depending on the initial phase at the beginning of the sampling period. Considering that the initial phase in one ring oscillator is independent of the other, subtracting one counter output from the other, results in C_e with three possible values: -1, 0, and +1. Since ideally, C_e is zero with zero input voltage v_e, the actual value of C_e has uncertainty range of 2.

Fig. 5.4 shows the transfer characteristics of the ring-ADC. The shaded area marks the possible range of value that the code C_e may end up. It can be noticed that with different values of x, the shape of the shaded area varies. However, the range of possible C_e values is always 2, for any given error voltage v_e. Let ΔV represents the increment of the input voltage v_e, by which the differential digital code C_e increases by 2. In other words, Δf increases by $2f_s$ with every increment of ΔV on v_e, according to (5.6). The value of ΔV can be calculated using (5.3), (5.5), and (5.8), by substituting Δf with $2f_s$

$$\Delta V = \frac{2f_s NCV_{swing}}{g_m}. \tag{5.12}$$

Therefore, to have a monotonic output, the quantization step size of the ring-ADC has to be greater than ΔV.

Assume each ring oscillator in the ring-ADC has N taps. To reduce the output uncertainty, instead of looking at one tap per ring, all the N taps on each ring oscillator are observed for frequency information through N counters. And all the counters' output are summed to get the total counter readout, resulting in a gain of N. Thus, the differential counter output C_e has the following expression

$$C_e = N\Delta f T_s. \tag{5.13}$$

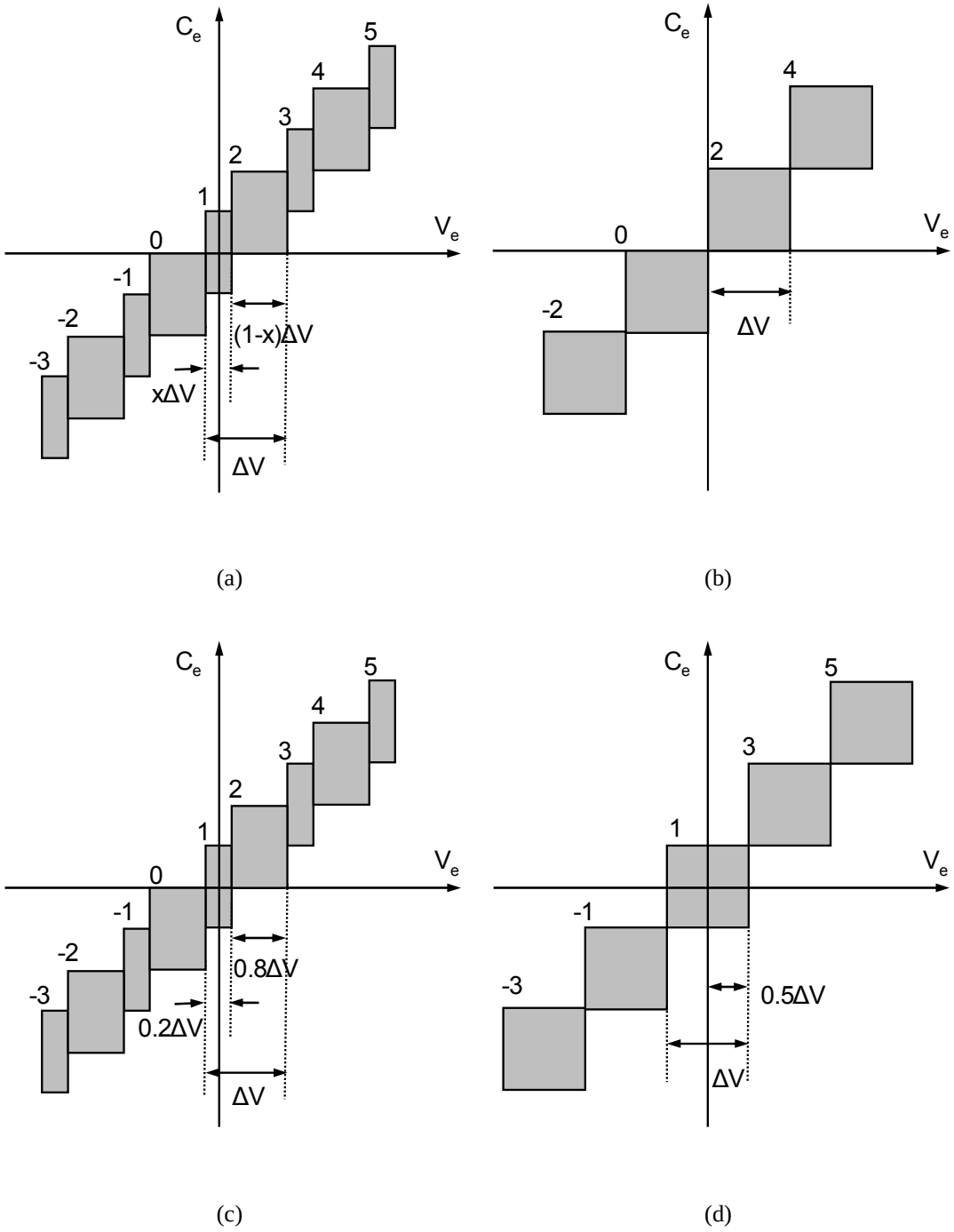


Figure 5.4: Uncertainty range of output code C_e (a) general form with $f_0 = (n + x)f_s$, where n is an integer and $x \in [0, 1)$, and three special case with (b) x=0, (c)x=0.1, (d)x=0.5, respectively.

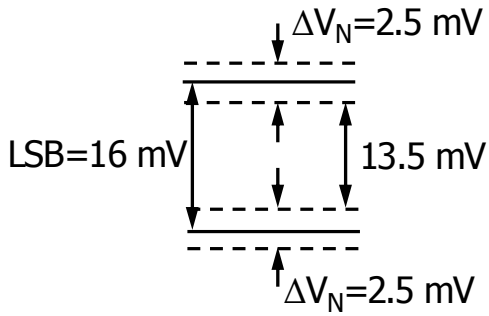


Figure 5.5: The LSB of the ring-ADC and the input voltage range, ΔV_N, that may cause uncertainty in C_e.

The range of C_e value variation for a given v_e is still 2. Let ΔV_N be the new increment of v_e, by which the differential digital code C_e increases by 2. Using (5.3), (5.5), (5.8), and (5.13), ΔV_N is given by

$$\Delta V_N = \frac{2 f_s C V_{swing}}{g_m}. \tag{5.14}$$

Therefore, by getting frequency information from all N taps on each ring, the minimum quantization step size for a monotonic ring-ADC can be reduced by a factor of N. In this work, a pair of four-stage differential ring oscillators are used in the ring-ADC, thus there are eight taps in each ring. A 3-bit resolution increase can be achieved by looking at all the taps in the ring. Instead of choosing the LSB of the ADC to equal to ΔV_N, in this work, the ADC LSB is 16 mV, which is much greater than the calculated ΔV_N, i.e. 2.5 mV, as shown in Fig. 5.5. Thus, the ring-ADC is monotonic, and the input voltage range that may cause output uncertainty is sub-LSB.

5.2.4 Resolution of Ring-ADC

The final expression of C_e is given by

$$C_e = \frac{g_m T_s}{C V_{swing}} v_e. \tag{5.15}$$

Obviously for a given oscillator structure, the lumped capacitance is a constant. The voltage swing V_{swing} varies very weakly with bias current, and can be treated as a constant, as well. Thus, the resolution of a ring-ADC with sampling period T_s is determined by the transconductance of the differential pair. Contrary to intuition, increasing the number of stages in the ring oscillator does not increase the resolution of the ADC, because the frequency-current sensitivity index k is inversely proportional to the number of stages.

5.2.5 Linearity of Ring-ADC

In the buck converter applications, the ADC linearity is not critical. Thus only some comments are given on the linearity of the ring-ADC.

The ring-ADC discussed above has the advantage of automatic monotonicity as long as the quantization step size is greater than ΔV_N. Thus, the differential non-linearity (DNL) of the system has an upper bound of $\Delta V_N/2$, which is a well-controlled value compared to that in comparator-based ADC's, where the offset of the comparators is random and leads to a less predictable DNL.

The integral non-linearity (INL) of the ring-ADC relies on the linearity between frequency and biasing current in the ring oscillators, which is good in subthreshold region.

The INL also depends on the linearity of the input differential pair. Since the saturation behavior of the input differential pair depends on the ratio of the input voltage and the overdrive voltage of the differential pair, good linearity of the input transistors can be acquired by designing the overdrive voltage a few times higher than the input voltage. Since v_e is usually less than 100 mV, the overdrive voltage needs to be only a few hundred millivolts.

5.2.6 Level Shifters

Since the signal swing on the ring oscillator outputs in the ADC is below the threshold voltage of CMOS transistors, level shifters shown in Fig. 5.6 are required to restore the differential signals to full swing. Since the input voltage is below the threshold voltage, the two NMOS devices have to be much stronger than the PMOS cross-coupled pair. Because of the subthreshold input operation, the delay of the level shifter is sensitive to parameter variations, such as the NMOS threshold voltage variation. However, the delay variation of the level shifters does not influence the steady-state resolution of the ADC. This level shifter has zero static power, and the simulated current consumption is 0.4 μA/MHz.

As mentioned earlier, the linearity between the oscillation frequency and the biasing current also exists in single-ended ring oscillators. Thus a single-ended oscillator with an odd number of stages can also be used to implement the ring-ADC. However, in the single-ended ring oscillator case, the differential low swing signals are not available for level restoration using the level shifter in Fig. 5.6. A low-swing signal going through an inverting stage biased by the same current-starving scheme results in an inverted signal

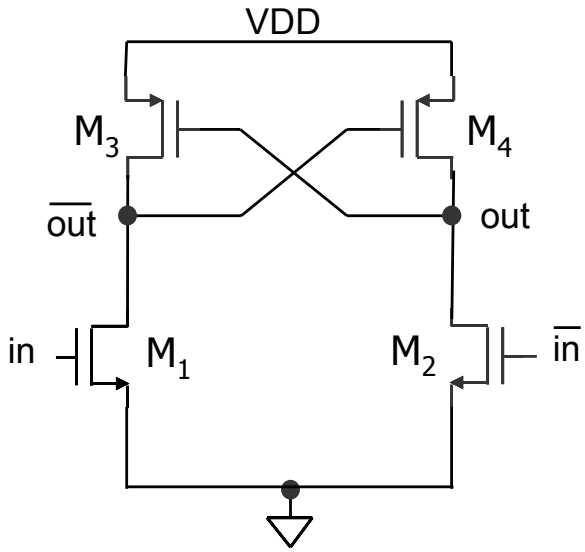


Figure 5.6: Schematic of differential level shifter that converts signal swing from sub-threshold to rail-to-rail.

with excessive delay, and is thus not appropriate for the level shifting function. In such a case, a ring level shifter, as illustrated in Fig. 5.7, can be considered.

For a five stage ring, signals $in_1 - in_5$ are the inputs to the ring level shifter and out_1- $- out_5$ are the outputs. When the propagating transition edge in the ring oscillator reaches the input NMOS of one stage of the ring level shifter, the output of the previous level shifter stage is arriving at the PMOS of the same level shifter stage. The two signals have the same transition direction and work together to generate an inverting output with restored swing.

5.2.7 Implementation of Ring-ADC

For the cell phone applications, a ring-oscillator ADC with 16 mV quantization bin size, or 8.3-bit resolution, and a quantization window of 80 mV is implemented in a 0.25-μm CMOS N-well technology. At a sampling frequency of 500 kHz, the measured current

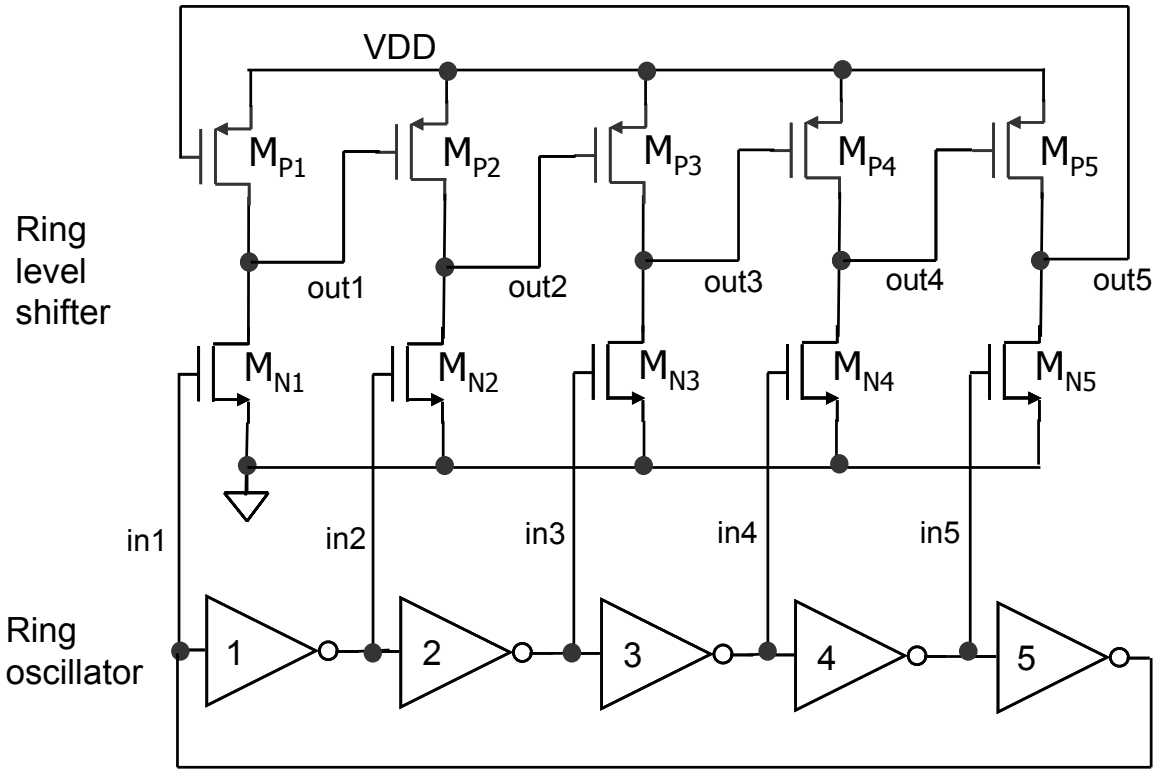


Figure 5.7: Schematic of a ring level shifter connected to a 5-stage single-ended ring oscillator.

consumption of the ADC is 37 μA at 3.0 V input voltage, out of which 19 μA is consumed by the digital block, and 18 μA by the analog block. The bias current for the differential pair is only 1.68 μA, thus most of the current in the analog block is taken by the eight differential level shifters. The total area of this implementation is 0.15 mm^2, most of which is taken by the digital block.

Both the power consumption and the die area of the ring-ADC can be greatly reduced by using a latch and a counter, instead of a number of counters, to monitor the signals on all the taps in each ring. Since each oscillator is fully differential and has 4 stages, only 4 taps are needed to determine the state of each ring oscillator. The improved ring-ADC

implementation is shown in Fig. 5.8. Only one tap per ring is used to drive a counter, and the integer number of oscillation period each ring goes through in one ADC sampling period is captured by this counter. The phase of each oscillator waveform at the end of the sampling period is recorded by latches L1 and L2. The fraction of a oscillation period each ring oscillator goes through in one sampling period can be calculated by subtracting the latch output of the previous sampling cycle from the latch output of the current cycle, i.e. L1[n]-L1[n-1] for the left-hand-side ring, and L2[n]-L2[n-1] for the right-hand-side ring. The differential output C_e is thus given by

$$C_e[n] = N(C_1[n] - C_2[n]) + ((L1[n] - L1[n-1]) - (L2[n] - L2[n-1])). \quad (5.16)$$

Notice that the above equation can be rewritten as

$$C_e[n] = N(C_1[n] - C_2[n]) + ((L1[n] - L2[n]) - (L1[n-1] - L2[n-1])), \quad (5.17)$$

which gives the implementation shown in Fig. 5.8. Compared to direct implementation of equation (5.16), which requires four 4-bit latches to record L1[n], L1[n-1], L2[n] and L2[n-1], equation (5.17) requires only three 4-bit latches.

In the improved implementation, only one level shifter per ring works continuously in each sampling period. The other three level-shifters are activated momentarily at the end of each sampling period. Thus, the dynamic loss from the level shifters is greatly reduced. In the digital block, compared to the first implementation shown in Fig. 5.3, the number of counters that run at the fundamental oscillation frequency reduces from 16 to 2, as shown in Fig. 5.8, and the number of adders (or subtractors) are also reduced accordingly. Three 4-

bit latches are added in the second implementation, but the overhead caused by the latches is trivial compared to the power saving from the counters and the adders. Therefore, the total power consumption of the ring-ADC can be greatly reduced. Since the power saving comes from the reduction of hardware, the die area of the ring-ADC can also be improved.

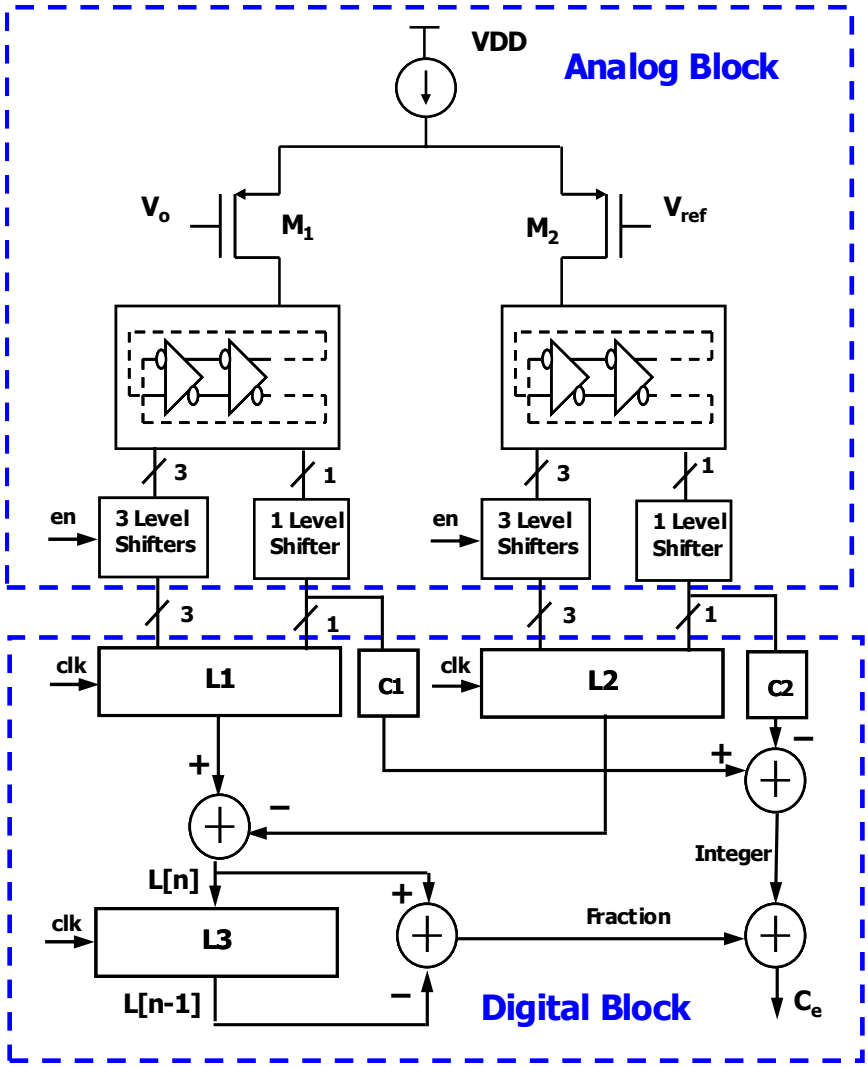


Figure 5.8: Improved implementation of the ring-ADC. L1-L3 are latches, and C1 and C2 are counters.

Chapter 6

Digital Pulse Width Modulation

6.1 Overview of Digital PWM Generation Schemes

6.1.1 Dither and Digital PWM

As illustrated in Chapter 4, to meet the sufficient conditions to prevent limit-cycling in steady-state operation, the resolution of the digital PWM (DPWM) module should be higher than that of the ADC. In this work, the regulation precision of the converter requires an ADC resolution of effectively 8.3-bit, and the DPWM resolution is chosen to be 10-bit.

One method which can increase the effective resolution of a DPWM module is dithering [16]. The idea is to vary the LSB over a sequency of consecutive switching periods, so that the average duty cycle has a value between two adjacent quantized duty cycle levels. The high frequency variation of the LSB is filtered by the output LC filter to achieve an averaging effect. It was shown in [16] that by using dither patterns spanning 2^M switching periods, the effective DPWM resolution can be increased by M bits,

$$N_{dpwm,eff} = N_{dpwm} + M \tag{6.1}$$

where N_{dpwm} is the hardware DPWM resolution, and $N_{dpwm,eff}$ is the effective DPWM resolution. In this work, M is chosen to be 5-bit, thus the actual hardware resolution of the DPWM is also 5-bit.

6.1.2 Overview of DPWM Schemes

One method to create digital PWM signals is with a fast-clocked counter-comparator scheme [7]. Such a design takes reasonable die area but the power consumption reported

is on the order of mW's. The main reason is that in this scheme, a high frequency clock and fast logic circuits are needed to achieve a reasonable resolution for a given switching frequency. For example, for a voltage regulator with 10-bit resolution and 1 MHz switching frequency, a 1 GHz clock is needed. For a counter-comparator DPWM, the main design challenge lies in the fast logic design. The counter-comparator scheme is illustrated in Section 6.2 and the design of an ultra-fast flip-flop is also presented. Simulation shows that this proposed flip-flop is faster than the previously reported fastest flip-flop [19], implemented in the same technology, with the same layout area and power consumption.

A tapped delay-line DPWM is proposed in [10]. Power is significantly reduced with respect to the fast-counter-comparator scheme since the fast clock is replaced by a delay line which runs at the switching frequency of the converter. One drawback of this design is that the delay line is not suited for the multi-phase application. In a multi-phase controller, precise delay matching among the phases places a stringent symmetry requirement on the DPWM module.

A ring-oscillator-MUX (ring-MUX) DPWM has been developed [13], which has area and power similar to those of the delay line approach. The ring-MUX scheme has the advantage of a symmetric structure, which can be used in multi-phase applications. Also, the ring oscillator serves as the clock generator for the whole controller system. The ring oscillator in the DPWM is biased in current-starved mode, and the signal swing on the ring oscillator is below threshold, resulting in even lower power than the tapped delay-line case. The design of the ring-oscillator-MUX DPWM is presented in Section 6.3.

6.2 Counter-comparator DPWM

6.2.1 Counter-comparator DPWM

An N-bit counter-comparator DPWM is illustrated in Fig. 6.1. At the beginning of each switching cycle, the N-bit output Q[N-1:0] of the asynchronous counter is zero, and the PWM signal is on. An N-bit comparator compares Q[N-1:0] with the command duty ratio D[N-1:0]. The clock drives the counter until Q[N-1:0]=D[N-1:0] is detected by the comparator, and then the PWM signal turns off.

The comparator stage is composed of static logic only and can be designed to have very small delay, thus the critical path in the counter-comparator scheme is the N stages of T-flip-flops (TFF) in series and the last stage of the comparator. The delay of the critical path has to be smaller than the period of the fast system clock T_{clk}, otherwise a new counter readout at the next active edge of Clk would interfere with the on-going comparison. Therefore, the delay of each TFF is bounded by

$$t_{d,TFF} < \frac{T_{Clk}}{N}. \tag{6.2}$$

It is essential to design a TFF with sufficiently small delay for high resolution applications.

6.2.2 Fast Flip-flop Design

In this section, a new scheme of master-slave TFF (MSFF) is illustrated. To the best of the author's knowledge, it has a shorter clock to output (clock-Q) delay than the fastest flip-flop previously reported [19]. The new MSFF is compared with the design in [19] via

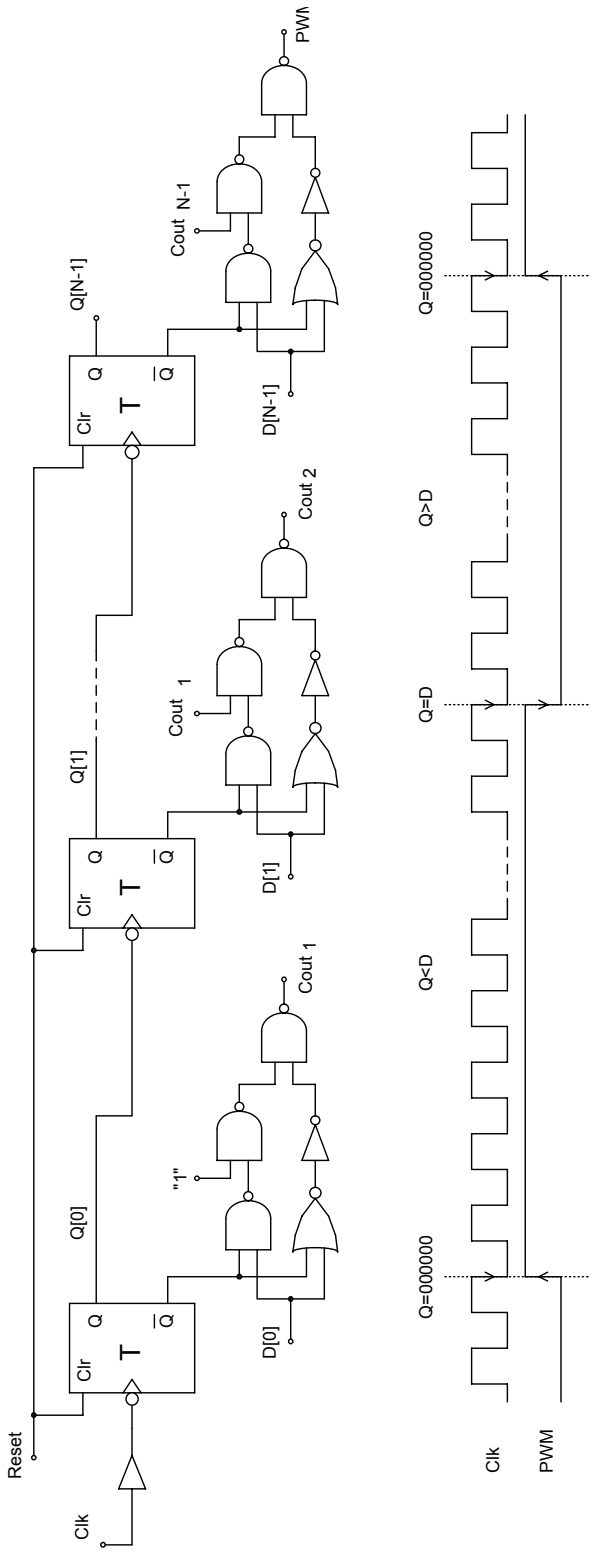


Figure 6.1: Schematic of an N-bit counter-comparator DPWM with timing diagram.

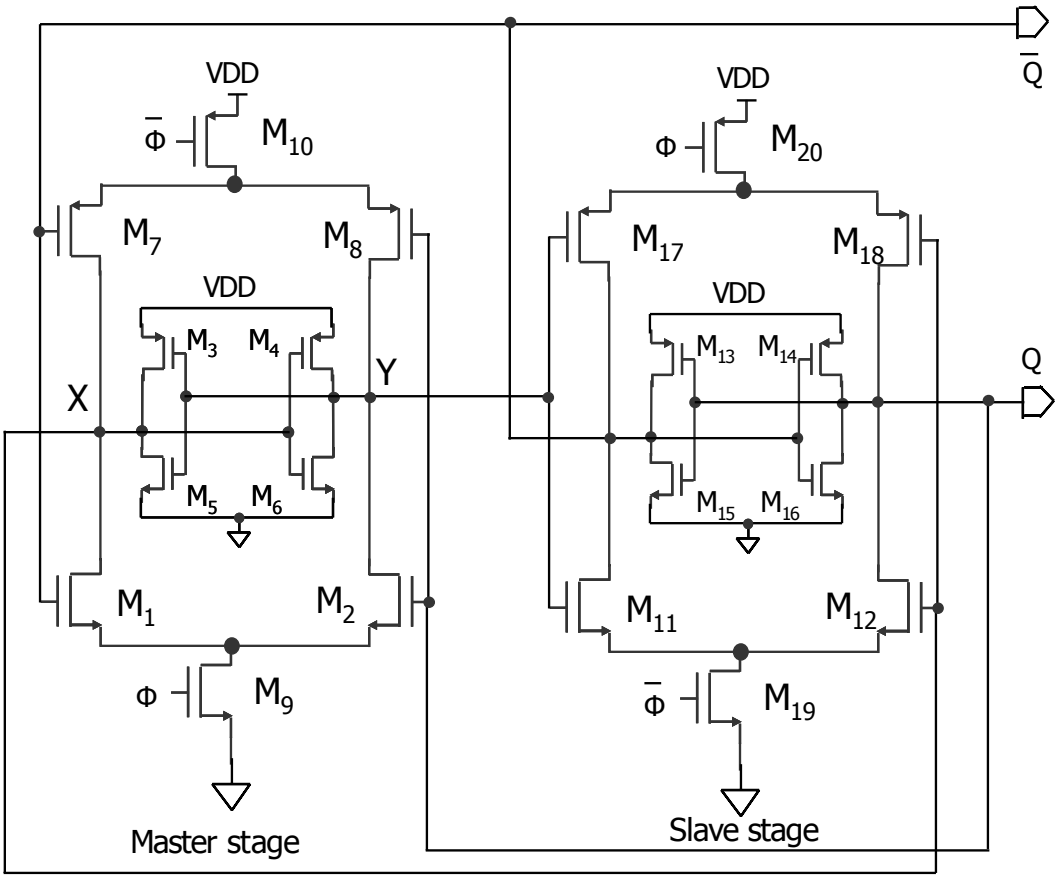


Figure 6.2: Schematic of proposed master-slave T flip-flop.

SPICE simulation. Both flip-flops are simulated on the same 0.35-μm CMOS process, with the same power consumption and layout area. The operation of the MSFF is first elaborated below. Then comparison results are presented.

The schematic of the MSFF is shown in Fig. 6.2. Assume Q is high and $\bar{Q}$ is low in the previous state. When clock Φ goes high, the master stage goes to transition mode and nodes X and Y are charged high and low, respectively, while the slave stage is in static state and holds the output logic levels. When Φ goes low, the master stage enters the static state, and

the slave stage is activated. Output Q goes low and $\bar{Q}$ goes high, and the transition of one cycle is finished. The flip-flop outputs update at the negative edge of Φ, thus this MSFF is negative edge triggered.

The master stage is one third the size of the slave stage, to optimize the speed, given a total layout area. Although a TFF is used in this application, for comparison purposes, a D flip-flop (DFF) using the same structure (without feedback from slave to master) is used in comparison with the fastest D flip-flop previously reported, the sense-amplifier based DFF (SAFF) in [19].

Table 6.1: Comparison of the MSFF and the SAFF

	MSFF	SAFF
$t_{clk,Q}$ (ps)	133	167
Total W/L	556	523
Power (mW)	0.730	0.715

Fig. 6.3 shows the delay time v.s. setup time of the MSFF compared to that of the SAFF. Delay time is also known as clk-Q time which is the time the flip-flop takes to develop valid output Q after the active edge of the clock. Setup time refers to the amount of time by which the data has to stabilize in advance of the active clock edge. If the data arrive too late and the setup time is violated, the delay time of the flip-flop will increase significantly. Table 6.1 shows a comparison of delay time, layout area (represented by total W/L of the circuit) and power dissipation between the two flip-flops. Each flip-flop is loaded with 200 fF

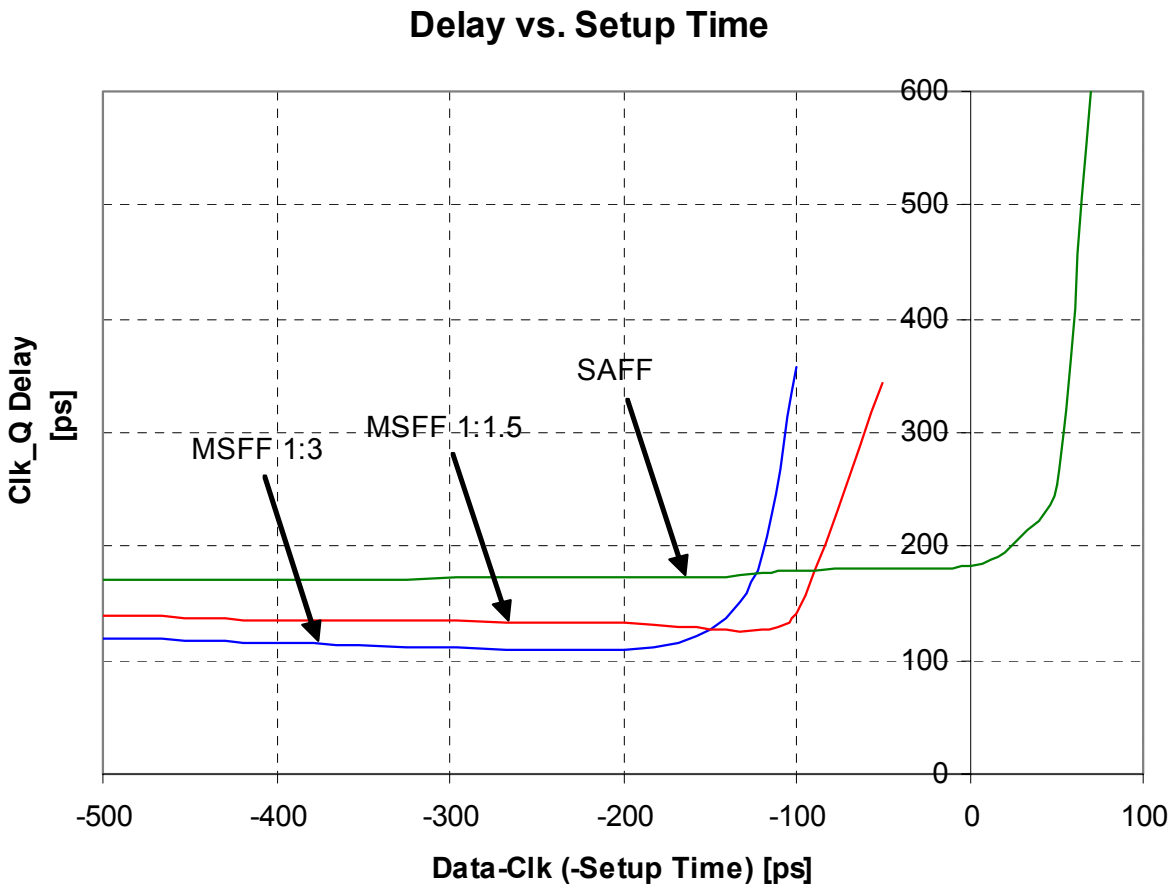


Figure 6.3: Clk-Q delay vs. setup time in the MSFF and the SAFF. For the MSFF, delay with master-slave ratio of 1:3 and 1:1.5 are presented.

capacitance on each of its differential outputs, and each circuit is simulated with 0.35-μm CMOS models with 3.3V supply voltage. The delay of the MSFF is 133 ps, while that of the SAFF is 167 ps. Thus, with comparable total layout area and power dissipation, the new MSFF has significantly shorter clk-Q delay than the SAFF.

Trade-offs between delay time and setup time for the MSFF can be seen in Fig. 6.3. When the master-slave size ratio is 1:3, the delay is 133 ps and the setup time is 150 ps. If the ratio is increased to 1:1.5, the setup time is reduced to around 100 ps but the delay

time increases to 150 ps. More simulations show that by increasing the ratio to 1:1 and by adjusting the clock for the master stage, the setup time can be further reduced to around 50ps, but at the expense of even higher clk-Q delay. The sum of setup time and delay time reaches its minimum of 210 ps at the master-slave ratio of 1.15. For applications such as the DPWM module, setup time is not a major concern. Thus, master-slave ratio of 1:3 is used to achieve small clk-Q delay.

In Fig. 6.3, trends of delay time variation can be observed as the data arrival time moves from far to close to the active clock edge. In the SAFF, the delay is constant when the data arrives much earlier than the clock, and it starts to increase when setup time is approached, which is the normal phenomenon found in most flip-flops in case of setup time violation. While in the MSFF, the delay time exhibits a decreasing trend when data arrival is pushed towards the clock edge, and then increases monotonically as setup time is violated. This is due to uncompleted capacitive coupling recovery at Q and $\bar{Q}$ when the slave stage inputs are flipped.

The delay time in Table 6.1 is measured when the data arrives 2000 ps earlier than the clock, where the delay time is invariant for both flip-flops. Thus the delay time measured under this condition is the best case for SAFF and worst case for the new MSFF. In other words, if the application pushes the data arrival closer to the clock edge than 2000 ps, the MSFF is faster and the SAFF is slower than the time shown in the table.

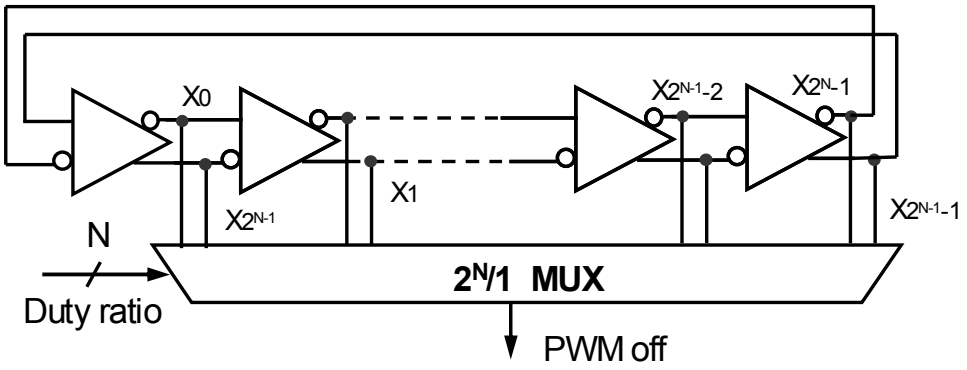


Figure 6.4: Block diagram of an N-bit ring-MUX DPWM.

6.3 Ring-MUX DPWM

An N-bit ring-MUX DPWM is illustrated in Fig. 6.4. The main components of the ring-MUX scheme are a 2^{N-1}-stage differential ring oscillator, which yields 2^N symmetrically oriented taps X_0 to X_{2^N-1}, and a $2^N/1$ MUX that can select appropriate positions from the ring.

A square wave propagates along the ring. When the rising edge reaches tap X_0 in the ring, the rising edge of the PWM signal is generated. The falling edge of this PWM signal is generated when the rising edge of the propagating square wave reaches a specified tap in the ring. The MUX is used to specify the tap in accord with the command duty cycle.

The fully differential delay stage in the ring oscillator is the same as the one used in ring-ADC in Chapter 5, which allows a ring with an even number of stages to support a stable oscillation. The use of an even number of stages permits the use of a binary number of stages (2^N), which is especially compatible with binary numbered system.

For multi-phase applications, the different phases can be tapped out from symmetric

positions on the differential ring. Two MUX's, with 4-phase MSBs each, can be used in an interleaved manner, in conjunction with a differential ring oscillator, to generate the PWM signals for the multiple phases. In each switching period, a new duty cycle command $D(n)$ is applied to one of the MUX's while the other one is holding the previous value $D(n-1)$ to ensure correct PWM signal generation for all phases. In general, two MUX's are sufficient for updating D in a multi-phase application.

The ring oscillator in the DPWM provides the clock for the entire digitally controlled buck converter system. As in the ring-ADC, the frequency of the ring oscillator in the DPWM can be controlled by adjusting the supply current to the entire ring.

The ring-MUX DPWM module for the cellular phone application has a 5-bit hardware resolution, and takes 2 μA at 1 MHz frequency. This module is integrated and tested with the entire digital controller, and is not tested individually. Instead, the test data of an 8-bit ring-MUX DPWM for a voltage regulation module (VRM) application is presented here. This 8-bit DPWM has been fabricated and tested on the same 0.25-μm CMOS process, the die photo of which is shown in Fig. 6.5. Instead of using a flat MUX, a binary-tree MUX is used because of its smaller transistor count and smaller area. The current drawn by the entire chip comprising the ring oscillator and the MUX is 10μA at 1MHz. The waveforms of the complementary outputs of one of the stages for operation at 1MHz are shown in Fig. 6.6(a). Fig. 6.6(b) shows the LSB resolution of 4 ns for 1MHz operation.

In the DPWM chip, only the fundamental oscillation frequency has ever been observed, although in principle, a ring oscillator can support more than one oscillation pattern, de-

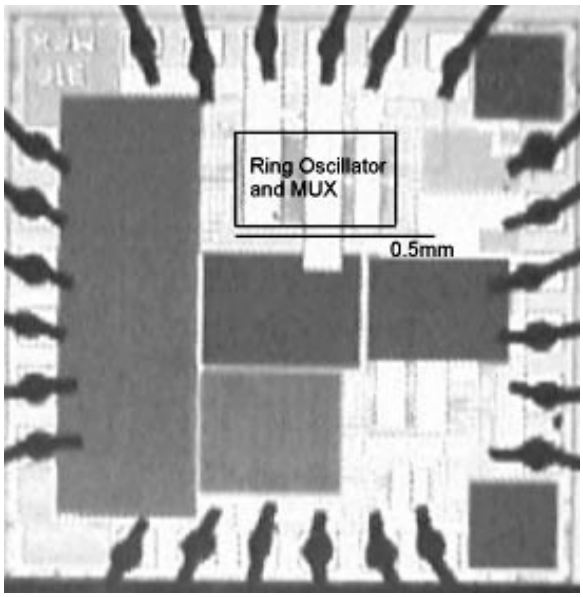
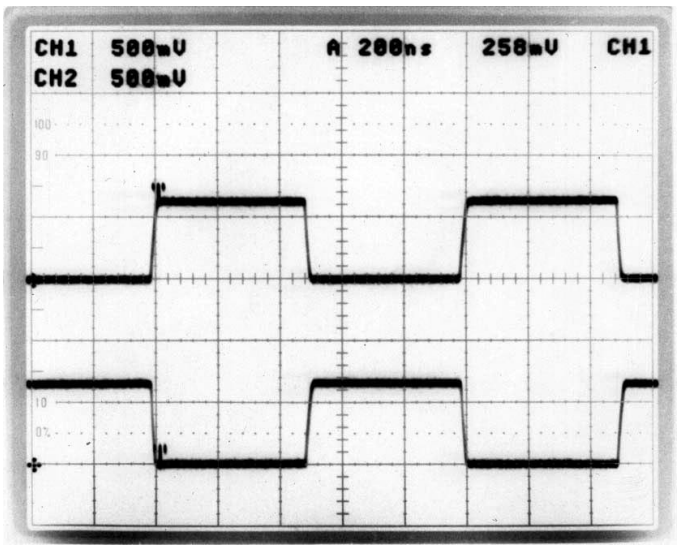


Figure 6.5: Die photo of an 8-bit ring-MUX DPWM test chip in 0.25-μm CMOS process.

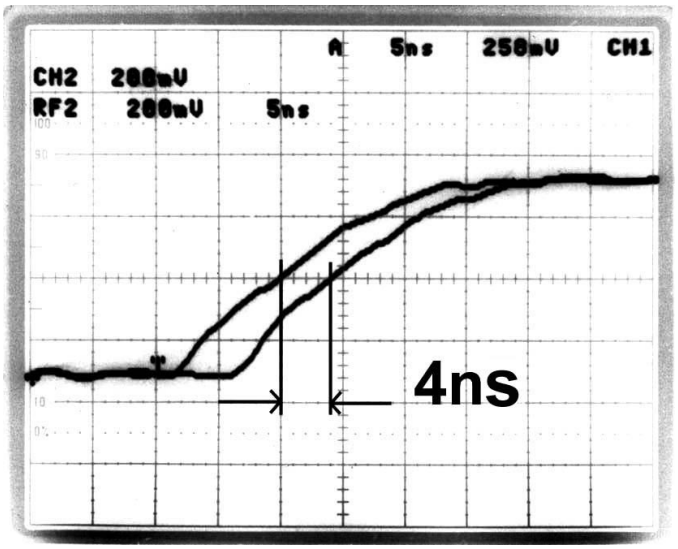
pending upon initial condition. The quasi-square wave at the fundamental frequency is the only desirable pattern. As shown in Chapter 7, the dynamics are such that only the fundamental mode is stable. This result has never been contradicted experimentally.

6.4 Comparison between the Two DPWM Schemes

Table 6.2 compares the counter-comparator scheme and the ring-MUX scheme. Each DPWM scheme has 8-bit resolution and a switching frequency of 1MHz, and is implemented with 0.25-μm CMOS process. The die area and current consumption data of the ring-MUX scheme is achieved experimentally, and that of the counter-comparator is based on simulation. It is clear that the counter-comparator scheme employs a fast clock, which results in excessive power consumption.



(a)



(b)

Figure 6.6: Experimental waveforms of a 8-bit ring-MUX scheme (a) differential output of one ring oscillator delay stage, the two waveforms are taken from the complimentary taps of the same stage with the vertical scale being 500 mV/div, and horizontal scale being 200 ns/div, (b)resolution between two adjacent outputs is 4 ns at 1 MHz oscillation frequency.

In case of high resolution DPWM hardware, a combined scheme of ring-MUX and counter-comparator can be used to get a compromise between die area and power consumption.

Table 6.2: Comparison of the counter-comparator scheme and the ring-MUX scheme.

Schemes	Main clock (MHz)	Area (μm^2)	Current consumption (μA)	Hardware sharing in multi-phase
Counter-comparator	256	300x250	2000	Low
Ring-MUX	1	350x240	10	High

Chapter 7

Thermal Noise and Ring Oscillator Stability

Ring oscillators are widely used in circuit design as clock generators and as speed testers. In both applications, a stable fundamental oscillation frequency is required to guarantee correct performance and precise measurement. However, the stability problem of ring oscillators has not gotten as much attention as the frequency stability problem of jitter and phase noise [3]. In this chapter, the stability of ring oscillators is discussed. A hypothesis to explain the stabilization process is presented based on the statistics of thermal noise. For simplicity, a single-ended digital ring oscillator is used for analysis.

7.1 Oscillation Patterns in Ring Oscillators

As shown in Fig. 7.1, a single-ended ring oscillator is composed of an odd number of inverter stages. The oscillation period T of an N-stage oscillator is given by [20]

$$T = 2 \cdot t_p \cdot N, \tag{7.1}$$

where t_p is the propagation delay of each inverting stage. The factor 2 results from the observation that a full cycle requires both a low-to-high and a high-to-low transition. The oscillation of the ring can be understood as a transitional edge propagating in the chain. Without losing generality, assume a positive edge initiates at the input of the first inverter. When the edge propagates to the end of the chain, it becomes a negative edge because of the odd number of inverting stages. The negative edge will propagate again along the chain, until it reaches the input of the first stage again with flipped polarity.

Assume each stage has a unit delay. Let X be the state vector of the oscillator, then

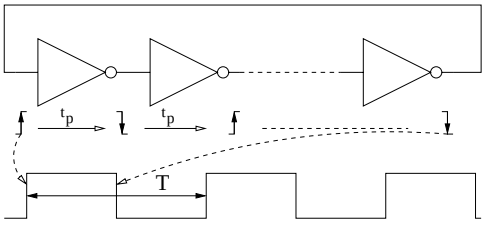


Figure 7.1: Single-ended ring oscillator with fundamental oscillation mode

each of the N variables in $\mathbf{X}$ corresponds to the state of one stage in the oscillator. Each variable has value of 1 or -1 corresponding to the respective value, high or low. Then, the N-stage oscillator can be modeled by a difference equation

$$\mathbf{X}(m+1) = \begin{bmatrix} 0 & \dots & \dots & 0 & -1 \\ -1 & 0 & \dots & \dots & 0 \\ 0 & -1 & 0 & \dots & 0 \\ \dots & \dots & \dots & \dots & \dots \\ 0 & \dots & 0 & -1 & 0 \end{bmatrix} \cdot \mathbf{X}(m) \tag{7.2}$$

where m is the discrete time variable, corresponding to uniform sampling at the rate of $1/t_p$.

Let $\mathbf{A}$ be the matrix in (7.2), the N eigenvalues are uniformly distributed on the unit circle, with values

$$\lambda_l = e^{j(2l+1)\pi/N}, \quad l = 0, 1, 2, \dots, N-1 \tag{7.3}$$

The solution of the difference equation for the oscillator is

$$\mathbf{X}(m) = A^m \mathbf{X}(0). \tag{7.4}$$

Since $\mathbf{A}$ satisfies

$$\mathbf{A^{2N}} = \mathbf{I}, \tag{7.5}$$

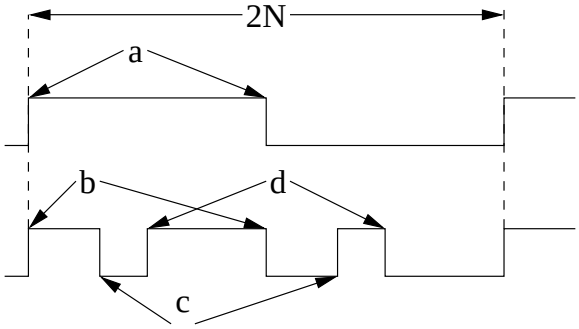


Figure 7.2: Possible oscillation patterns in a ring oscillator. The upper waveform is the fundamental pattern with the period of $2N$, where "a" denotes the one pair of transition edge. The lower waveform is a pattern with 3 pairs of transition edges, where "b", "c" and "d" denote the three pairs of edges.

for any $\mathbf{X}(0)$, $\mathbf{X}(2N) = \mathbf{A^{2N}X}(0) = \mathbf{X}(0)$. It is clear that all initial condition in the oscillator can lead to a possible stable oscillation pattern with period T=2N. It is shown below that only odd numbers of transitions can exist in each half period of N unit delays. The pattern with one transition in half the period is called the fundamental pattern. Fig. 7.2 plots the fundamental pattern and a pattern with 3 transitions. A spice simulation showing a ring oscillator supporting both fundamental and 3-transition non-fundamental patterns is given in Fig. 7.3.

Assume a ring oscillator with N=2k+1 stages, where k is a positive integer, can support i transitions in each half period, where i is an even integer. Let $i = 2l$, where l is an integer and $l \leq k$. Then there are the i number of stages, the output of which will flip in the next discrete time unit. The values of 1 and -1 still denote the high and low voltage on delay stages, respectively. Since each delay stage is an inverting stage, a transition is marked by having two successive stages with the identical output sign. At any instant, there is at least one output in the ring, the output of which is not going to flip in the next

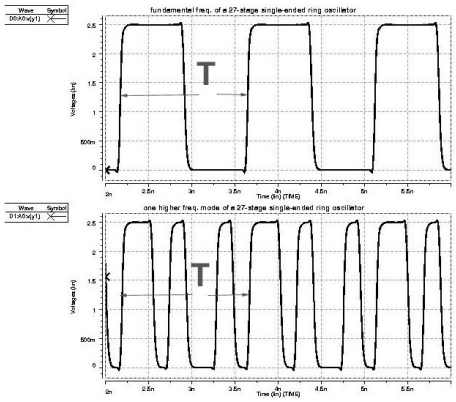


Figure 7.3: Simulation results showing fundamental pattern and multi-transition pattern in a ring oscillator.

discrete time unit. Choose such a stage as stage one. Then from stage one to stage N, there are $N - i = 2(k - l) + 1$ outputs that are not flipping in the next discrete time unit. In other words, from stage one to stage N, the number of the non-transition inverting stages is $2(k-l)+1$, which is an odd number. Thus, the output of stage N must be the same as stage one, creating a transition on the output of stage one in the next discrete time unit. Clearly, this contradicts with the assumption that the output of stage one is not flipping in the next discrete time unit. Therefore, the initial assumption does not hold, and a single-ended ring oscillator can only support oscillation with odd number of transitions in each half period. Similar conclusion holds for differential ring oscillators.

In experiments, only the fundamental pattern is found. A hypothesis to explain that the fundamental pattern is the only stable pattern is given below, based on clock jitter due to thermal noise.

7.2 Thermal Noise and Clock Jitter in Ring Oscillators

The uncertainty of spacing between clock edges, which is caused by noise in the transistor current during transition, is known as clock jitter. The clock jitter in a ring oscillator increases with measurement interval ΔT, as illustrated in Fig. 7.4 [3]. Thermal noise is considered to be white and clock jitter due to thermal noise is considered to be a random variable with Gaussian distribution. The standard deviation of the clock jitter due to thermal noise after ΔT seconds is [21]

$$\sigma_{\Delta T} = \kappa\sqrt{\Delta T}, \tag{7.6}$$

where κ is a proportional constant determined by circuit parameters and bias conditions. For a single-ended ring oscillator with identical stages, the expression for κ is given by [3]

$$\kappa \approx \sqrt{\frac{8}{3\eta}} \cdot \sqrt{\frac{kT_t}{P} \cdot \frac{V_{DD}}{V_{char}}}, \tag{7.7}$$

where η is a constant that equals the ratio of the delay and the rise time of each stage, T_t is the temperature, P is the overall power consumption of the ring oscillator, and V_{char} is a characteristic voltage of the device. For short-channel devices, $V_{char} = E_c L/\gamma$, where E_c is the critical electric field defined as the value of electric filed resulting in half the carrier velocity expected from low field mobility, L is the channel length, and γ is a phase noise coefficient.

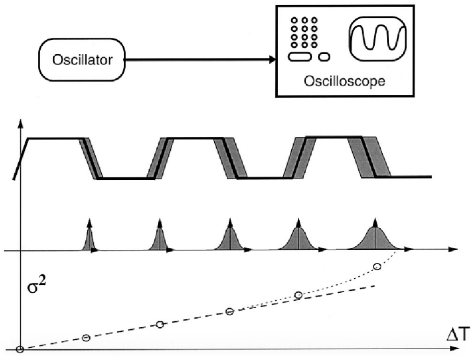


Figure 7.4: Clock jitter increasing with time [3]

7.3 Thermal Noise and Stability of Ring Oscillator

Assume a ring starts oscillation with 3 transition edges, as shown in the lower waveform in Fig. 7.2. Each edge propagates independently, and is subject to accumulating clock jitter. Without loss of generality, two adjacent transition edges are the rising edge of d and the falling edge of b, known as edge 1 and edge 2 respectively. Let Δ_{12} be the spacing between the two. Since the clock jitters of different edges due to thermal noise are independent Gaussian random variables, the jitter of Δ_{12} is also Gaussian and its standard deviation σ_{12} is given by

$$\sigma_{12} = \sqrt{{\sigma_1}^2 + {\sigma_2}^2} = 2\kappa\sqrt{\Delta T}, \tag{7.8}$$

where σ_1 and σ_2 are the standard deviation of edge 1 and 2, respectively.

If the accumulated jitter on Δ_{12} is less than $-\Delta_{12}$, edge 1 and edge 2 will collide and mutually annihilate. If the jitter is greater than $T/2 - \Delta_{12}$, one of the edges would run into the third transition edge in the oscillator. Since any two adjacent edges in the oscillator

are opposite in transition, in either case, only one edge would be left in the ring oscillator, resulting in the fundamental pattern.

The probability that the jitter on Δ_{12} is less than $-\Delta_{12}$, or is greater than $T/2 - \Delta_{12}$ is given by

$$P_{12} = P(jitter < -\Delta_{12}, jitter > \frac{T}{2} - \Delta_{12}) = 1 - P(-\Delta_{12} \leq jitter \leq \frac{T}{2} - \Delta_{12}). \quad (7.9)$$

Since there are originally three edges in the oscillator, P_{12} is a lower bound for the overall probability, P_{cnv}, of converging to fundamental pattern. Probability P_{12} reaches minimum $P_{12,min}$ when $\Delta_{12} = T/4$. Therefore,

$$P_{cnv} \geq P_{12,min} = 1 - \frac{1}{\sqrt{2\pi}\sigma_{12}} \int_{-\frac{T}{4}}^{\frac{T}{4}} e^{-\frac{1}{2}(\frac{x}{\sigma_{12}})^2} \, \mathrm{d}x. \quad (7.10)$$

Substituting σ_{12} in (7.10) from (7.8) and taking the limit of P_{cnv} as $\Delta T \to \infty$, results in

$$\lim_{\Delta T \to \infty} P_{cnv} = 1. \quad (7.11)$$

Equation (7.11) shows that the probability that the 3-edge oscillation pattern converges to the fundamental pattern approaches one asymptotically as ΔT increases, due to thermal noise alone. The above argument illustrates that the fundamental pattern is the only stable pattern. The same conclusion also holds for differential ring oscillators.

Chapter 8

Experimental Results and Conclusions

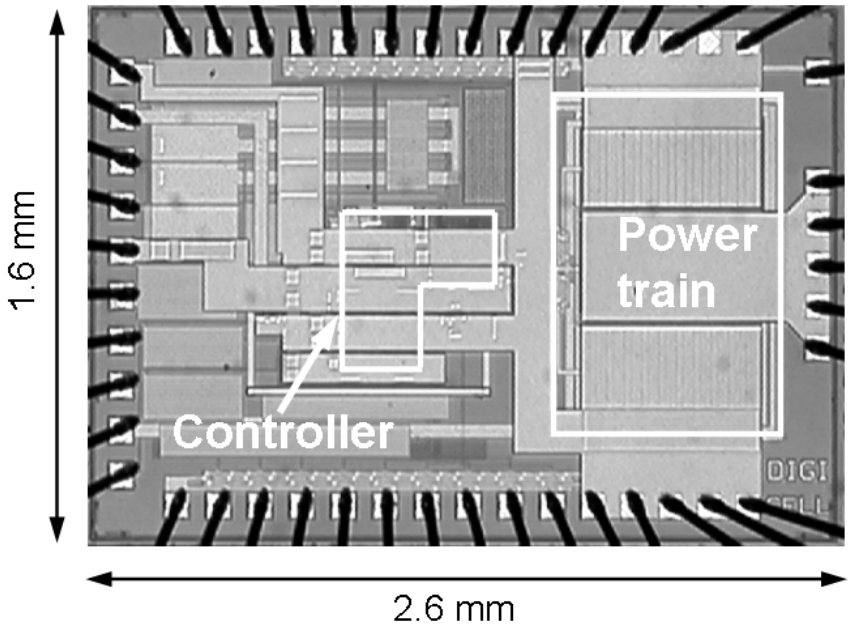


Figure 8.1: Chip micrograph.

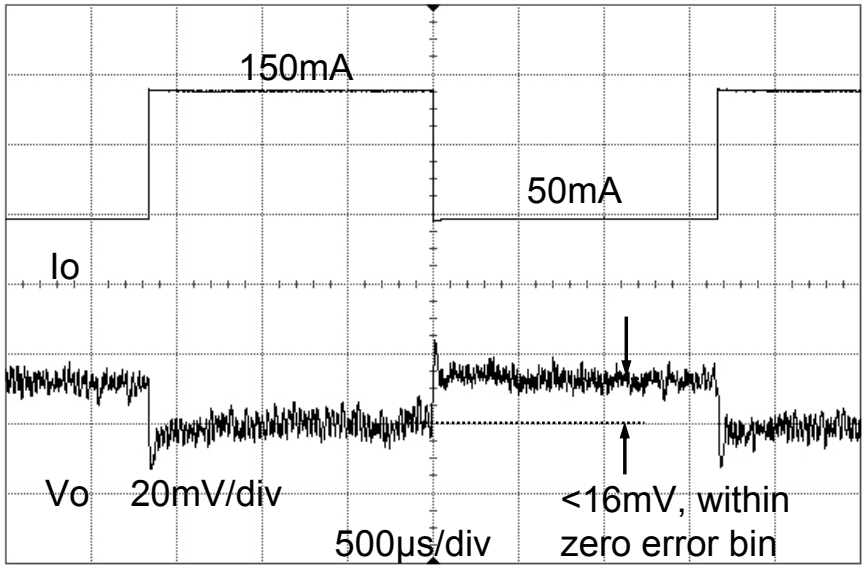
8.1 Experimental Results

The dual-mode digitally-controlled buck converter IC is implemented with a 0.25-μm CMOS N-well process. The die photo of the chip is shown in Fig. 8.1. The total chip area is $4\mathrm{mm}^2$, out of which $2\mathrm{mm}^2$ is the active area. The required pin count for the buck converter IC is 10, and all the other pins are for test purposes, only. Table 8.1 contains the description of the 10 required pins.

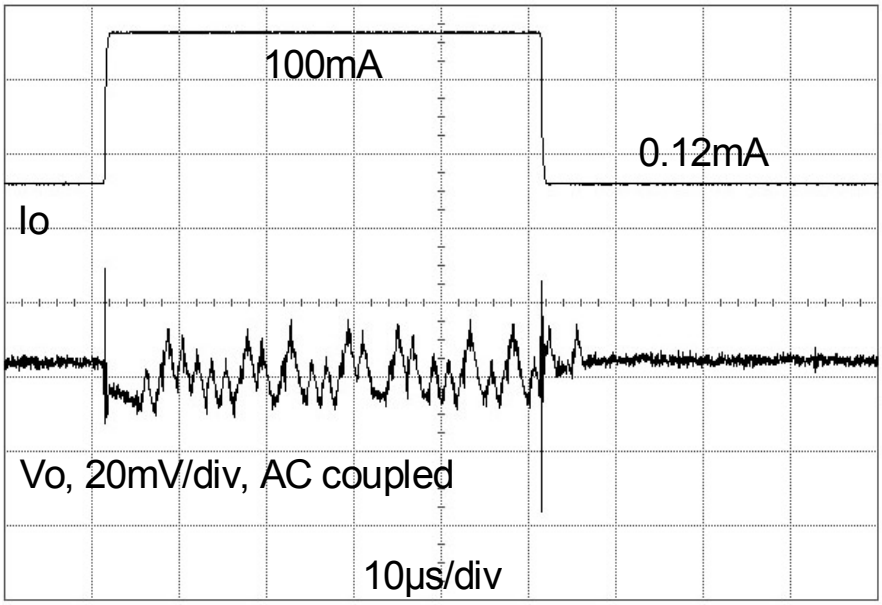
The input voltage range of the chip is 5.5-2.8 V, and the output voltage range is 1.0-1.8 V. The measured quiescent current in PFM mode with 600 kHz sampling frequency is 4 μA, compared to 15 μA in leading state-of-the-art analog controllers. In PWM mode, the DC output voltage precision over the full V_o range is $\pm 0.8\%$ with off-chip reference. The

Table 8.1: Digital controller IC pin description.

Pin Number	Pin Name	Function
1	FB	ADC input. Connect directly to Vout
2	REF	Analog voltage reference Vref
3	MP	Internal voltage level, mid-point of PVIN and PGND
4	MODE	High for PFM mode; low for PWM mode
5	EN	Enable input
6	PGND	Power ground
7	SW	Switching Node connection to internal PFET and NFET
8	PVIN	Power supply input to internal PFET switch
9	SVDD	Signal supply input
10	SGND	Signal ground



(a)



(b)

Figure 8.2: Experimental load transient response with V_{in}=3.2 V, V_o=1.2 V, L=10 μH and C=47 μF, (a) PWM mode response with f_s=1 MHz, (b) PFM mode response with f_{sample}=600 kHz.

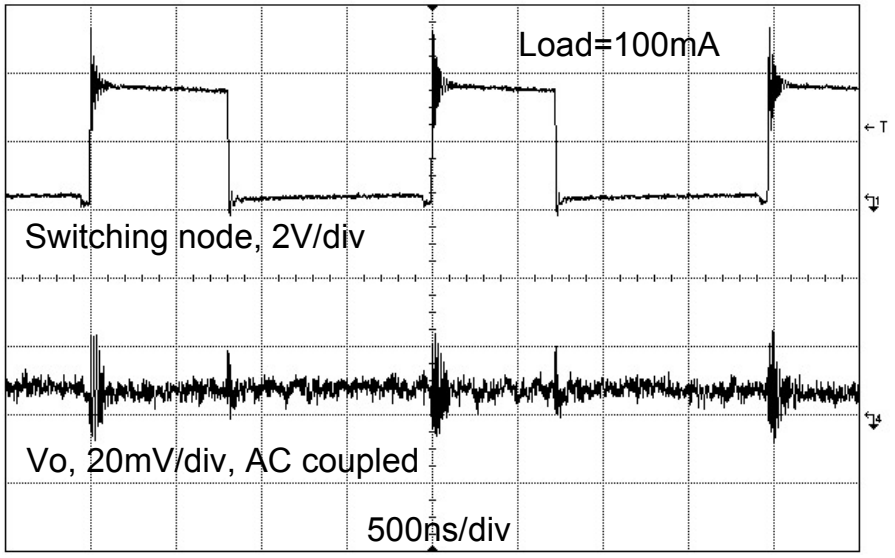


Figure 8.3: Experimental steady-state response in PWM mode with V_{in}=3.2 V, V_o=1.2 V, I_o=100 mA, L=10 μH, C=47 μF, and f_s=500 kHz.

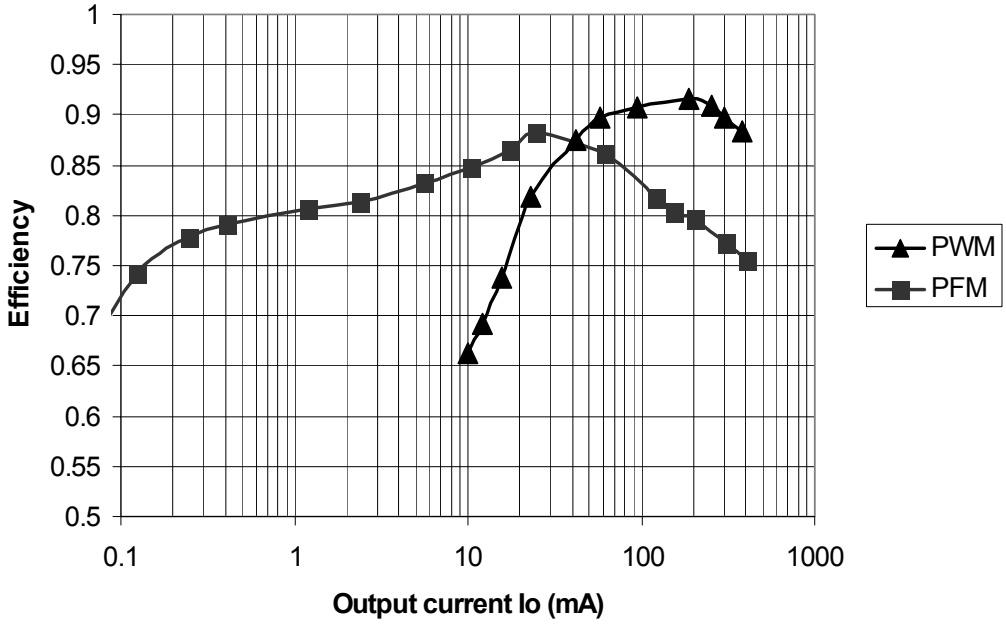


Figure 8.4: Measured PWM and PFM mode buck converter efficiency vs output current, with V_{in}=4 V and V_o=1.5 V.

PWM mode steady-state output voltage waveform is shown in Fig. 8.3. The voltage ripple at V_o is 2 mV peak to peak.

Experimental closed-loop load transient responses with load current steps of 100 mA in PWM and PFM mode are shown in Fig. 8.2(a) and Fig. 8.2(b), respectively. In PWM mode, it can be seen that the steady state DC voltages at different load levels are within the zero error bin of the ADC, which is 16 mV in this design. In PFM mode, the voltage excursion is below 20 mV when the load current is 100 mA.

The buck converter IC demonstrates safe 5.5 V operation of 0.25-μm CMOS circuitry (nominal supply voltage is 2.5 V). The power train transistors are protected from high input voltage by the cascode structure. Internal power management provides proper bias for the cascode transistors, and safe supply voltage for the control circuitry.

Converter efficiency as a function of load current in both PWM mode and PFM mode is measured with V_{in}=4 V and V_o=1.5 V, as illustrated in Fig. 8.4. An efficiency of 92$\%$ is achieved in PWM mode with load current of 189 mA. It can be observed that 40 mA is the crossover point of the PWM and the PFM efficiency curves. Thus, when load current is lower than 40 mA, the converter should be switched from PWM to PFM mode for better efficiency. Furthermore, over a 20 mA to 200 mA load current range, high efficiency (over 80$\%$) can be observed in each mode, thus it is easy to implement a scheme to switch between the two modes due to the wide load range of overlapping high efficiency.

Table 8.2 summarizes the application and the measured performance of the IC.

Table 8.2: Chip performance summary.

Technology	0.25-μm CMOS (Max. supply 2.75 V)
Input voltage range	5.5-2.8 V
Output voltage range	1.0-1.8 V
External LC filter	L=10 μH, C=47 μF
Maximum load current	400 mA
PFM mode sampling frequency	600 kHz
PFM mode quiescent current	4 μA
PWM mode switching frequency	0.5-1.5 MHz
PWM mode DC output voltage precision	$\pm 0.8\%$
PWM mode output voltage ripple	2 mV
Active chip area	2 mm^2

Table 8.3: Comparison of LM2612 and the buck converter IC in this work.

	LM2612	This work
Controller type	Analog	Digital
Process	BJT	0.25-μm 2.5V CMOS
Output filter	L=10 μH, C=22 μF	L=10 μH, C=47 μF
DC output voltage precision [1]	$\pm 2\%$	$\pm 0.8\%$
Maximum load capability (mA)	400	400
PWM mode output voltage ripple (mV)	2	1.5
PWM mode peak efficiency	88%	92 %
Quiescent current in PFM mode (μA)	70[2]	4

8.2 Comparisons and Conclusions

Table 8.3 shows the comparison between this work and an analog commercial part with the same input/output voltage range, load current, and switching frequency, the LM2612 of National Semiconductor. It shows that the CMOS-based digital controller can have the same performance as or better performance than the analog controller, with quiescent current more than an order of magnitude lower. Even when compared to the analog controller with the lowest quiescent current TPS62200, which has, inherently, lower switching fre-

quency range, lower load current, and less DC voltage precision, the quiescent current of the digital controller is still three times lower, making it possible to extend the cellular phone standby time by up to three times.

The safe operation of the digital controller in 0.25-μm CMOS N-well process with 5.5V input voltage is made possible by using a cascode power train to protect the power transistors from high voltages, and internal power management which provides proper supply voltage for the controller circuit. Extra power saving is achieved by scavenging the charge from the high side gate drive.

8.3 Summary of Research Contributions

An ultra-low-quiescent-power dual-mode digitally-controlled buck converter IC has been designed and tested for cellular phone applications. A quiescent current of 4 μA is achieved experimentally in PFM mode, allowing cellular phone standby time to be extended by up to three times compared to the leading state-of-the-art analog controller. Through side-by-side comparison with an analog controller with the same specifications, it has been shown that digital controllers can achieve equal or better performance with much lower quiescent current.

Internal power management, a new architecture that allows a controller to be implemented with a low voltage process and to safely operate with high input voltage, is intro-

[1]The LM2612 has on-chip references while in this work an off-chip references is used.

[2]The quiescent current on the LM2612 data sheet is 150μA, including the on-chip references and current overload protection. The 70μA is the quiescent current suggested by the designer of LM2612 excluding these features so that a fair comparison can be made.

duced. New modules developed for the digital controller include an averaging windowed ring-ADC which is nearly entirely synthesizable and is robust against noise, and an ultra-low-power ring-MUX DPWM which also serves as clock generator for the whole system. Other cells that are of general interest such as zero-DC-current comparators and an ultra-fast flip-flop are also developed.

This work demonstrated sub-threshold operation of CMOS transistors as a viable, very low power option for analog-digital interface elements. Furthermore, with the chip implemented in a digital CMOS process, the possibility of integrating the power management unit with other digital system on the same die is demonstrated, which can achieve significant cost reduction. The work illustrates the promise of digital power management IC's as a high performance, low power, and small area alternative to analog controllers, using a combination of digital processing and special purpose analog-digital interface structures.

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Appendix A

Output Voltage Ripple Calculation for Buck Converter in Continuous Conduction Mode

The capacitance-dominant output voltage ripple of a buck converter in continuous conduction mode has been given in Chapter 3. In this appendix, the output voltage ripple due to both the output capacitor and its equivalent series resistance (ESR) is calculated.

Assume the converter has an input voltage V_{in}, an output voltage $V_o(t)$ with average value of V_o, a steady-state duty ratio D, an output current I_o, and an inductor current $I_L(t)$ with peak to peak ripple ΔI_L. And the output filter is composed of inductor L and capacitor C with ESR of value R. Let time $t = 0$ when the inductor current i_L reach its minimum. The converter has a switching period of T, then the on-time of the PWM signal is DT. Voltage ripple ΔV_o can be calculated with Fig. A.1.

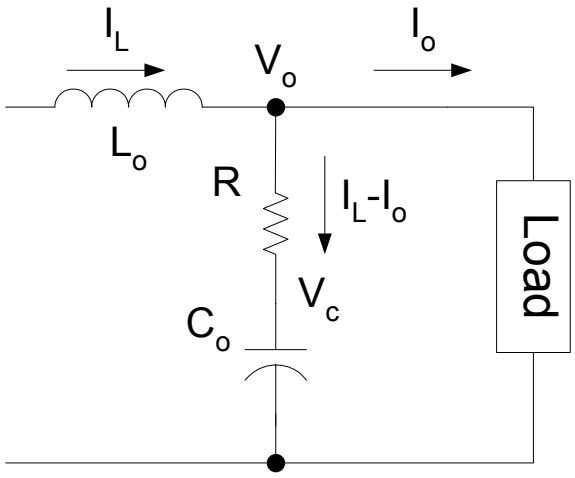
In each switching cycle, the inductor current can be divided into ramping up region A and ramping down region B respectively, as shown in Fig.A.1(b). During $t \in [0, T)$ I_L can be represented by the following equation

$$I_L(t) = \begin{cases} k_1 t + b_1 & \text{for} \quad t \in [0, DT), \\ k_2(t - DT) + b_2 & \text{for} \quad t \in [DT, T). \end{cases} \tag{A.1}$$

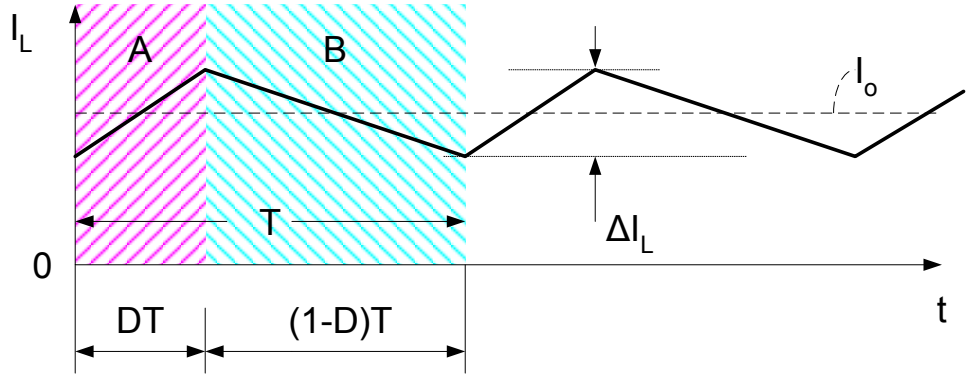
Using conditions $I_L(0) = I_o - \frac{1}{2}\Delta I_L$ and $I_L(DT) = I_o + \frac{1}{2}\Delta I_L$, k_1, b_1, k_2, b_2 can be solved

$$\begin{cases} k_1 = \frac{\Delta I_L}{DT}, \\ b_1 = I_o - \frac{1}{2}\Delta I_L, \end{cases} \tag{A.2}$$

$$\begin{cases} k_2 = -\frac{\Delta I_L}{(1-D)T}, \\ b_2 = I_o + \frac{1}{2}\Delta I_L. \end{cases} \tag{A.3}$$



(a)



(b)

Figure A.1: Buck converter in continuous conduction mode (a) schematic, (b) inductor current waveform.

Let $V_C(0)$ be the voltage across the capacitor when $t = 0$, $\Delta V_C(t) = V_C(t) - V_C(0)$ be the voltage change on capacitor from time 0 to time t, and $V_R(t)$ be the voltage drop on R. The output voltage at time t is the sum of $V_C(0)$, $\Delta V_C(t)$, and $V_R(t)$, namely

$$V_o(t) = V_C(0) + \frac{1}{C}\int_0^t (I_L(t) - I_o)dt + (I_L(t) - I_o)R, \qquad \text{for} \quad t \in [0, DT) \tag{A.4}$$

Combining (A.1) through (A.3) and (A.4), the piece wise linear expression of $V_o(t)$ is

$$V_o(t) = \begin{cases} V_C(0) + \frac{1}{C}\int_0^t (\frac{\Delta I_L}{DT}t - \frac{1}{2}\Delta I_L)dt + (\frac{\Delta I_L}{DT}t - \frac{1}{2}\Delta I_L)R \\ \qquad\qquad\qquad\qquad\qquad\qquad \text{for} \quad t \in [0, DT), \\ V_C(DT) + \frac{1}{C}\int_{DT}^t (-\frac{\Delta I_L}{(1-D)T}t + \frac{\Delta I_L}{2}\frac{1+D}{1-D})dt + (-\frac{\Delta I_L}{(1-D)T}t + \frac{\Delta I_L}{2}\frac{1+D}{1-D})R \\ \qquad\qquad\qquad\qquad\qquad\qquad \text{for} \quad t \in [DT, T). \end{cases} \tag{A.5}$$

To find V_{omin}, taking the derivative of first part in (A.5) and making it equal to zero, results in

$$\frac{dV_o(t)}{dt} = \frac{1}{C}\frac{\Delta I_L}{DT}t - \frac{1}{2C}\Delta I_L + \frac{\Delta I_L}{DT}R = 0, \qquad \text{for} \quad t \in [0, DT). \tag{A.6}$$

Solving (A.6) for t, it can be found

$$t = \frac{1}{2}DT - RC. \tag{A.7}$$

Define $\tau_o = RC$, which is the time constant of the output capacitor. The expression for t can be rewritten as

$$t = \frac{1}{2}DT - \tau_o. \tag{A.8}$$

Combining the constraint $t \in [0, DT)$ and (A.8) gives

$$t_{omin} = \begin{cases} \frac{1}{2}DT - \tau_o & \text{for} \quad \tau_o < \frac{1}{2}DT, \\ 0 & \text{for} \quad \tau_o \geq \frac{1}{2}DT. \end{cases} \tag{A.9}$$

Therefore,

$$V_{omin} = \begin{cases} V_o(\frac{1}{2}DT - \tau_o) = V_C(0) - \frac{\Delta I_L}{8C}DT - \Delta I_L R\frac{\tau_o}{2DT} & \text{for} \quad \tau_o < \frac{1}{2}DT, \\ V_o(0) = V_c(0) - \frac{\Delta I_L}{2}R & \text{for} \quad \tau_o \geq \frac{1}{2}DT. \end{cases} \tag{A.10}$$

Similarly, V_{omax} can be calculated by making the derivative of second part in (A.5) equal to zero,

$$\frac{dV_o(t)}{dt} = -\frac{1}{C}\frac{\Delta I_L}{(1-D)T}t + \frac{\Delta I_L}{2C}\frac{1+D}{1-D} - \frac{\Delta I_L}{(1-D)T}R = 0, \qquad \text{for} \quad t \in [DT, T). \tag{A.11}$$

Solving (A.11) for t, the following expression can be derived

$$t = \frac{1}{2}(1+D)T - \tau_o. \tag{A.12}$$

Combining constraint $t \in [DT, T)$ with (A.12) gives

$$t_{omax} = \begin{cases} \frac{1}{2}(1+D)T - \tau_o & \text{for} \quad \tau_o < \frac{1}{2}(1-D)T, \\ DT & \text{for} \quad \tau_o \geq \frac{1}{2}(1-D)T. \end{cases} \tag{A.13}$$

Thus

$$V_{omax} = \begin{cases} V_o(\frac{1}{2}(1+D)T - \tau_o) = V_C(0) + \frac{\Delta I_L}{8C}(1-D)T + \frac{\Delta I_L}{2C}\frac{\tau_o^2}{(1-D)T} \\ \qquad\qquad\qquad\qquad\qquad\qquad \text{for} \quad \tau_o < \frac{1}{2}(1-D)T, \\ V_o(0) = V_c(0) + \frac{\Delta I_L}{2}R \\ \qquad\qquad\qquad\qquad\qquad\qquad \text{for} \quad \tau_o \geq \frac{1}{2}(1-D)T. \end{cases} \tag{A.14}$$

If the duty ratio $D < 50\%$,

$$min(\frac{1}{2}DT, \frac{1}{2}(1-D)T) = \frac{1}{2}DT. \tag{A.15}$$

The output voltage ripple $\Delta V_o = V_{omax} - V_{omin}$ is

$$\Delta V_o = \begin{cases} \frac{\Delta I_L T}{8C} + \Delta I_L R\frac{\tau_o}{2T}(\frac{1}{1-D} + \frac{1}{D}) & \text{for} \quad \tau_o \leq \frac{1}{2}DT, \\ \frac{\Delta I_L}{8C}(1-D)T + \Delta I_L R\frac{\tau_o}{2(1-D)T} + \frac{\Delta I_L}{2}R & \text{for} \quad \frac{1}{2}DT < \tau_o \leq \frac{1}{2}(1-D)T, \\ \Delta I_L R & \text{for} \quad \tau_o > \frac{1}{2}(1-D)T. \end{cases} \tag{A.16}$$

To summarize, if the duty ratio $D \geq 50\%$

$$\Delta V_o = \begin{cases} \frac{\Delta I_L T}{8C} + \Delta I_L R\frac{\tau_o}{2T}(\frac{1}{1-D} + \frac{1}{D}) & \text{for} \quad \tau_o \leq \frac{1}{2}(1-D)T, \\ \frac{\Delta I_L}{8C}DT + \Delta I_L R\frac{\tau_o}{2DT} + \frac{\Delta I_L}{2}R & \text{for} \quad \frac{1}{2}(1-D)T < \tau_o \leq \frac{1}{2}DT, \\ \Delta I_L R & \text{for} \quad \tau_o > \frac{1}{2}DT. \end{cases} \tag{A.17}$$

To verify the special case when the ESR is zero, let $R = 0$, then $\tau_o = 0$. Both (A.16) and (A.17) give the same result as (3.5).