# A Soft-Switched Constant-Frequency Square-Wave Half-Bridge DC-DC Converter

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*Abstract*— **This paper introduces a constant-frequency zero-voltage-switched square-wave DC-DC converter, and presents results from experimental half-bridge implementations. A saturable magnetic element produces the advantageous square waveforms, and provides isolated terminals from which the output voltage may be controlled. Semiconductor stresses and losses are minimized both by the square waveforms and by low switching losses. The active switches and the output rectifiers both exhibit zero-voltage switching. The active switches (MOSFET's) are operated at a fixed frequency with 50% duty cycle, which allows the use of a simple self-oscillating gate drive. An experimental implementation achieves over 80% efficiency at approximately 70 W/in$^3$.**

## I. Introduction

This paper introduces a constant-frequency zero-voltage-switched square-wave DC-DC converter. Half-bridge versions of the circuit have been experimentally implemented. The circuit is built with a saturating magnetic element that provides a mechanism to effect both soft switching and control. The square current and voltage waveforms result in low voltage and current stresses on the primary switch devices and on the secondary rectifier diodes, equal to those in a standard half-bridge pulse-width modulated (PWM) converter. The primary active switches and the output rectifiers exhibit zero-voltage switching. The output rectifier circuit does have small switching losses due to the leakage inductance between the two secondary windings on the output transformer, but this may be kept very small. The $V$-$A$ rating, and hence physical size, of the saturable reactor is small. The rating of this device is a fraction of that of the transformer in an isolated circuit. The active switches (MOSFET's) are operated at a fixed frequency with 50% duty cycle. Control can be effected by varying the current in an auxiliary winding on the saturable reactor. Due to the simple open-loop nature of the gate drive pattern, our prototype has been built with a self-oscillating gate drive.

A plethora of soft-switched and/or resonant converter circuits have emerged over the last ten years. To the best of the authors' knowledge, there is no constant-frequency soft-switched half-bridge circuit featuring square current waveforms and simple control. We believe this circuit will be of use where power levels cannot justify use of a full bridge configuration. In addition, the control and gate drive scheme is considerably simpler than that used in other soft-switched full-bridge converters. A number of authors [1, 2, 3, 4] have reported on soft-switched full-bridge circuits that rely on phase-shifting between the legs of the bridge for control. A potential difficulty with this class of circuits is with the complexity of the gate drive timing. In particular, commutation is achieved via the ringing of leakage inductance (or an auxiliary commutating inductor) and switch capacitance. Careful timing needs to be implemented to allow for zero-voltage transitions. In any case, phase-shifting is not possible with a half-bridge configuration.

One class of circuits that has emerged in the literature [5, 6, 7] is similar to the circuit introduced in this paper. The class of circuits in [5, 6, 7] features square waveforms and zero-voltage switching for the primary switch devices. This is accomplished through the use of saturable reactors. The saturable reactors are configured differently, but serve similar functions to those in the present work. However, in the simple form of the circuits in [5, 6, 7], the secondary rectifier devices exhibit lossy turn-off transitions. In [7], these losses are controlled by the addition of a resonant inductor and capacitor on the rectifier. Nevertheless, the diode faces a large peak reverse voltage. These topologies will be compared in more detail below.

There have also been a large number of publications on soft-switched single-ended circuits. The single-ended circuits that most closely resemble the work reported here are in [8, 9]. The paper of Erickson et al. [8] used a sat-

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urable reactor to clamp a resonant current waveform in a zero-current-switched single-ended circuit. This function of a saturable reactor is similar to that of the saturable reactor in the present work.

## II. Circuit Description

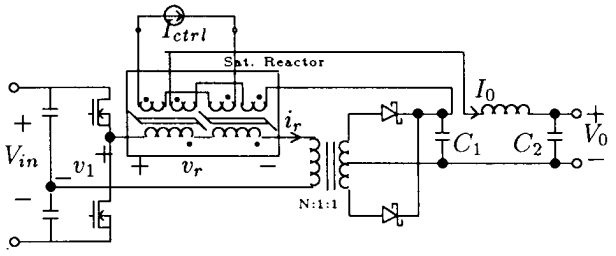


Fig. 1. Soft-switched square-wave half-bridge DC-DC converter

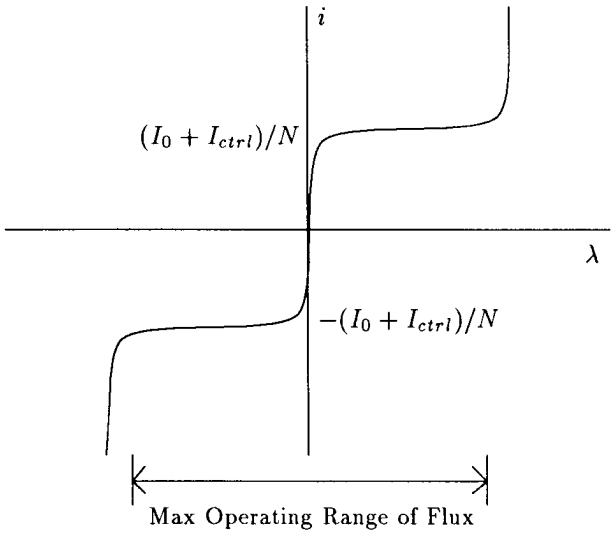


Fig. 2. Flux-current characteristic of saturating reactor

The salient element of the schematic shown in Fig. 1 is the saturable reactor. With constant secondary bias currents of $I_0$ and $I_c$, the flux-current characteristic at the primary terminals of this reactor has the form shown in Fig. 2. For this circuit, it is desirable to operate the reactor with the flux within the bounds of the indicated "maximum operating range". Within this region the characteristics resemble those of an ordinary saturating inductor, but with the current and flux switched. Instead of having the incremental inductance decrease at a saturation flux level, this reactor has the incremental inductance increase greatly when a current threshold is reached. This clamps the current in the primary winding of the reactor near this current level, equal to the sum of the secondary bias currents adjusted for the turns ratio, and thus, gives the converter its advantageous square current waveforms. In practice, the saturable reactor element is built with a pair of amorphous magnetic metal mag-amp cores available from a number of manufacturers.

The action of the saturable reactor can be viewed as follows. If the reactor is driven with a balanced square voltage waveform, one would expect to observe a balanced square current waveform that is delayed by a quarter cycle with respect to the drive waveform. The magnitude of the current waveform is determined entirely by the secondary bias currents. When inserted in the half-bridge circuit, the nonlinear reactor faces the sum of a square primary voltage waveform and a square voltage waveform reflected from the secondary. The reflected secondary voltage waveform is approximately in phase with the reactor current since the capacitor-loaded rectifier is current-controlled from the primary. Hence, ideal waveforms for the reactor are as shown in Fig. 3. As such, the reactor current always lags the voltage squarewave applied by the active half-bridge, and zero-voltage switching is readily effected.

Since the secondary rectifier is current-fed and capacitor-loaded, it also exhibits zero-voltage transitions, as long the two secondary windings are tightly coupled. This is not unlike the rectifier switching behavior in a capacitor-loaded series resonant converter. Fortunately, the rectifier load capacitor only handles short-duration transient currents that are generated during the commutation of the saturable reactor and rectifier combination.

Our implementation is built around a self-oscillating gate drive. In this scheme, the upper MOSFET is held on for a fixed duration $T/2$ while the lower MOSFET is held off. After this duration, the upper device is turned off. After the current in the nonlinear reactor commutates the capacitance at the inverter node, the lower MOSFET gate drive circuit detects that the voltage has collapsed on the lower MOSFET, and immediately turns this device on for a complementary fixed duration $T/2$. As such, the conduction time for the MOSFET body diodes is minimized or eliminated. While the lower MOSFET is held on, the current in the nonlinear reactor switches polarity. The turn-off of the lower MOSFET occurs in an analogous manner to that of the upper MOSFET. Consequently, the primary side control is simply built around two independent self-timed gate drive circuits. It is not necessary to couple signals between the two drive circuits. A simple start-up circuit is needed and incorporated, however. Our implementation uses a simple commercially-available gate drive IC in combination with two CMOS NAND gates. Each gate drive section could easily be integrated into a single simple IC. Fig. 4 illustrates the overall organization of the gate drive scheme.

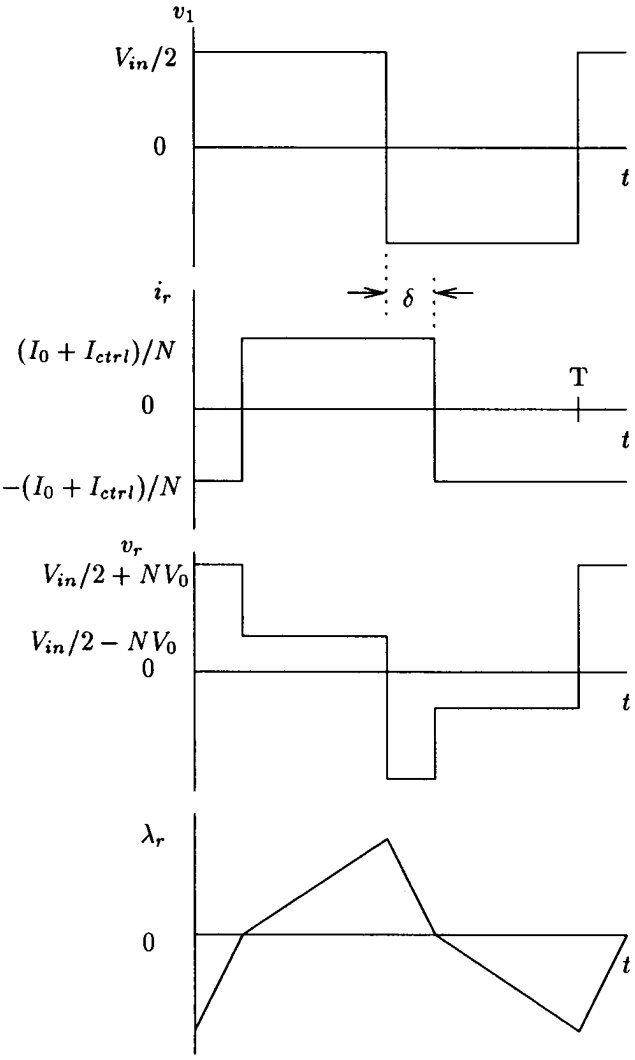


Fig. 3. Ideal circuit waveforms

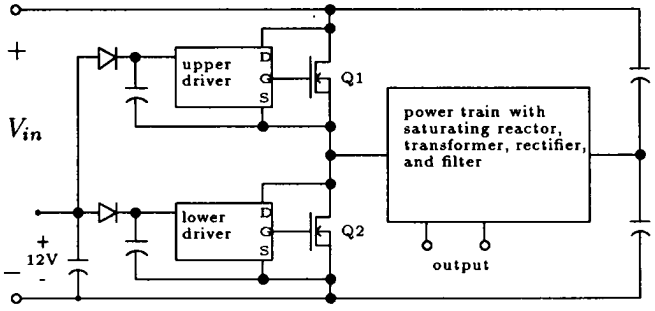


Fig. 4. Organization of the gate drive

The control of the output voltage or current is effected by controlling the current in a secondary winding on the nonlinear reactor, and hence, there is no need for any additional control mechanism in the active bridge circuit. The control can be understood by considering that in steady state the voltage on the two secondary capacitors must be equal. The current charging capacitor $C_1$ is ideally equal to $|Ni_r| - I_0$. Since the saturable reactor serves to clamp the transformer primary current to plus or minus $(I_0 + I_{ctrl})/N$, the net charging current for $C_1$ is ideally equal to the control current $I_{ctrl}$, and the output voltage is ideally the integral of the control current, divided by the value of $C_1$. In practice, some DC control current is necessary to maintain $C_1$ at the desired voltage. This steady-state current in the control winding compensates for the current needed to charge and discharge the capacitance of the output rectifiers during commutation of the reactor current, the magnetizing current of the transformer, and the deviations of the saturable reactor characteristics from ideal, square, single-valued $\lambda - i$ characteristics.

The action of the control can also be viewed from the standpoint of voltage and flux in the saturable reactor. As discussed above, the saturable reactor serves to introduce a delay between the driving voltage square wave and the transformer primary voltage square wave. From considering the reactor flux, $\lambda_r$, it is apparent that when the output voltage is adjusted via the control current, the delay, $\delta$, adjusts such that the constraint

$$(V_{in}/2 + NV_0)\delta = (V_{in}/2 - NV_0)(T/2 - \delta) \qquad (1)$$

is satisfied. Hence, voltage regulation is accompanied by phase shift between inverter voltage and primary current.

We are now prepared to compare the present circuit with the similar circuit of [5, 6, 7], shown in Fig. 5. The saturating reactors in both circuits serve to delay the current reversal in the primary. However, in the circuit of Fig. 5, the reactors do not serve to clamp the current waveform and force it to be square. Thus connecting a capacitor directly to the output of the rectifiers is not possible, as it would result in current pulses following each commutation. The necessity of omitting a capacitor at this node results in higher diode switching losses, accompanied by higher peak diode voltage, due to ringing. Although these losses can be controlled by the addition of a resonant inductor and capacitor [7], that is unnecessary in the present circuit, shown in Fig. 1. Furthermore, the circuit fo Fig. 1 results in low peak reverse diode voltage.

## III. Averaged Circuit Model

Based on the above discussion, an approximate averaged circuit model can be developed for the purpose of

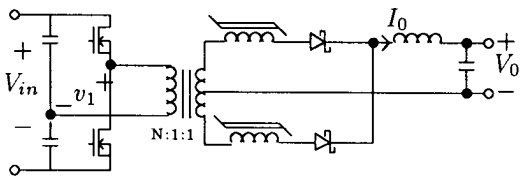


Fig. 5. A similar circuit.

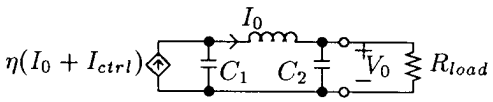


Fig. 6. Averaged dynamical model for the effect of control current on output voltage.

modelling the dynamics of the effect of control current on output voltage. In the averaged model, shown in Fig. 6, the bias winding of the saturable reactor, connected between the output choke and $C_1$, is replaced with a short, recognizing that only high-frequency AC voltage appears across this winding, as shown if Fig. 3. Also, the output of the rectifier is replaced with its average value, which is assumed to be determined by the ideal saturable reactor clamp current, $I_0 + I_{ctrl}$, multiplied by an scaling factor, $\eta$ $(0 < \eta < 1)$, which accounts for the non-ideal behavior discussed above.

## IV. Experimental Results

Two prototype circuits were constructed. The first was a low-frequency (25 kHz) converter used to verify the waveforms predicted above. The second was a 700 kHz circuit built with thick-film conductors on a ceramic substrate. Because some measurement points on the 700 kHz circuit, in particular currents and primary side transformer voltage, are difficult to access, it is useful to show some of the low-frequency prototype's waveforms.

### *A. Low Frequency Prototype*

The low frequency prototype was designed for a nominal input voltage of 40 volts, a nominal maximum output voltage of 5 volts, and maximum load current of 20 amps. The transformer turns ratio was 4:1:1. The turns ratio on each core of the nonlinear reactor was 4:1:1. (The primary side winding had four times the number of turns on the secondary winding, and four times the number of turns on the control winding.)

Fig. 7 shows the lower MOSFET drain-source voltage and the primary side reactor current of the 25KHz

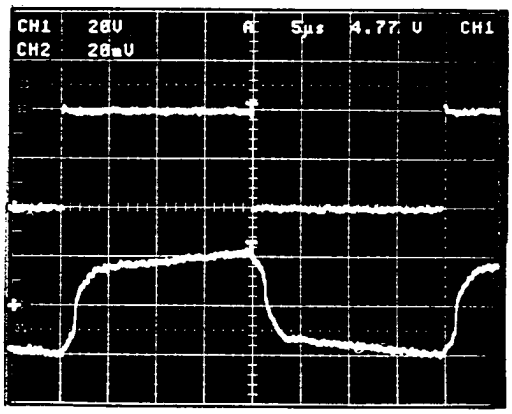


Fig. 7. 25 kHz prototype primary side waveforms. Top: $V_{DS2}$ (20V/div.); Bottom: $I_{primary}$ (1A/div.); 5 $\mu$sec/div.

circuit. As seen in this photograph, the current has a square characteristic and lags the switch voltage waveform. The reason for the non-zero slope of the top of the current waveform is the finite inductance of the output choke and finite magnetizing inductance of the saturable-reactor cores. The rounded corners of the current waveform are a result of the deviations from squareness of the $B - H$ characteristic of the saturating cores.

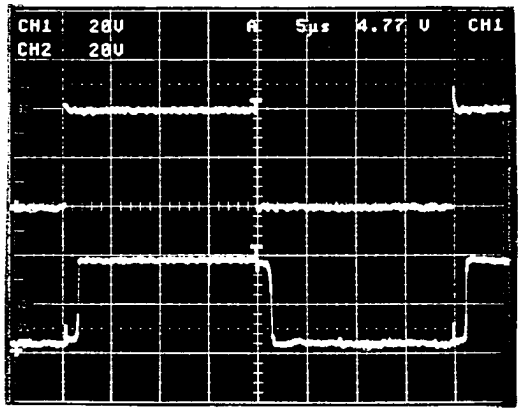


Fig. 8. 25 kHz prototype primary side waveforms. Top: $V_{DS2}$ (20V/div.); Bottom: $V_{xformer-pri}$ (20V/div.); 5 $\mu$sec/div.

Fig. 8 shows the lower MOSFET drain-source voltage and the primary side transformer voltage. Note that the transformer voltage is approximately in phase with the primary current of Fig. 7. The phase shift evident in Fig. 8 is the mechanism by which the converter voltage conversion ratio is adjusted. In particular, for maximum conversion ratio, the phase shift is minimum, and for zero conversion ratio, the phase shift is 90 degrees. The control of this phase shift is accomplished by adjusting the current $I_{ctrl}$ in the control winding of the saturable reactor, as discussed in Section II.

Fig. 9 shows the voltage applied to the final $L$-$C$ fil-

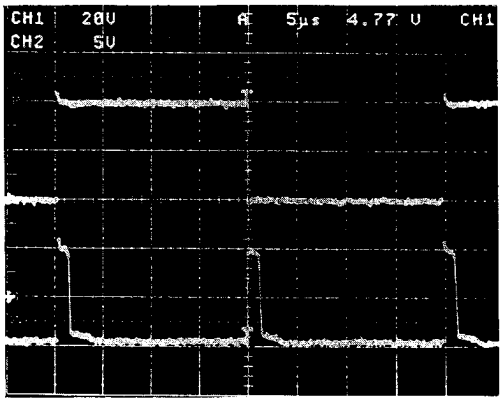


Fig. 9. 25 kHz prototype waveforms. Top: $V_{DS2}$ (20V/div.); Bottom: $V_{choke}$ (5V/div.) 5 $\mu$sec/div.

ter stage, after the bias winding on the saturable reactor. This voltage, $Vchoke$, is the sum of the approximately constant voltage on the rectifier load capacitor, $C_1$, and the secondary voltage on the saturable reactor. Note that the effective 'duty cycle' in this waveform is nearly unity since the circuit is being operated at nearly full output voltage.

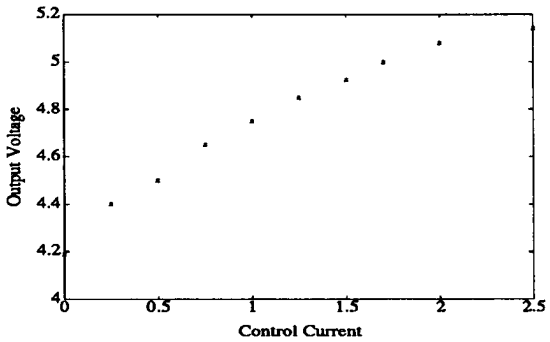


Fig. 10. Effect of control current on output voltage in 25 kHz prototype.

Fig. 10 shows the output voltage as a function of control current in the saturable reactor. The maximum operating range of the saturable reactor in this circuit was designed to allow only a limited range of control, and the offset from zero output at zero control current can be be attributed to saturation in the reactor.

Fig. 11 shows the output response to a step change in control current, from zero to one amp. Fig. 12 shows a simulation of the averaged circuit model of Fig. 6, which corresponds very closely to the experimental result. The value of $\eta$ for the simulation was determined from measurements of circuit operation to be approximately 0.64. Both the simulation and the experiment had a 8.9 $\mu H$ choke, 220 $\mu F$ capacitors for both $C_1$ and $C_2$, and a 0.52 $\Omega$ load resistor. The simulation differed from the model

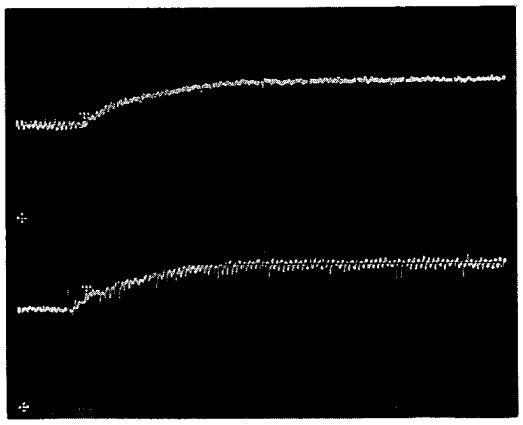

Fig. 11. 25 kHz prototype response to a step in control current. Top: $V_{out}$ (1V/div.); Bottom: $V_{C_1}$ (1V/div.); 0.2 msec/div.

of Fig. 6 by having a DC offset equal to the DC offset observed in the experimental circuit added to the current source.

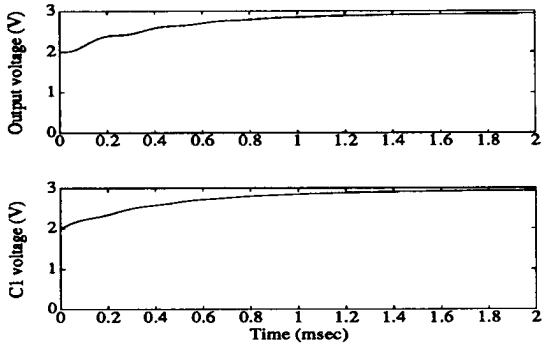


Fig. 12. Simulation of response to a step in control current, based on the averaged model in Fig. 6.

### *B. 700 kHz Prototype*

A 700 kHz prototype, shown in Fig. 13, was fabricated on a 0.025 in (0.64 mm) thick alumina substrate. Silver thick-film conductors were used with a palladium-silver top layer for solderability. Details on similar fabrications methods with thick-film copper are in [10]. Although a larger substrate was used for convenience, the active area used was approximately $3 \times 2$ in$^2$ ($8 \times 5$ cm$^2$). The board was designed to accommodate either packaged power semiconductors or bare dice. The test results reported here are with Schottky diode dice, and TO-220 packaged MOSFET active switches.

The transformer was constructed on a small ferrite "EI" core, 0.41 in (10.5 mm) high. The saturating reactors were built with a pair of amorphous metal alloy cores (Toshiba MB-8). The transformer and reactor were wound with

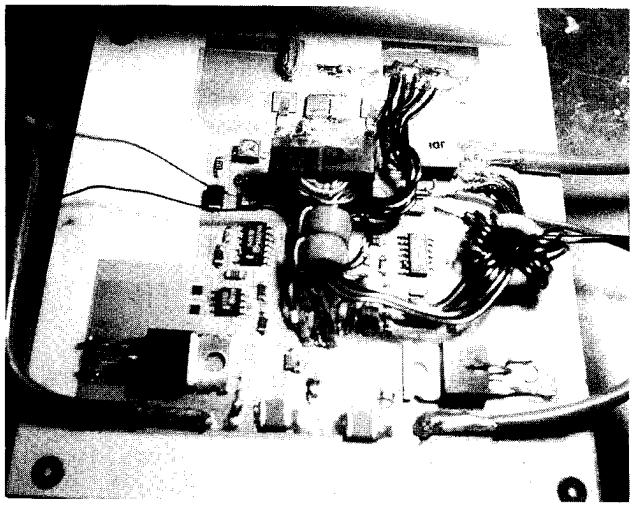

Fig. 13. 700 kHz prototype.

Litz wire, with multiple paralleled interleaved windings to reduce leakage inductance and proximity effect. Of particular importance was the leakage inductance between the two secondary windings of the transformer. This was kept under 10 nH by using four paralleled bifilar windings. Another leakage inductance that must be controlled is the inductance of the primary winding of the saturable reactor, when the core is saturated. This inductance, together with other leakage inductances, controls the switching time of the current, shown as instantaneous in Fig. 3. This leakage is controlled by making sure that the primary windings on the saturable reactor are tightly wrapped to the core so that they enclose a minimum area. The turns ratios were 2:1:1 on the transformer, and 2:1:5 on the saturable reactor. (The primary side winding had two turns, the secondary had one turn, and the control winding had five turns.)

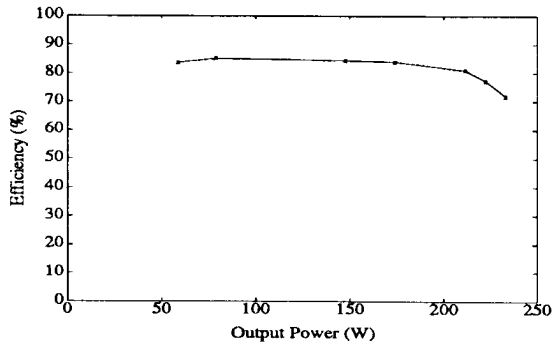


Fig. 14. Measured efficiency of the 700 kHz prototype.

The measured efficiency of the 700 kHz prototype with 40 V input and output near 6.5 V is shown in Fig. 14. The efficiency stays above 80% up to over 210W. Although our objective was not to maximize power density, we note that this corresponds to approximately 70 W/in$^3$(1100 W/cm$^3$), without the heat sink volume, or 45 W/in$^3$(740 W/cm$^3$) including the heat sink volume. We expect to achieve higher power and efficiency once several problems with the initial prototype are solved. First, the saturable reactor in the current prototype overheats, due to excessive losses and a poor thermal path. We suspect that some of the loss is due to eddy currents in the core when it is saturated. In this situation, the magnetic field is no longer parallel to the sheets of amorphous metal, and so is unfavorable for eddy currents. We are investigating improved methods of fabricating this component [11]. Our second major limitation preventing improved performance at high power is a higher-than expected resistivity of the silver conductor on the board. This was improved somewhat by soldering copper wire to the exposed conductors, some of the lower-layer conductors were not accessible, and their losses could not be reduced.

Despite these problems, the prototype did verify the viability of this topology for operation at high frequency. The waveforms shown in Fig. 15 show that zero voltage switching was achieved on the MOSFETs. Although there is ringing evident on the diode voltage, it is small, and represents only about 0.1 W of loss. Control by means of the saturable reactor functioned as expected, although overheating quickly lowered its flux capacity and decreased the control range. With the core around 40 degrees centigrade, and a 0.15 Ω load, the output voltage was 3.6 V with zero control current, and could be raised to 5.4 V with a control current of 2.5 A.

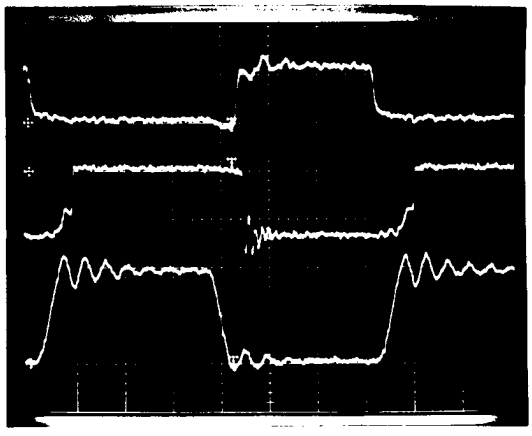

Fig. 15. Waveforms of 700 kHz prototype with 40 V input, 6.2V, 27 A output. Top: $V_{GS2}$ (10 V/div.); Middle: rectifier voltage, (10 V/div.); Bottom: $V_{DS2}$ (20 V/div.); 200 nsec/div.

## V. Variations and Extensions

The features of this circuit lend it to applications in many different configurations. For multi-output supplies, multiple power trains may be connected to the same half-bridge. Each output is then controlled by a separate control winding, but they share the same inverter bridge and gate-drive circuits. The windings of the saturating reactor may be reconfigured in such a way as to allow it to be connected on the secondary side of the transformer, allowing multiple outputs to share the same transformer. Placing the reactor on the secondary side also allows the use of a push-pull primary configuration. Multiple outputs can also be used to construct high power factor supply, using the approach of [12, 13], as shown in Fig. 16. In

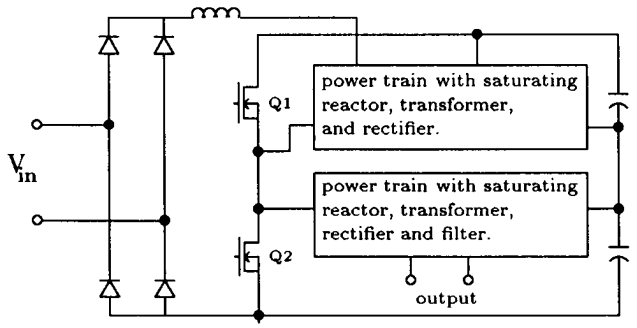


Fig. 16. High Power Factor Circuit

all of these circuits, the lack of a need for signals passing through isolation barriers is a salient advantage. The need for gate-drive signal isolation is avoided by the use of the local self-oscillating gate drive. The control winding is inherently isolated, and may be connected to a regulator circuit referenced to the isolated circuit it is controlling, or to the primary in the case of the high-power-factor circuit.

## VI. Conclusion

The DC-DC converter presented features constant-frequency operation, zero-voltage-switching, and square current and voltage waveforms. A saturable magnetic element produces the advantageous square waveforms, and provides isolated terminals from which the output voltage may be controlled. All of the semiconductor devices exhibit very low switching losses. The primary active switches exhibit zero-voltage switching. The output rectifier circuit has switching losses only due to the leakage inductance between the two secondary windings on the output transformer, which may be kept very small. The active switches (MOSFET's) are operated at a fixed frequency with 50% duty cycle, which allows the use of a simple self-oscillating gate drive. Experimental half-bridge implementations demonstrated operation as expected. A 700 kHz circuit achieved 200 Watt output at over 80% efficiency. The circuit is applicable to high-power factor converters and multi-output supplies, as well as DC-DC converters.

## Acknowledgment

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