Microfabrication Process for High-Frequency Power-Conversion Transformers

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Abstract– **A process for microfabrication of transformers for high-frequency power conversion applications is described. The process uses multilayer films of NiFe/SiO_2 magnetic material and copper coils deposited on a silicon substrate. Transformers less than 100 μm thick are designed to handle 1.7 W each in an area 1.5 by 5.4 mm. Coil measurements confirm predicted DC and AC resistance. Applications to a 10 W, 10 MHz DC-DC converter are discussed.**

I. Introduction

Magnetic components based on thin-film magnetic materials, constructed with microfabrication techniques, show great promise as components for compact and efficient high-frequency power conversion circuits. Experimental devices have demonstrated the principle [1, 2, 3, 4, 5, 6], and even demonstrated integration with semiconductor devices on the same substrate [7]. Calculations have indicated that transformers with a power density of 50 to 100 W/cm^2 and 90 to 95% efficiency should be possible [8].

This paper details the development of a fabrication process for such transformers, including sputtering of NiFe/SiO_2 multilayer magnetic material, electroplating of a copper coil, and the integration of these steps into a process for fabrication of a high-performance transformer. The approach used for the selection of the process is to give careful attention to those aspects that are important to achieving the high predicted performance, but also to keep the process as simple as possible, and to use as few different types of equipment as possible, in order to minimize the capital costs that would be required to establish a manufacturing facility capable of producing these devices.

Based on the features of the process developed, a design for a high-efficiency 10 MHz transformer is proposed. Converter designs using this transformer are also discussed, and preliminary test results on microfabricated transformer coils are reported.

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II. Transformer Geometry

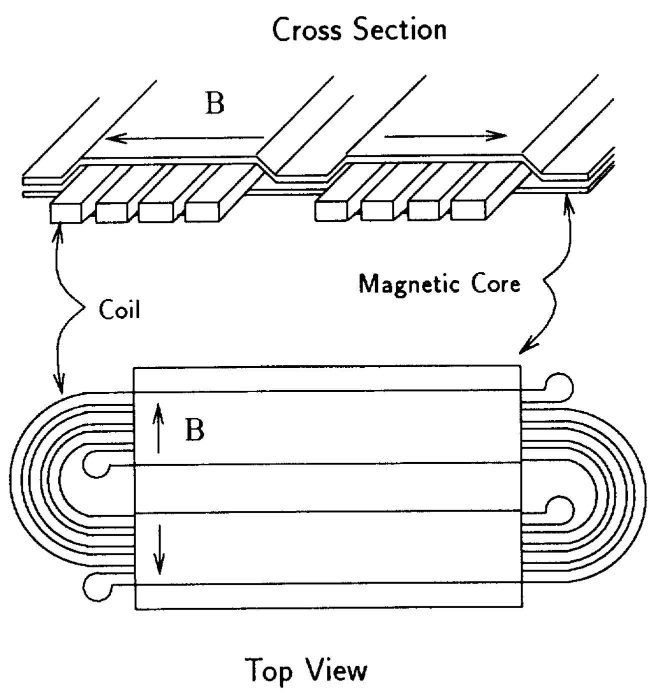

Fig. 1. "Pot-Core" Microfabricated Transformer Design

Figure 1 shows a general sketch of the "pot core" microfabricated transformer design that is used in this work. Magnetic material is deposited on a substrate. A set of interleaved primary and secondary coils is fabricated in a single layer on top of the magnetic material. Then additional magnetic material is deposited to close the magnetic path.

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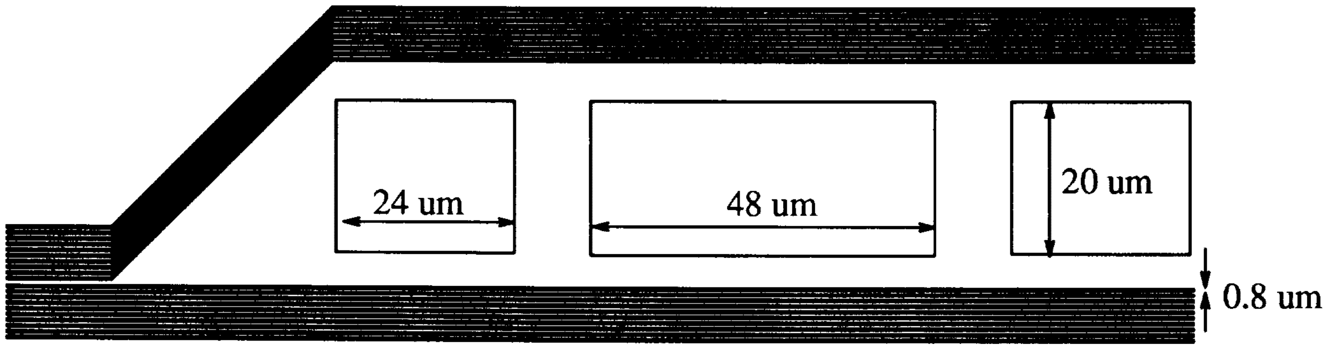

Fig. 2. Transformer design cross section

Compared to other possible designs, such as those using a single deposited layer of core material with conductors above and below it, this design has several important advantages. First, an anisotropic magnetic material can be used to full advantage, because the flux in the transformer is oriented in only one direction, as indicated. This results in very low hysteresis losses if a material with good anisotropic properties is used [8]. Secondly, there are no via connections between different layers of conductor. Multiple via connections forming a winding must have very clean, low-resistance contacts to insure that the overall resistance of the winding is not substantially affected. While this is possible to achieve [9], it is desirable to avoid this complication.

Based on the design method described in [8], a design for transformers for the 40 V to 10 V converter described in section IV has been developed. The converter is constructed with an array of six transformers connected in parallel, with each transformer designed to handle one sixth of the 1 amp output current, with 94.5% efficiency.

For a 2:1 transformer winding, we use two primary windings, connected in series after fabrication by using a bond wire. The primary windings are on either side of the secondary winding. The AC resistance of either winding may be calculated by multiplying the DC resistance by a factor F_r,

$$F_r = 1 + \frac{5p^2 - 1}{45}\psi^4, \qquad (1)$$

where p is the number of "layers," and ψ is the ratio of conductor thickness to skin depth [10, 11]. With primary windings on either side of each secondary winding, the value of p is one half for the secondary, and one for the primary. In [8], a single-variable optimization is used to find the optimal width for identical primary and secondary windings. For this "sandwiched" 2:1 transformer design, a similar multivariable optimization results in optimal widths of 24 μm for the primary and 48 μm for the secondary, assuming a 10 μm spacing between turns. AC winding loss has been confirmed by a finite element simulation, as detailed in Table II.

TABLE I
Parameters of Transformer Design

Symbol		Value
W_c	Width of conductor area	504 μm
W_{tp}	Width single primary turn	24 μm
W_{ts}	Width single secondary turn	48 μm
S_t	Spacing of turns	10 μm
W_s	Width of core	4.14 mm
h_c	Height of conductor	20 μm
h_s	Height of core	8.0 μm
h_s/N	Thickness of core layer	0.8 μm
h_d	Thickness of dielectric between conductor and core	5 μm
N	Number of layers of core	10
n_p	Number of turns in primary	8
n_s	Number of turns in secondary	4
	Outline of transformer	5.40 mm × 1.56 mm
A	Substate area	0.0841 cm^2
f	Operating frequency	10 MHz
B	Peak flux density	1.0 T
ρ_c	Conductor (Cu) resistivity	2.0 $\mu\Omega - cm$
ρ_s	Core (80% NiFe) resistivity	20 $\mu\Omega - cm$
μ	Core permeability	2000 μ_0

III. Transformer Fabrication Process

The transformer fabrication process described here follows thin film magnetic recording head fabrication processes [12, 13, 14, 15, 16, 17] very closely. Fig. 4 outlines the process. The first step is deposition of alternate layers of NiFe and SiO_2. The NiFe layers are on the order of 1 μm thick, and the SiO_2 on the order of 0.1 μm thick. Ten layers of each are deposited. Next, a 5 μm thick layer of photoresist is deposited. A thin ($\approx$ 1 μm or less) layer of

TABLE II
ELECTRICAL PERFORMANCE OF TRANSFORMER

Symbol		Calculated	Simulated	Measured
P	Power throughput	1.77 W		
P/A	Power density	21.0 W/cm^2		
P_{core}	Eddy current loss in core	27 mW		
R_p	DC resistance of primary (both windings in series)	3.62 Ω		4.09Ω
R_s	DC resistance of secondary	0.904 Ω		0.883 Ω
Fr_{sine}	AC resistance factor, 10 MHz sine wave	1.063	1.053	1.02 ± 0.06
Fr_{square}	AC resistance factor 10 MHz square wave	1.38		
P_{cond}	Total conductor losses	69 mW		
L_{ms}	Secondary Magnetizing Inductance	1.7 μH		
L_{as}	Secondary magnetizing inductance, air core			70 nH
v	Voltage on secondary	10.6 V		
P_{loss}	Total power loss	97 mW		
η	Efficiency	94.5%		

Fig. 3. Layout of photolithograhy masks for transformer, 25 times actual size. Overall dimensions are 5.4 mm by 1.56 mm.

metal, NiFe or Cu, is deposited on top of this to act as the seed layer for subsequent electroplating of the Cu coil. It is etched in a pattern similar to that of the coil. Next a 20 μm layer of photoresist is deposited, and patterned to form a mold into which the Cu coil is then electroplated. This results in a nearly-planar top surface if the electroplating rate is well-controlled to produce a thickness equal to that of the photoresist. Baking at 240° C results in the photoresist melting and flowing, to produce a sloped sidewall onto which subsequent NiFe and SiO_2 layers can be sputtered. Another 5 μm layer of photoresist is deposited, both to accomplish any addition planarization necessary for the top of the coils, and to act as an insulator. Finally, additional layers of NiFe and SiO_2 are deposited on top, to complete the magnetic path.

A. NiFe Deposition

If thin films of NiFe are deposited under the proper conditions, anisotropic properties allow for very low hysteresis loss [8]. The two most common deposition methods in the magnetic recording head industry are electroplating and sputtering. In order to control eddy current losses, we use multiple layers of thin NiFe film, separated by insulator [18, 19, 20]. Although the deposition itself proceeds much faster with electroplating than with sputtering, the over-

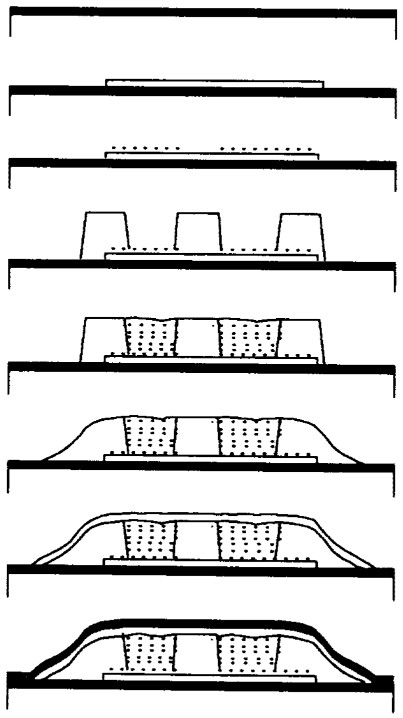

Fig. 4. Transformer Fabrication Process

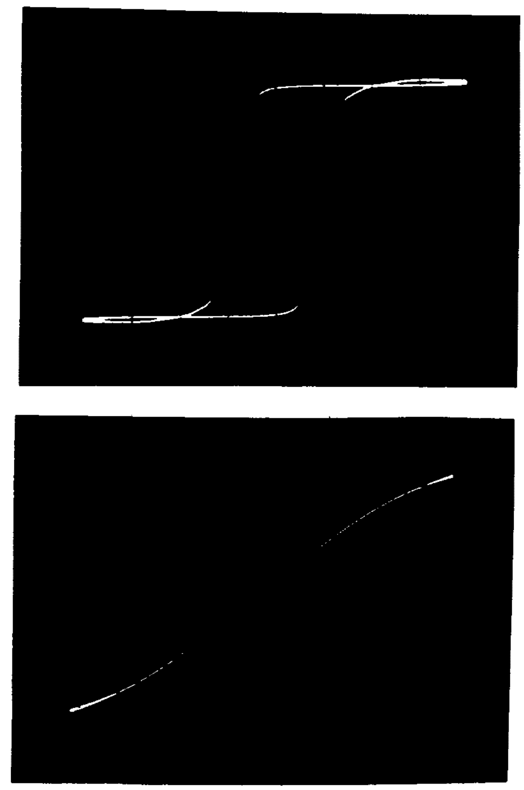

Fig. 5. (a) Easy-axis and (b) hard-axis hysteresis loops of a sputtered NiFe film.

all process for deposition of a multilayer film is faster and easier with sputtering. A sputtering machine outfitted with multiple targets can be used to alternately deposit the two materials without removing the substrate from the vacuum chamber, whereas a multilayer plating process would require not only a separate process to deposit the insulator, but also a new electroplating seed layer each time.

Figure 5 shows the hard axis and easy axis hysteresis loops of a sputtered film. In order to achieve this nearly-ideal behavior, it is important to pump down the sputtering chamber to a low base pressure, in order to remove any impurities such as water vapor, and prevent them from being incorporated in the film. A base pressure of 4×10^{-7} torr was found to give good results. The pumpdown to this point takes about eight hours using the cryogenic pump in our system.

The composition of the NiFe is also important. We started with an alloy target with a nominal composition of 80% Ni, 20% Fe by weight. The fraction of Ni was adjusted upwards by about 1% by attaching seven small squares of Ni to the surface of the target. Final tweaking of the process is then accomplished by varying the argon pressure used during deposition, in the range of 4 to 7 millitorr. The pressure affects both stress in the film and the exact composition, because Ni and Fe are scattered differently by the argon.

A permanent magnet is used to apply a small DC field of about 40 Oe during the deposition, to orient the magnetic anisotropy. A small field is sufficient, and a larger field can disturb the plasma and the sputtering process. The field must only be sufficient to overcome any stray fields in the area. The shape of the deposited structure also has an effect on the anisotropy, with a preferred easy axis in the long direction of a rectangular or elliptical outline of material. In the case that the shape anisotropy is opposite the desired easy axis direction, the applied field must also overcome this effect. However, our structures have the desired easy axis in the long direction.

Patterning a multilayer film presents some difficulty. One possible method is a wet etch, using a solution of ammonium persulfate and nitric acid to etch the NiFe, and hydrofluoric acid to etch the SiO_2. We have had difficulty with this method because the NiFe and SiO_2 layers tend to delaminate from each other during the etch. A solution to this problem may be to add a very thin ($\approx$ 10 nm) layer of a metal such as titanium, chromium, or aluminum between the SiO_2 and NiFe layers to enhance adhesion. In order to streamline this process, a single etch bath with solution of hydrofluoric and nitric acid can be used to etch through layers of NiFe, SiO_2, and Ti.

Fortunately, the patterning required for the magnetic layer need not be highly precise. Thus, it is should be possible to use a mechanical shadow mask during the multilayer $NiFe/SiO_2$ deposition. This is desirable, as it saves processing steps compared to the wet etch process. In our first attempt at this process, we used a 100 μm thick etched stainless steel mask. This intial mask did not work because of thermal expansion problems, and because it was difficult to get it to lie completely flat on the substrate. A silicon mask, currently being fabricated, will be superior in several respects. By using an anisotropic potassium hydroxide etch to pattern the silicon mask, it is possible to make a more precisely dimensioned mask, yet have it thick and stiff enough to remain flat against the substrate. In addition, silicon has much lower thermal expansion than stainless steel.

Ion milling could also be used to pattern the multilayer film. However, this will be slow, and thus expensive for thick films—on the order of 10 μm total thickness for the multilayer $NiFe/SiO_2$ in our devices. Care would need to be taken to avoid high temperatures and the resulting degradation of magnetic properties.

Shorts between NiFe layers at the edges could potentially provide an eddy current path and result in substantial losses. With the wet etch process, the relative etch rates may be adjusted such that the NiFe etches faster, insuring that the SiO_2 insulation extends beyond the edge of the NiFe and prevents any egde shorts. With a shadow mask during sputtering, it is possible to avoid edge shorts by sputtering the insulator with a higher argon pressure. Greater scattering results in the insulator extending further under the edges of the mask than the NiFe does.

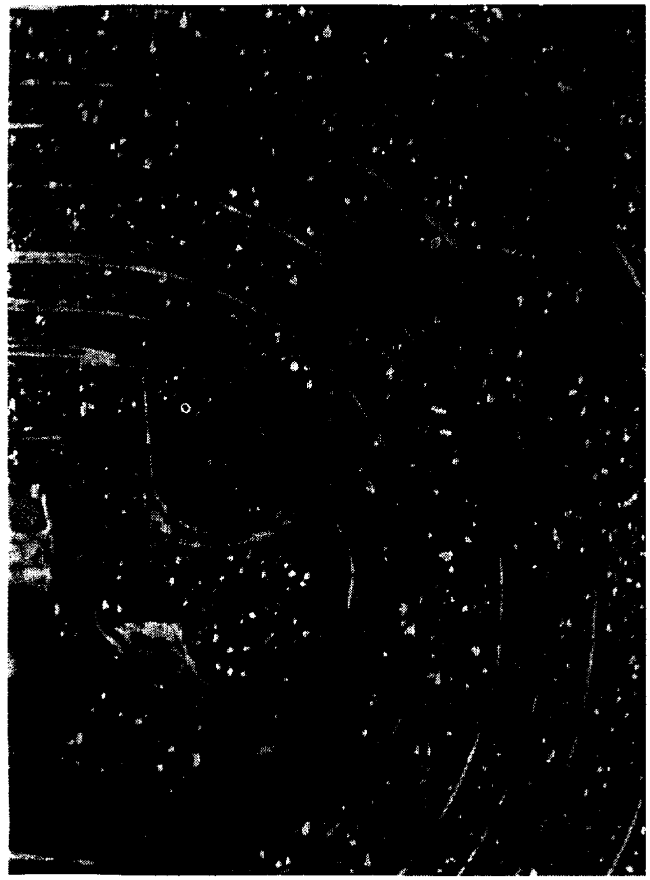

Fig. 6. Copper coil, showing bond pads at center. Width of the primary conductors is 24 μm, secondary 48 μm. All are 20 μm thick. Approximately 200 times actual size.

B. Coil Fabrication

In this process, photoresist is used not just as a temporary mask in fabrication, but as a part of the final structure, serving as an insulator around the conductors. This is rarely done in the IC industry, but is common in the magnetic recording head industry [16, 12, 21]. A 12 hour bake at 240°C in a vacuum or forming gas (10%H_2, 90%N_2) atmosphere is used to hard cure the photoresist. Although photoresist would present reliability concerns for semiconductor circuitry, the materials used in our device are all similar or identical to those used in magnetic recording heads, and thus we do not believe this will present a problem.

The coil fabrication starts with a 5 μm thick layer of photoresist for insulation between the core and coil. After this layer is hard baked, a thin ($\approx$ 1 μm) layer of NiFe is sputtered to serve as a seed layer for electroplating. The pattern of the seed layer is then defined by photoresist, and etched in a wet etch solution. The pattern is the same as that of the coil, with the exception of a temporary connection that comes out from each coil to join a bus that runs to the edge of the substrate for connection of wires for electroplating. The photoresist used to define the seed layer can be stripped with a solvent, leaving the hard-baked photoresist underneath unaffected. NiFe is used as the seed layer because it is already necessary to have deposition equipment and an etch bath for NiFe available for other parts of the process. Other metals could also be used for the seed layer.

After the photoresist used to define the seed layer is stripped, a 20 μm thick layer of photoresist is deposited. A commercially available photoresist (AZ P4620) is applied in two layers, each 10 μm thick. The substrate is soft baked (45 seconds on a 90° C hot plate bake) between photoresist applications. Following the second photoresist application, the photoresist is soft baked at a higher temperature (120° C, for 45 seconds), before it is exposed and developed. The mold for the coil consists of walls approximately 10 μm wide and 20 μm tall separating wider open areas. If the adhesion between the walls and the surface beneath them is not good, they tend to break off during or after developing, particularly where there are long, straight sections. Photoresist sticks well to hardbaked photoresist, and so this problem is avoided with the use of hardbaked photoresist as an insulator underneath the coils.

Contact exposure avoids the need for a projection system with a 20 μm depth of field. However, it is essential to get good contact between the mask and substrate in order to get precise patterning and near-vertical sidewalls. The process of spinning on the thick photoresist leaves an even thicker "edge bead" that stands the mask off from most of the substrate. Thus, it is necessary to wash off the edge bead prior to the exposure [22]. To allow this, the substrate is clamped between two metal plates, with an O-ring slightly smaller in diameter than the substrate between the substrate and the top plate. The edge bead can then be washed off cleanly.

Exposure and development of this thick resist results in a mold into which the copper coil can be electroplated. Figures 6 and 7 show a section of a coil following the electroplating step. After this, an additional 5 μm layer of photoresist is spun on the top to accomplish any additional planarization required, and to act as an insulator between core and coil. Baking then results in sloped sidewalls, necessary for the subsequent sputtering steps.

Measurements on completed coils (see Table II) show DC resistance within 15% of the expected value, indicating that the actual plated geometry is close to the design, and that the plated copper has good conductivity. Measurements of 10 MHz AC resistance were also performed, by shorting the secondary with a bond wire, and measuring impedance at the primary, with the two sections of the primary connected in series. At 10MHz a small uncertainty ($\approx$ 1 nsec) in the delay in the current measurement translates to a substantial uncertainty in the resistance measurement ($\approx$ 6%). Nonetheless, it was possible to confirm that the AC resistance was not excessive.

IV. Converter Design

As a first test bed for this circuit, a simple half-bridge forward converter (Fig. 8), has been designed. Zero voltage switching of the primary devices will be accomplished through the leakage inductance of the transformer. A limited range of voltage control can be achieved by varying the duty cycle between 50:50 and 70:30, resulting in a 20% line regulation range. A nominal 40V to 10V, 10W DC-DC converter will be constructed on the same silicon substrate as the transformers supporting it. Interconnections for the the circuit are fabricated in the same steps used to define the transformer coil. Since this gives only a single layer of conductor, a ground plane is used on the reverse side of the substrate to carry image currents and so reduce stray inductance of the interconnects (with a slight penalty in conduction losses). Small surface-mount-

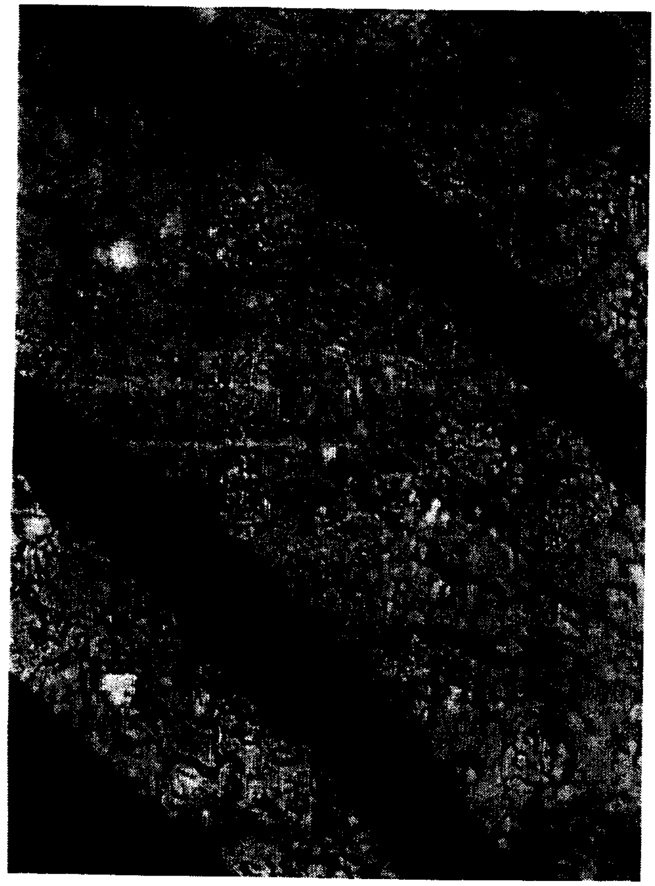

Fig. 7. Magnified view of conductors in electroplated coil. The grain structure of the copper formed by electroplating results in the rough surface on the top of the conductors. Approximately 1000 times actual size

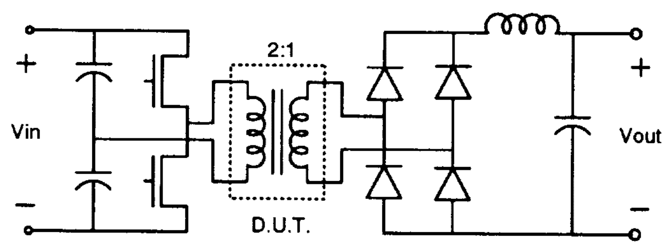

Fig. 8. DC-DC converter circuit.

package MOSFETs are used for the primary switches. Low-drop Schottky diodes for the full bridge rectifier are sized to minimize the combination of conduction loss and capacitive switching loss on the secondary.

V. Conclusion

A process for microfabricating a thin-film NiFe transformer for power conversion applications has been presented. The process uses multilayer films of NiFe/SiO_2 magnetic material and copper coils deposited on a sili-

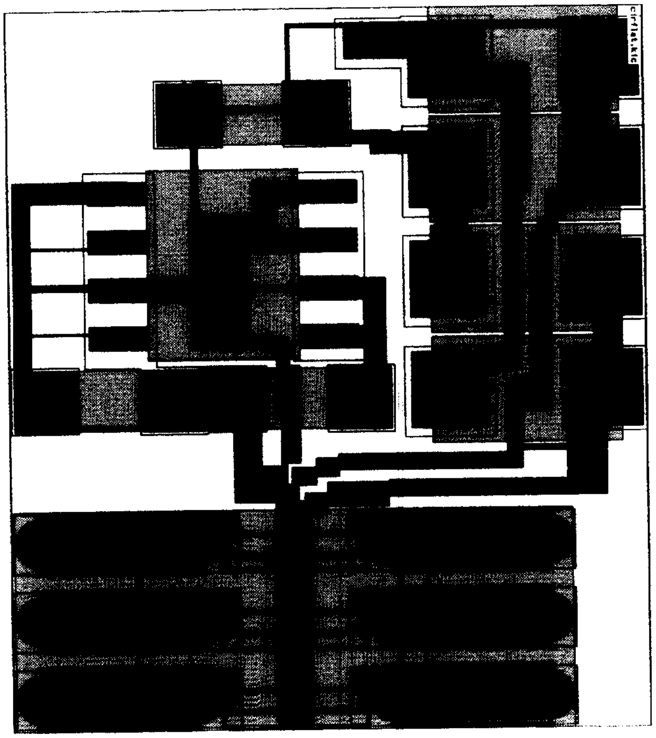

Fig. 9. Layout of circuit, including six parallel transformers, shown 5 times actual size. Solder pads for surface-mount components are outlined in grey. Connections in the electroplating seed layer that are subsequently cut are also shown in grey.

con substrate. Transformers less than 100 μm thick are designed to handle 1.7 W each in an area 1.5 by 5.4 mm. They will be applied to a 10W, 10MHz 40V to 10V DC-DC converter. Coil measurements have confirmed predicted DC and AC resistance.

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