Measured Performance of a High-Power-Density Microfabricated Transformer in a DC-DC Converter

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Abstract– **Experimental measurements are reported on microfabricated power conversion transformers. A device fabricated using a simplified 'sandwich' process confirms predicted performance in an 8 MHz DC-DC converter, where it achieves a power-handling density of 22.4 W/cm^2 at 61% efficiency. Preliminary test results are reported for transformers based on a closed-core design, which is expected to achieve higher efficiency.**

I. Introduction

Magnetic components based on thin-film magnetic materials, constructed with microfabrication techniques, show great promise as components for compact and efficient high-frequency power conversion circuits. Experimental devices have demonstrated the principle [1, 2, 3, 4, 5, 6, 7], including integration with semiconductor devices on the same substrate [8]. Calculations have indicated that transformers with a power density of 50 to 100 W/cm^2 and 90 to 95% efficiency should be possible [9].

This paper reports experimental performance measurements on transformers fabricated with a process similar to the process described in [10], including sputtered NiFe/SiO_2 multilayer magnetic material and an electroplated copper coil. One set of devices was fabricated using a simplified "sandwich" process. Test results on these sandwich transformers, including tests in an 8 MHz DC-DC converter application circuit, are reported. Subsequent fabrication work has been used to produce closed-core devices, which are expected to have higher efficiency. Initial tests on these devices are also reported.

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TABLE I
Transformer Design Parameters (All Designs)

Symbol		Value
W_{tp}	Width single primary turn	24 μm
W_{ts}	Width single secondary turn	48 μm
S_t	Spacing between turns	10 μm
h_c	Height of conductor	20 μm
h_s	Height of core	8.0 μm
h_s/N	Thickness of core layer	0.8 μm
h_d	Thickness of dielectric between conductor and core	5 μm
N	Number of layers of core	10
n_p	Number of turns in primary	8
n_s	Number of turns in secondary	4
	Outline of transformer	
	Original	5.40 mm × 1.56 mm
	Revised	5.46 mm × 2.17 mm
A	Substate area	
	Original	0.841 cm^2
	Revised	0.118 cm^2
f	Operating frequency	10 MHz
B	Peak flux density	1.0 T
ρ_c	Conductor (Cu) resistivity	2.0 $\mu\Omega - cm$
ρ_s	Core (80% NiFe) resistivity	20 $\mu\Omega - cm$
μ	Core permeability	2000 μ_0

II. Transformer Designs

The transformer designs used are based on the design techniques discussed in [9]. We report on two designs, summarized in Tables I, II, and IV. Both designs are variations of the designs reported in [10]. Fabrication of a "sandwich" test device, as shown in Fig. 3, was initially easier than the fabrication of the closed-core design, shown

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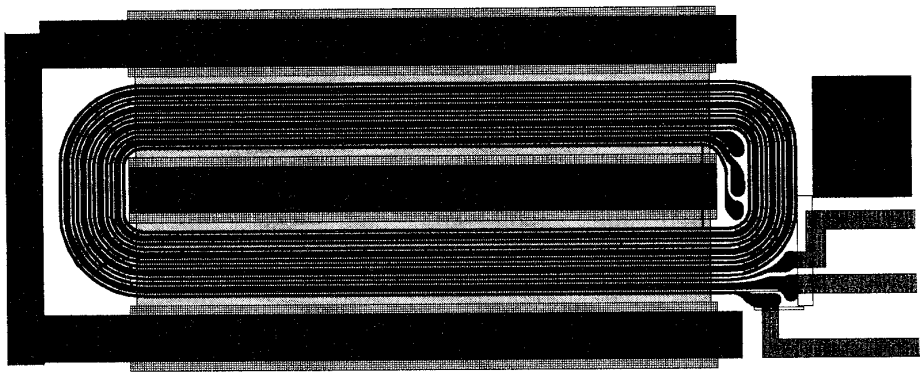

Fig. 1. Revised transformer layout, 20 times actual size.

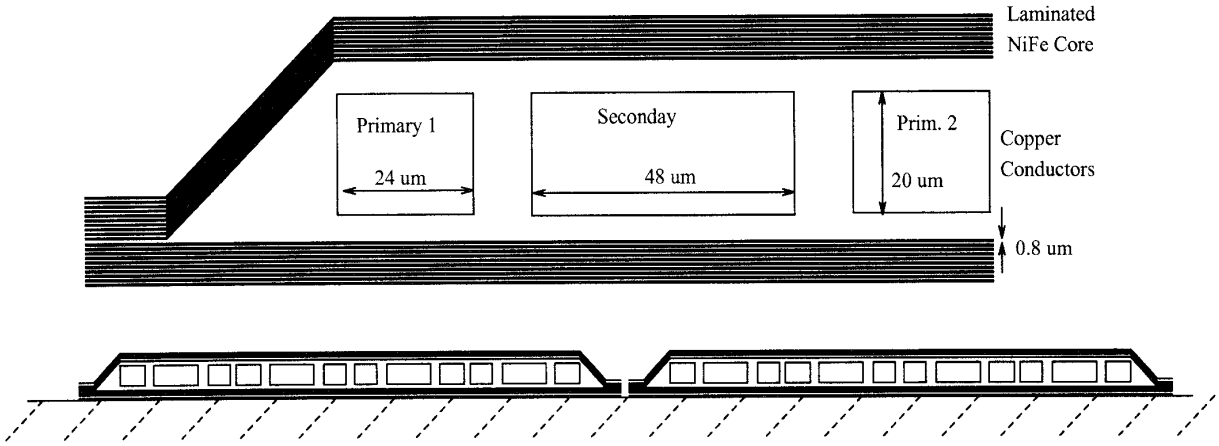

Fig. 2. Closed-core transformer design: detailed cross section and overall cross section.

in Fig. 2. Unfortunately, in the sandwich design, the gap in the magnetic path significantly degrades performance in several ways, but the device still performs better than previously-reported devices, and is useful to verify performance calculations. The reluctance introduced by the gap decreases the magnetizing inductance by about a factor of 5. The resulting increase in magnetizing current would increase the corresponding loss by a factor of 25, for the same primary resistance. However, the sandwich design produces an unfavorable field distribution [9], which results in a high AC resistance factor for the magnetizing current. A finite element simulation found this factor to be 3.84 for this design, when operating at 10 MHz. Thus, the overall conduction losses associated with the magnetizing current are about 90 times what they would be with a closed core. Although this severely limits the performance, the device is still useful for verifying proper operation. Conduction losses associated with the magnetizing current should be negligible in the closed-core design.

The second design was used to test closed-core devices. The mask layout was revised prior to fabricating these devices, in order to allow more room in the center of the windings for alternative methods of closing the core. Thus, the the area of the device is slightly larger (0.118 cm^2) and the calculated efficiency slightly lower (93.6%), than in the orginal design. Fig. 1 shows the revised mask layout.

III. Transformer Fabrication Process

The transformer fabrication process used is based on that described in [10]. However some aspects of the process have been improved, and will be described below, after the basic process is outlined. The first step is the deposition of alternate layers of NiFe and SiO_2. The NiFe layers are on the order of 1 μm thick, and the SiO_2 on the order of 0.1 μm thick. Ten layers of each are deposited. Next, a 5 μm thick layer of photoresist is deposited. A thin ($\approx$ 1 μm or less) layer of metal is deposited on top of this to act as the seed layer for subsequent electroplating of the Cu coil. It is etched in a pattern similar to that of the coil. Next a 20 μm layer of photoresist is de-

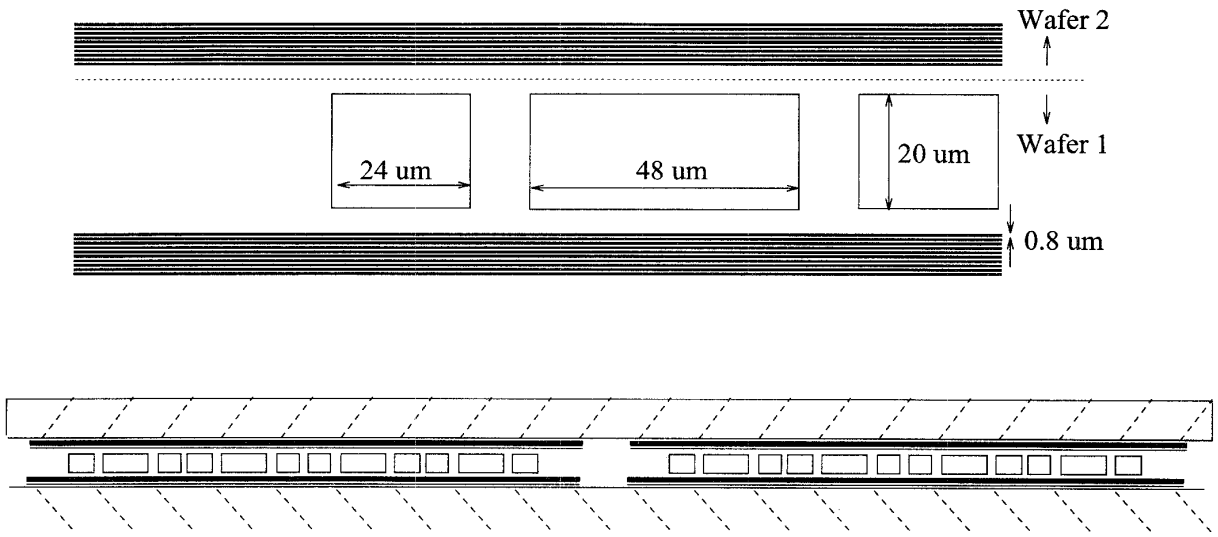

Fig. 3. Sandwich transformer design: detailed cross section, and overall cross section.

posited, and patterned to form a mold into which the Cu coil is then electroplated. This results in a nearly-planar top surface if the electroplating rate is well-controlled to produce a thickness equal to that of the photoresist. A device at this stage is shown in Fig. 4. Baking at 240° C

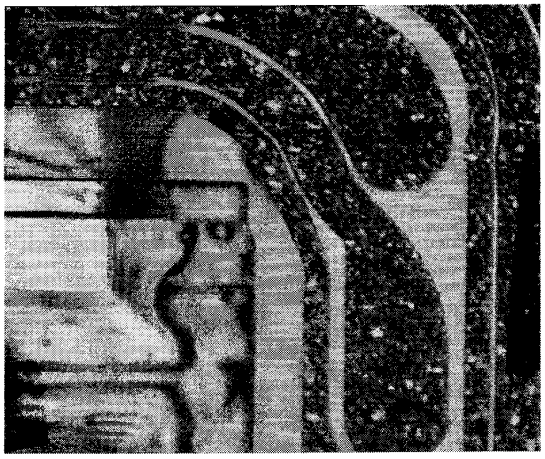

Fig. 4. Lower core and coil of transformer.

results in the photoresist melting and flowing, to produce a sloped sidewall onto which subsequent NiFe and SiO_2 layers can be sputtered. Another 5 μm layer of photoresist is deposited, both to accomplish any addition planarization necessary for the top of the coils, and to act as an insulator. Finally, additional layers of NiFe and SiO_2 are deposited on top, to complete the magnetic path.

A. Patterning the Magnetic Multilayer Film

The patterning of the multilayer film is accomplished with a wet-etch. Difficulties faced included finding a single etch solution to etch both NiFe and SiO_2, and the tendency for the layers to delaminate during the etch, due to stress in the NiFe. The latter problem was solved by the use of a very thin ($\approx$ 10 nm) layer of titanium between each layer of NiFe and SiO_2 to enhance adhesion.

A solution of nitric acid and hydrofluoric acid was found to etch all three materials, allowing a single etch bath to be used for the entire multilayer etch. Immersion in hydrofluoric acid delaminates photoresist from many surfaces, including SiO_2 and NiFe. For this reason, a thin layer of chrome was used as a mask for this step. The exact composition of the bath can be adjusted to vary the relative etch rates of the magnetic and insulating materials. This is useful because a slower etch rate for the insulator helps guarantee that the NiFe layers will not short at the edges (Fig. 5). Shorts at some edges would introduce detrimental eddy current paths. An alternative is to use a bath with similar etch rates for the two materials, but subsequently cut back the NiFe in a bath that etches only NiFe and not SiO_2. The results of these two strategies are shown in Figs. 6 and 7.

B. Completing the Magnetic Path

Difficulties with adhesion were initially encountered when completing the magnetic path by depositing further magnetic material on top of the hardbaked photoresist. Although these problems have largely been solved, several other means of completing the magnetic path were used to

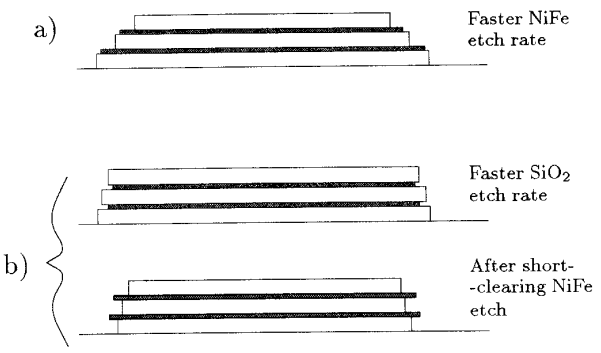

Fig. 5. Effect of multilayer etch bath composition on potential for edge shorts. a) Faster etch rate of NiFe prevents shorts. b) An etch in a bath that might leave shorts between layers, due to similar etch rates or a faster etch rate of SiO_2, can be followed by an etch that removes only NiFe to clear any shorts between layers.

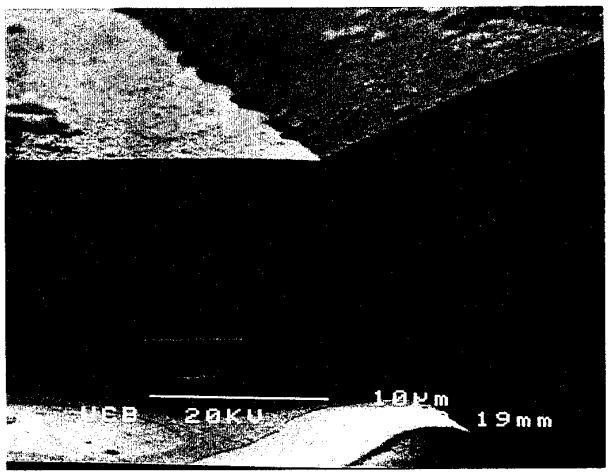

Fig. 7. Laminations of NiFe/SiO_2, patterned by first etching in a solution that attacks both materials at a similar rate, and then etching in a solution that only attacks NiFe. The protruding layers are the SiO_2 left behind by the second etch.

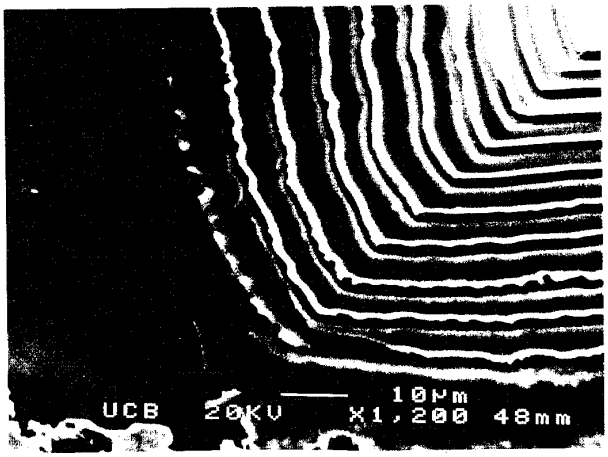

Fig. 6. Laminations of NiFe/SiO_2, patterned by etching in a solution that attacks NiFe faster.

fabricate complete devices while problems with the original process were being solved. One of these methods is the sandwich construction, as described above. A coil is fabricated on top of patterned magnetic material, as described above, but then the magnetic path is completed with a patterned magnetic multilayer deposited on a different substrate, diced into individual "lids" that are then inverted on top of the coil (Fig. 3).

To avoid the degradation in performance that results from the gaps in the magnetic path in the sandwich device, an improved "lid" process was developed to produce devices with a closed magnetic path. Prior to deposition of the magnetic multilayer, the substrate used for the lid has "bumps" added to close the core, as shown in Fig. 8.

The fabrication of the lid proceeds as follows. A thin adhesion layer of Ti, followed by 0.2 um of NiFe, is sputter deposited on a silicon wafer. This initial layer of NiFe serves to enhance adhesion of subsequently deposited photoresist and NiFe. Next, thick photoresist (35 um) is spun on in three layers, and then exposed and developed in the pattern of the desired bumps. It is baked in forming gas (10% H_2, 90% N_2) at 240° C at atmospheric pressure, and then in a vacuum to remove any residual nitrogen or water vapor. A brief sputter etch removes any surface contamination or oxide, to insure that the following layer of sputter deposited NiFe adheres well. Alternate layers of NiFe and SiO_2 are deposited, with a thin adhesion layer of Ti between each. A 30 nm thick layer of Cr is evaporated on top of the multilayer. The chrome is patterned with a wet etch, and then serves as a mask for the etch of the magnetic multilayer. A complete lid is shown in Fig. 9. Fig. 7 is a close-up of the edge of one of the "bumps" on the same lid.

The initial adhesion problems with direct deposition of the top layers of magnetic material over the coil were partly due to an attempt to improve adhesion on top of the photoresist by using a thin layer of Ti. Although Ti improves adhesion for many materials, subsequent tests demonstrate that it actually is detrimental to adhesion on hardbaked photoresist. Directly deposited NiFe adheres much better. In addition, there were problems with wa-

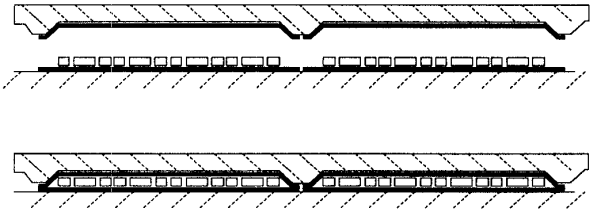

Fig. 8. Closed-core device assembled from coil and core on lower substrate and core on upper grooved substrate.

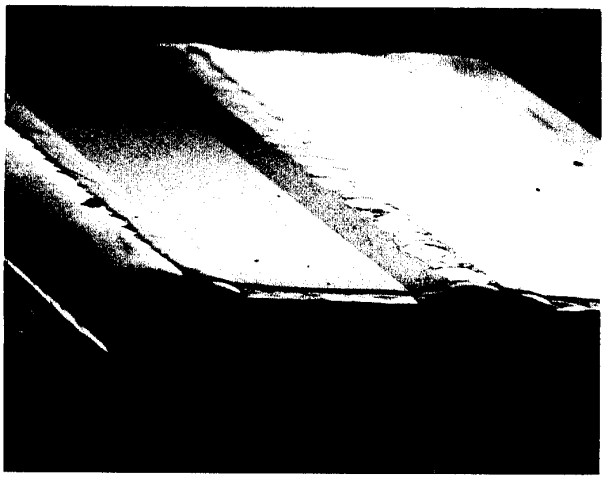

Fig. 9. Lid for assembled closed-core transformer.

ter vapor or other gas bubbling out of the photoresist and getting trapped beneath the deposited film. The gas was forced out of the photoresist by the combination of heat and vacuum encountered during sputtering. To remove the gas ahead of time, a vacuum bake process was developed. A short sputter etch prior to deposition is also used to clean and prepare the surface. Although the process has not been tested with a complete device, the same process was used to prepare the photoresist bumps used in the closed-core lid process described above, and we have encountered no problems with adhesion on the bumps.

IV. Experimental Results

A. Sandwich Device

The sandwich transformer was initially tested on a probe station with a network analyzer calibrated for impedance measurements with the voltage and current probes in the same position as used for the actual measurement. The measured secondary inductance at 10 MHz was 345 nH, with an ESR of 3.6 ohms, both similar to predictions from finite element analysis (see Table II), confirming small-signal performance as expected.

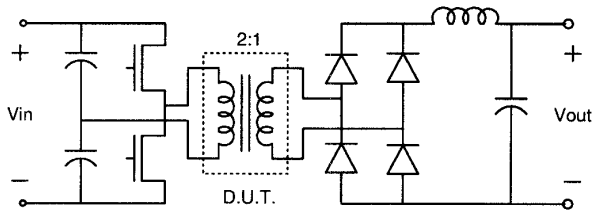

Fig. 10. DC-DC converter circuit.

As a first test bed for the transformers, a simple half-bridge forward converter (Fig. 10), is used. A similar circuit is discussed in detail in [11, 12]. Zero voltage switching of the primary devices may be accomplished through the leakage inductance of the transformer. A limited range of voltage control can be achieved by varying the duty cycle between 50:50 and 70:30, resulting in a 20% line regulation range.

Large signal performance of the sandwich transformer was tested using this circuit. First the no-load magnetizing losses were measured with the secondary open-circuited. The DC input power to the circuit was measured, and compared with the DC input power with the transformer primary replaced by a "dummy" air-core litz-wire inductor having the same inductance, but assumed to have negligible losses. The difference in loss was attributed to core loss and conduction loss in the transformer primary. An additional inductor connected in parallel with the transformer primary or dummy inductor was used to provide sufficient current to commutate the inverter node capacitance with low loss.

Fig. 12 compares the measured loss to the I^2R loss predicted from the AC resistance factor obtained from simulations and the current calculated assuming ideal waveforms. The independent variable is the DC bus voltage. The predicted and measured loss agree well, except at high voltages where the measured loss is significantly higher, indicating the onset of magnetic saturation or hysteresis loss in the core. Further work is needed to determine what caused this deviation. However, the device shows nearly ideal operation at up to 75% of the design voltage of 40V.

The results of efficiency measurements for operation in an 8 MHz DC-DC converter, including a breakdown of estimated losses in different portions of the circuit, are

TABLE II

SANDWICH TRANSFORMER PARAMETERS

Symbol		Calculated	Simulated	Measured
R_p	DC resistance of primary (both windings in series)	3.62 Ω		4.84Ω
R_s	DC resistance of secondary	0.904 Ω		1.09 Ω
R_{bp}	Resistance of primary bond wires	0.13 Ω		
R_{bs}	Resistance of secondary bond wires	0.12 Ω		
$F_{r\,sine}$	AC resistance factor, load current, 10 MHz sine wave	1.063	1.053	1.02 ± 0.06*
R_{tl}	Total load-current resistance, reflected to primary	10.3Ω**		
$F_{r\,mag}$	AC resistance factor, magnetizing current, 10 MHz sine wave		3.84	3.3
L_{ms}	Secondary magnetizing inductance at 10 MHz		360 nH	345 nH
L_{as}	Secondary magnetizing inductance, air core			70 nH
EPR	Parallel loss resistance (an alternative model for the loss modeled by R_s and $F_{r\,mag}$		134Ω 134Ω	

*Measured with no core.

**Based on measured DC resistance and F_r from simulation, with calculated bond-wire resistance added.

TABLE III

PERFORMANCE OF SANDWICH TRANSFORMER IN 8 MHz CONVERTER

Symbol		Calculated	Measured
P_{in}	Converter power input		3.74 W
V_{in}	Converter input voltage		30 V
P_{out}	Converter power output		1.625 W
V_{out}	Converter output voltage		4.21 V
P_d	Rectifier loss	.263 W	
P_{to}	Transformer output power	1.89 W	
$P_{ckt-ref}$	Reference half-bridge circuit power loss, with 0.6 A rms triangular current waveform.		.585 W
P_{ckt}	Half-bridge circuit power loss, calculated by scaling $P_{ckt-ref}$ to account for increased primary current.	.644 W	
P_{tm}	Transformer magnetizing loss	.535 W*	.723 W
P_{tw}	Winding loss due to load current	.383 W	
P_t	Total transformer power loss. Measured result is based on assuming that all converter losses that are not otherwise accounted for occur in the transformer.	.919 W	1.206 W
η_t	Transformer Efficiency		61%
P/A	Transformer power density		22.4 W/cm^2
η_c	Circuit Efficiency		43.4%

*Based on measured resistance and inductance from Table II and an 8 MHz simulated F_r for magnetizing current of 2.93. Core loss is neglected.

detailed in Table III and Fig. 11. Assuming that all unaccounted-for losses are in the transformer, the device achieves an efficiency of 61% in-circuit, with a transformer output power of 1.89 W. This corresponds to a power density of 22.4 W/cm^2, an order of magnitude higher than the highest previously-reported power densities for a thin-film transformer.

Overall circuit performance was hindered by higher-than-expected losses in the half-bridge switches. The small commercial SO-8 package MOSFETs used were found to have substantial parasitic distributed gate resistance, limiting switching speed. Designing the a MOSFET layout to minimize gate resistance would facilitate high efficiency in the half-bridge circuit.

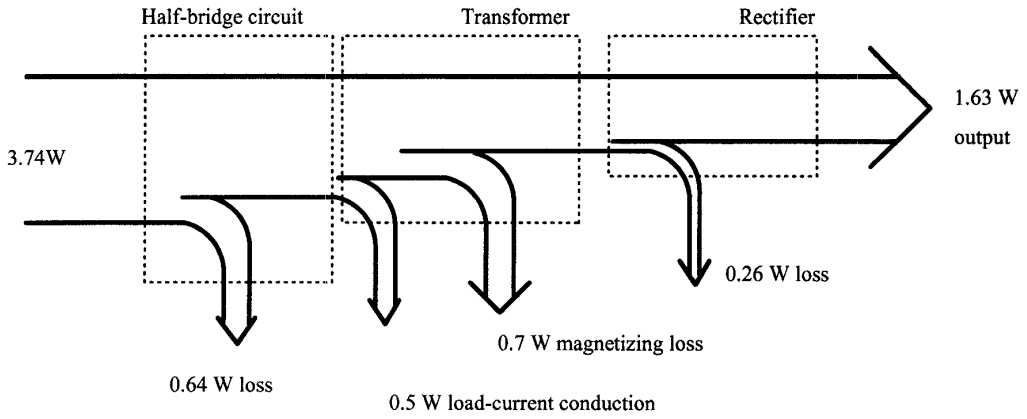

Fig. 11. Loss breakdown for 8 MHz DC-DC converter with sandwich transformer.

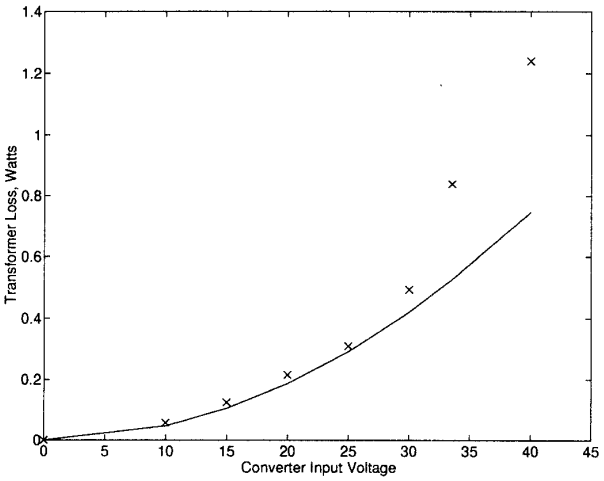

Fig. 12. No-load loss, sandwich transformer. Predicted (solid line) and measured ('x') as a function of input voltage.

B. Closed-Core Assembled Devices

Devices with a closed-core lid, as shown in Fig. 8, have been tested with a network analyzer, but have not yet been tested in the circuit application. Initial test results are summarized in Table IV. Secondary inductance at 10 MHz was 794 nH, with an equivalent parallel loss resistance of 160 ohms. The inductance is slightly more than one half of the expected 1.44 μH, but this can be explained by lower than expected permeability of the magnetic material in the lid deposition, of approximately 1000, and by imperfect mating of the lid and base. The loss, however, is significantly higher than expected. Network analyzer tests showed that the loss scales with the square of the voltage, at least over the tested voltage range, up to 1.4 V rms on the secondary. If this scaling holds up to the 10.6 V rated secondary voltage, the loss at 10 V would be 700 mW, or almost 20 times the expected 38 mW of core loss. The efficiency of the transformer, assuming operation as rated otherwise, would be 70%—better than the sandwich design, but still substantially lower than ideal.

Possible sources of the excess loss include hysteresis in the NiFe and eddy current resulting from shorts between layers of NiFe. Some defects were observed in the multilayer films of the lids, possibly resulting from particle contamination of the wafer prior to the multilayer sputter deposition. This could have produced shorts between layers. Eddy current losses in the NiFe films near the magnetic gap between upper and lower core halves could also contribute to the loss. The sputter deposition on the sloped sidewalls of the lid can be expected to affect the magnetic properities of the film. Additional anisotropy can be expected in the direction of the length of the bumps, resulting in lowered permeability [13]. Lower permeability in this region would be acceptable and would only slightly decrease magnetizing inductance. However, deposition on sloped surfaces has also been reported to result in increased hard-axis coercivity, and thus significant hysteresis losses [14]. The increased coercivity found in [14] was for a 60° slope, much greater than the 30° slope in our devices. However, this does not rule out hysteresis losses in the sloping portions of the lid NiFe as the source of excess loss.

V. Conclusion

Microfabricated transformers show great promise for high-frequency power conversion applications. A fabrication process using multilayer films of NiFe/SiO_2 mag-

TABLE IV
ELECTRICAL PERFORMANCE OF CLOSED-CORE TRANSFORMER (REVISED DESIGN)

Symbol		Calculated	Measured
P	Power throughput	1.77 W	
P/A	Power density	14.9 W/cm^2	
EPR	Core loss resistance referred to secondary	2.95 kΩ	160Ω
P_{core}	Core Loss	38 mW	0.70 W*
R_p	DC resistance of primary (both windings in series)	5.39 Ω	
R_s	DC resistance of secondary	1.35 Ω	
$F_{r\,sine}$	AC resistance factor, 10 MHz sine wave	1.063	
$F_{r\,square}$	AC resistance factor 10 MHz square wave	1.38	
P_{cond}	Total conductor losses	75 mW	
L_{ms}	Secondary Magnetizing Inductance at 10MHz	1.44 μH	794 nH
v	Voltage on secondary	10.6 V	
P_{loss}	Total power loss	113 mW	775 mW*
η	Efficiency	93.6%	69.5%*

* Projected from measured small-signal core loss measurement, assuming excess loss is eddy current loss.

netic material and copper coils deposited on a silicon substrate has been developed. Devices fabricated using a simplified 'sandwich' process confirm predicted performance, and operation has been further verified in an 8 MHz DC-DC converter application, where the transformer achieves a power-handling density of 22.4 W/cm^2 at 61% efficiency. Initial tests on transformers based on a closed-core design show the expected increase in magnetizing inductance, but show significant unexpected core losses. Further work is needed to identify the source of this problem, and achieve the predicted efficiency in excess of 90% at a similar power-handling density.

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