A Low-Voltage CMOS DC-DC Converter for a Portable Battery-Operated System

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Abstract— **Motivated by emerging battery-operated applications that demand compact, light-weight, and highly efficient DC-DC converters, a buck circuit is presented in which all active devices are integrated on a single chip using a standard 1.2μ CMOS process. The circuit delivers 750mW at 1.5V from a 6V battery. To effectively eliminate switching loss at high operating frequencies, the power transistors achieve nearly ideal zero-voltage switching (ZVS) through an adjustable dead-time control scheme. The silicon area and power consumption of the gate-drive buffers are reduced with a tapering factor that minimizes short-circuit current and dynamic dissipation for a given technology and application. Measured results on a prototype IC indicate that on-chip losses at full load can be kept below 8% at 1MHz.**

I. Introduction

Current trends in consumer electronics demand progressively lower-voltage supplies [1]. Portable electronic devices, such as laptop computers and personal communicators, require ultra low-power circuitry for battery operation. The key to reducing power consumption while maintaining computational throughput in such systems is to use the lowest possible supply voltage and compensate for the resulting decrease in speed with architectural, logic-style, circuit, and other technological optimizations [2].

The multimedia InfoPad terminal is one example of a portable, battery-operated, high-speed personal communication system [3, 4, 5]. The baseband circuitry in the current InfoPad terminal, including the encoder and decoder for data compression, A/D and D/A converters, and spreader and despreader for spread spectrum RF communication, are being designed to operate at 1.5V to minimize power consumption. However, because the system also requires supplies of $\pm$5V to power the RF transceiver circuitry and -17V, and $+12$V for the flat panel display, a number of DC-DC converter outputs are needed to generate these voltages from a single 6V battery. In order to facilitate portability and conserve battery life in InfoPad, power conversion must be done in minimal space and mass, implying high operating frequencies, while retaining the high efficiency more typical of lower frequency converters.

A completely monolithic supply (active and passive elements) would meet the severe size and weight restrictions of a hand-held device. Because such applications call for low-voltage power transistors, their integration in a standard logic process is tractable. However, existing monolithic magnetics technology cannot provide inductors of suitable size [6]. Fortunately, transformers and inductors fabricated with micron-scale magnetic-alloy and copper thin films are currently being developed [7], indicating that low voltage supplies able to efficiently deliver several watts of power will be realized in a single multi-chip module (MCM) within the next several years.

Motivated by the rigorous requirements of the InfoPad terminal, a 6V to 1.5V, 750mW buck converter has been designed and is presented in this paper. Due to the low voltage and current levels, all of the active devices are integrated on a single chip and fabricated in a standard 1.2μ process through MOSIS[1]. The circuit exhibits nearly ideal zero-voltage switching (ZVS) of the power transistors over a wide range of operating conditions using an adaptive dead-time control scheme, substantially reducing switching losses associated with high-frequency operation. The CMOS gate-drive buffers are designed with a process and application dependent tapering factor which minimizes both their dynamic and short-circuit current losses. The design is scalable, and all of the techniques presented here can be used to improve the efficiency of boost or buck-boost type converters, each of which is typically required in the power distribution scheme of a battery-operated system.

The paper is organized as follows. First, in section II, a brief circuit description is given, including a discussion

[1]MOS Implementation System: users submit VLSI designs expressed in digital form, and receive packaged parts in 8 to 10 weeks. MOSIS is under sponsorship of ARPA, and operated by the Information Sciences Institute of USC.

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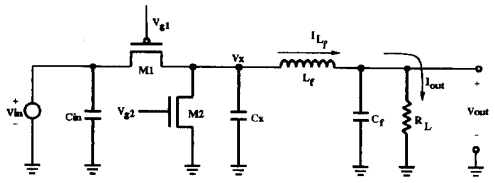

Fig. 1. Low-output-voltage buck circuit.

of relevant timing issues. Section III outlines an adaptive dead-time control scheme. Then, section IV describes the design of the power transistors. An overview of the low-power CMOS gate-drive is presented in section V, including a qualitative loss analysis. In section VI, the key layout and packaging issues are considered. Finally, section VII reports on results measured on a prototype IC.

II. Circuit Description

The power train of the low-voltage buck circuit is shown in Figure 1. All active devices, including the power transistors ($M1$ and $M2$) with their gate-drive, and all regulation and control circuitry, are integrated on a single 4.2mm × 4.2mm die in a 1.2μ CMOS process, and housed in a 64-pin PGA package. Currently, the design requires four passive components at the board level: a decoupling input capacitor (C_{in}), a snubber capacitor (C_x), and an output filter inductor and capacitor (L_f and C_f).

The operation of the circuit is described with reference to the waveforms of Figure 2, which represent the steady-state behavior of an ideal circuit with lossless filter components. The inverter node voltage, V_x, is quasi-square with an operating frequency of f_s =1 MHz, and a nominal duty cycle, D, of 25%. The soft-switching behavior is similar to that described by [8] and other authors. The converter delivers 500mA at 1.5V from a 6V battery.

Assume that at a given time (the origin in Figure 2), the rectifier ($M2$) is on, shorting the inverter node to ground. Since by design, the output is assumed DC and greater than zero, a constant negative potential is applied across L_f, and I_{L_f} is linearly decreasing. By choosing the filter inductor small enough such that the current ripple exceeds the average load current, I_{L_f} ripples below zero.

If the rectifier is turned off after the current reverses (and the pass device, $M1$, remains off), L_f acts as a current source, charging the inverter node. To achieve a lossless low to high transition at the inverter node, the pass transistor is turned on when $V_x = V_{in}$. In this scheme, a pass device gate transition occurs exactly when $V_{ds_1} = 0$.

With the pass device on, the inverter node is shorted to V_{in}. Thus, a constant positive voltage is applied across L_f, and I_{L_f} linearly increases. The high to low transition at V_x is initiated by turning $M1$ off. As indicated by Figure 2, at this time, the sign of current I_{L_f} is positive.

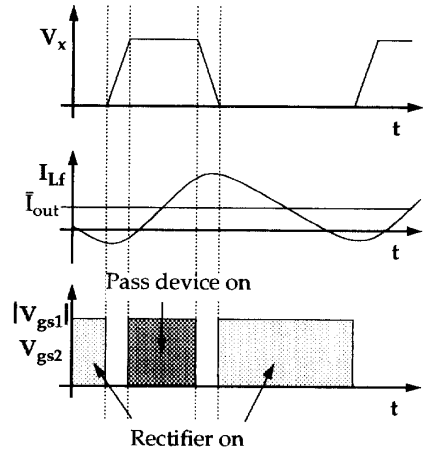

Fig. 2. Nominal waveforms of the buck circuit in Figure 1.

Again, L_f acts as a current source, discharging C_x. If the rectifier is turned on with $V_x = 0$, a lossless high to low transition of the inverter node is achieved, and the rectifier is switched at $V_{ds_2} = 0$.

In this scheme, the filter inductor is used to charge and discharge the parasitic and snubber capacitance at the inverter node in a lossless manner, allowing the power transistors to be switched at zero drain-source potential (ZVS). This essentially eliminates switching loss, a factor which may otherwise preclude the use of high-frequency converters in low-power systems.

A. Timing Issues

Because the inverter node transition intervals are designed to be small compared to the switching period, I_{L_f} is assumed triangular with peak values $\bar{I}_{out} - \frac{\Delta I_{L_f}}{2}$ and $\bar{I}_{out} + \frac{\Delta I_{L_f}}{2}$ which are constant over the entire dead-time. The ratio of inverter node transition times is given by the ratio of currents available for each commutation:

$$\frac{\tau_{x_{LH}}}{\tau_{x_{HL}}} = \frac{\frac{\Delta I_{L_f}}{2} + \bar{I}_{out}}{\frac{\Delta I_{L_f}}{2} - \bar{I}_{out}}, \quad (1)$$

and approaches unity for large inductor current ripple. Here, τ_x indicates an inverter node transition time, with subscripts LH and HL denoting low to high and high to low transitions respectively, $\bar{I}_{out}$ is the average load current, and $\frac{\Delta I_{L_f}}{2}$ is the zero-to-peak inductor current ripple. Choosing a maximum asymmetry in the transition intervals of $\frac{\tau_{x_{LH}}}{\tau_{x_{HL}}} = 4$ at full load results in a minimum zero-to-peak ripple of

$$\frac{\Delta I_{L_f}}{2} = \frac{5}{3}\bar{I}_{out} = 833.3\text{mA}, \quad (2)$$

and requires a filter inductor of

$$L_f = \frac{V_{in}D(1-D)}{f_s \Delta I_{L_f}} = 675\text{nH}. \quad (3)$$

Allowing for a 2% peak to peak ac ripple in the output voltage,

$$C_f \approx \frac{25\Delta I_{L_f}}{3f_s} = 13.9\mu\text{F} \quad (4)$$

is selected.

To slow the inverter node transitions, a snubber capacitor is added at V_x. The total capacitance required to achieve $\tau_{x_{LH}} = 0.1T_s = 100\text{ns}$ is

$$C_x = \frac{\bar{I}_{out}}{15V_{in}f_s} = 5.56\text{nF} \quad (5)$$

where C_x includes the snubber and all parasitic capacitance at the inverter node, V_x.

III. Adaptive Dead-Time Control

To ensure ideal ZVS of the power transistors, each dead-time when neither device conducts, τ_D, must equal the corresponding inverter node transition time:

$$\begin{aligned} \tau_{D_{LH}} &= \tau_{x_{LH}} \\ \tau_{D_{HL}} &= \tau_{x_{HL}}. \end{aligned} \quad (6)$$

In practice, the relationships of (6) may not always hold true. As indicated by Figure 2, the inductor current ripple is symmetric about the average load current. As the average load varies, the dc component of the I_{L_f} waveform is shifted, and the current available for commutating the inverter node, and ultimately, the inverter node transition time, is modified.

In one approach to soft-switching, a value of average load may be assumed, yielding estimates of the inverter node transition times. Gate delays are then used to determine fixed dead-times based on these estimates. In this way, switching loss is reduced, yet perhaps not to negligible levels. To keep switching losses at a reasonable level in these circuits, they must be operated at lower frequencies, thereby increasing the size of the passive filter components, and decreasing the power density.

In portable, battery-operated applications where area and battery-life are at a premium, this approach to soft-switching may not be adequate. To illustrate the potential hazards of fixed dead-time operation, Figure 3 shows the impact of non-ideal ZVS on conversion efficiency through reference to a high to low transition at the inverter node. In Figure 3a, $\tau_{x_{HL}} > \tau_{D_{HL}}$, causing the rectifier turn-on to occur at $V_{ds_2} > 0$, partially discharging C_x through a resistive path and introducing losses. In Figure 3b, $\tau_{x_{HL}} < \tau_{D_{HL}}$, such that the inverter node rings below zero

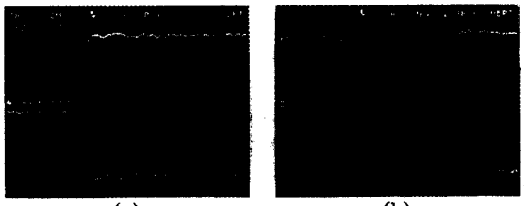

Fig. 3. Non-ideal ZVS and its impact on conversion efficiency. The upper trace is V_{g2}, the lower trace is V_x, the vertical scale is 2 V/div, and the horizontal scale is 20 ns/div.

until the drain-body junction of $M2$ becomes forward biased. In low-voltage applications, the forward-bias diode voltage is a significant fraction of the output voltage; thus, body diode conduction must be avoided for efficient operation. When the rectifier ($M2$) turns on, it must remove the excess minority carrier charge from the body diode and charge the inverter node back to ground, dissipating additional energy.

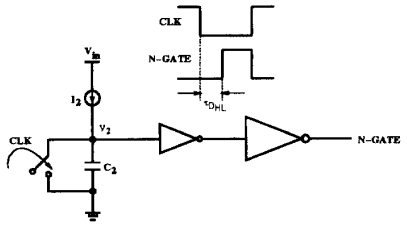

Fig. 4. Variable turn-on delay generator for the rectifier.

To provide effective ZVS over a wide range of loads, an adaptive dead-time control scheme is outlined here. Figures 4 and 5 show the $\tau_{D_{HL}}$ generator and adaptation scheme. Assuming the dead-time is large compared to an inverter delay:

$$\tau_{D_{HL}} \approx \frac{C_2 V_M}{I_2}, \quad (7)$$

where V_M is the switching threshold of an inverter.

To make the dead-time control scheme adaptive, current source I_2 is adjusted based on the relative timing of V_x and V_{gs_2}. In Figure 5, an error voltage proportional to the difference between $\tau_{x_{HL}}$ and $\tau_{D_{HL}}$ is generated on integrating capacitor C_I. The error voltage is sampled and held, and used to update I_2 in the variable turn-on delay generator of Figure 4. Using this technique, effective ZVS is ensured over a wide range of operating conditions and process variations. A nearly ideal ZVS high to low inverter node transition is shown in Figure 6.

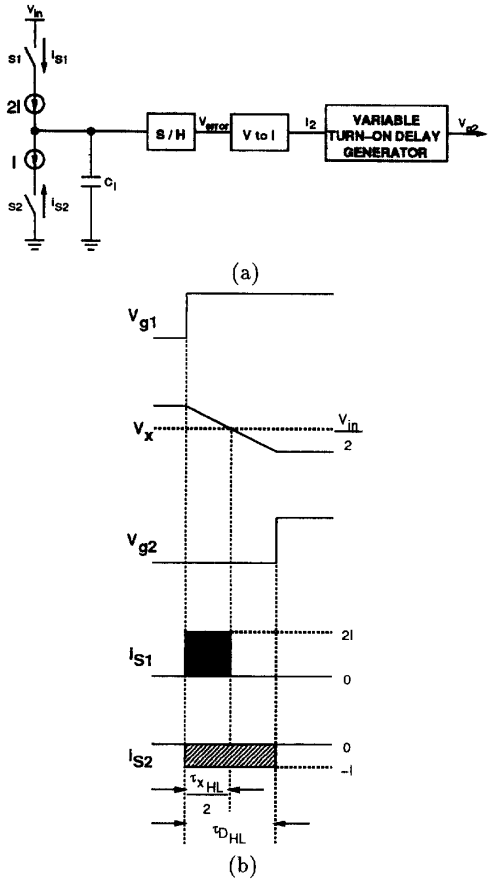

Fig. 5. Rectifier turn-on delay adjustment loop: (a) possible circuit implementation, (b) associated waveforms.

IV. FET Design

During their conduction intervals, the power transistors operate exclusively in the ohmic region, where $r_{ds} = R_0 \cdot \frac{1}{W}$ (the channel resistance is inversely proportional to gate-width, W, with constant of proportionality R_0). Thus, conduction loss in the FET, Mj, is given by

$$P_{q_j} = \frac{I^2_{D_j-rms} R_0}{W_j}. \quad (8)$$

It is further assumed that the power transistors exhibit ideal lossless zero-voltage switching. Therefore, their gate-drain (Miller) and drain-body capacitance are switched with negligible loss. Since the gate capacitance increases linearly with increasing gate width ($C_g = C_{g0}W$), and the power consumed by the gate-drive buffers varies linearly with the capacitive load, the gate-drive dissipation due to

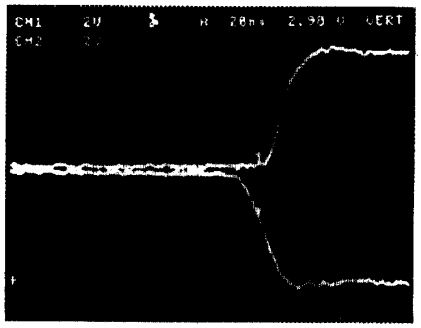

Fig. 6. A zero-voltage-switched high to low inverter node transition. The vertical scale is 2 V/div; the horizontal scale is 20 ns/div.

Mj is of the form:

$$P_{g_j} = E_{g0} f_s W_j, \quad (9)$$

where E_{g0} is the total gate-drive energy consumed in a single low-high-low gate transition cycle. Using an algebraic minimization [9], the optimal gate width of Mj,

$$W_{j-opt} = \sqrt{\frac{I^2_{D_j-rms} R_0}{E_{g0} f_s}} \quad (10)$$

is found to give equal conduction loss and gate-drive loss, where:

$$P_{q_j-opt} = P_{g_j-opt} = \sqrt{I^2_{D_j-rms} R_0 E_{g0} f_s} \quad (11)$$

and $P_{q_j} + P_{g_j}$ is at its minimum.

The layout of the power transistors is discussed in section VI.

V. Gate-Drive

In CMOS circuits, a power transistor is conventionally driven by a chain of N inverters which are scaled with a constant tapering factor, u, such that

$$u^N = \frac{C_g}{C_i}. \quad (12)$$

Here, C_g is the gate capacitance of the power transistor and C_i is the input capacitance of the first buffering stage. This scheme, depicted in Figure 7, is designed such that the ratio of average current to load capacitance is equal for each inverter in the chain. Thus, the delay of each stage and rise/fall time at each node are identical. It is a well known result that under some simplifying assumptions, the tapering factor u that produces the minimum propagation delay is the constant e [10]. However, in power

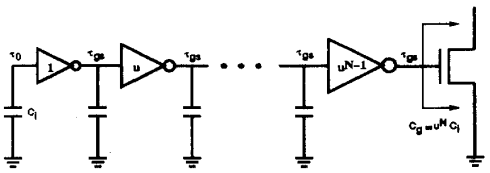

Fig. 7. CMOS gate-drive scheme.

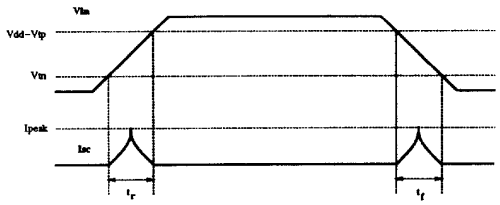

Fig. 8. Short-circuit current in an inverter.

circuits, the chief concern lies not in the propagation delay of the gate-drive buffers, but the energy dissipated during a gate transition.

In a ZVS power circuit, the following timing constraints are desired:

$$\tau_x \gg \tau_{gs} \approx u\tau_0 \tag{13}$$

where τ_x is the inverter node transition time, τ_{gs} is the maximum gate transition time which ensures effective ZVS of the power transistor, τ_0 is the output transition time (rise/fall time) of a minimal inverter driving an identical gate, and u is the tapering factor between successive inverters in the chain. In general, it is desirable to make τ_{gs} as large as possible (yet still a factor of five to ten less than τ_x), minimizing the gate-drive dissipation. Given τ_{gs} and τ_0, if there exists some $u > e$ such that the criteria given by (13) are met, the buffering scheme of Figure 7 will provide a more energy efficient CMOS gate-drive than that obtained through minimization of delay.

A. Determination of the Inverter Chain

In this analysis, a minimal CMOS inverter has an NMOS device with minimum dimensions (W_o/L) and a PMOS device whose gate width is $\mu_n/\mu_p \approx 3$ times that of the NMOS device. It has lumped capacitances C_i at its input and C_o at its output. Given that the pull-down device operates exclusively in the triode region during the interval of interest, it can be shown that the output fall time of a minimal inverter driving an identical gate from $V_{out} = V_{dd} - |V_{tp}|$ to $V_{out} = V_{tn}$ is:

$$t_f \equiv \tau_0 = \frac{C_o + C_i}{W_o} K, \tag{14}$$

which is linearly proportional to the capacitive load, inversely proportional to the gate-width of the n-channel device, and directly related to the application and technology dependent constant:

$$K \equiv \frac{2L}{\mu_n C_{ox}(V_{dd} - V_{tn})} \bullet \ln\left[\frac{(2V_{dd} - 3V_{tn})}{(V_{tn})} \frac{(V_{dd} - V_{tp})}{(V_{dd} - 2V_{tn} + V_{tp})}\right]. \tag{15}$$

A similar expression can be found for the rise time.

The factor u which results in an output transition time τ_{gs} is found by solving:

$$\tau_{gs} = \frac{K(C_o + uC_i)}{W_0} \approx u\tau_0, \tag{16}$$

yielding a corresponding tapering factor of

$$u = \frac{\tau_{gs} W_0 - KC_o}{KC_i} \tag{17}$$

between successive buffers. Given u, the number of inverters in the chain is:

$$N = \frac{\ln(C_g/C_i)}{\ln(u)}. \tag{18}$$

The inverter chain guarantees a gate transition time of τ_{gs} with minimum dissipation, and a propagation delay of

$$t_p \approx N u t_{p0} \tag{19}$$

where t_{p0} is the propagation delay of a minimal inverter loaded by an identical gate.

B. Loss Analysis

There are two components of power dissipation in the inverter chain:

$$P_{dyn} = C_T V_{dd}^2 f_s \tag{20}$$

$$P_{sc} = \sum_{i=1}^{N} \bar{I}_{sc_i} V_{dd} \tag{21}$$

where $\bar{I}_{sc_i}$ is the mean short-circuit current in the i^{th} inverter in the chain, and the total switching capacitance, including the load, is

$$\begin{aligned} C_T &= (1 + u + u^2 + \cdots + u^{N-1})(C_o + C_i) + C_g \\ &= \left[\frac{u^N - 1}{u - 1}\right](C_o + C_i) + C_g. \end{aligned} \tag{22}$$

Since u^N is the constant given by (12), C_T and thus, the dynamic dissipation, is minimized for large u.

Though the dynamic component is readily calculated from (20) and (22), the short-circuit dissipation is more

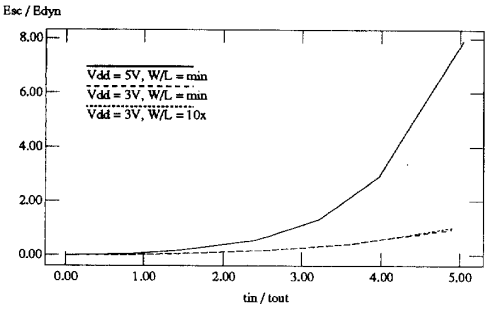

Fig. 9. Short-circuit energy versus input transition time.

difficult to quantify. From Figure 8, it can be seen that short-circuit current exists in a CMOS inverter while the n- and p-channel devices conduct simultaneously ($V_{tn} < V_{in} < V_{dd} - |V_{tp}|$), and the total energy consumed during an input transient is proportional to both the input transition time and the peak short-circuit current (which in turn, is related to the output transition time [11]). Figure 9 plots simulation results of the ratio of short-circuit to dynamic dissipation per cycle versus the ratio of input to output transition times for a minimal inverter operated at V_{dd} =5V and V_{dd} =3V, and a ten times minimal inverter operated at V_{dd} =3V. These results illustrate three key points regarding short-circuit dissipation in a CMOS inverter:

- The normalized E_{sc} is seen to increase exponentially with normalized input edge rate, but is negligible for equal input and output transition times.
- While the magnitude of short-circuit current is dependent on device dimensions (I_{peak} increases linearly with device size), the ratio of E_{sc} to E_{dyn} appears to be independent of size.
- For $V_{dd} \gg V_t$, there is an approximately linear increase in E_{sc} with increasing supply voltage. While the duration of short-circuit current flow decreases linearly, the magnitude increases quadratically.

Therefore, because the tapering factor u is constant throughout the inverter chain, providing equal transition times τ_{gs} at each node, the short-circuit dissipation is made negligible. Furthermore, for $u > e$, less silicon area will be devoted to the buffering; thus parasitics, and ultimately, dynamic energy loss, are reduced as compared to the conventional CMOS gate-drive.

To make a first-order estimate of the total gate-drive loss as a function of power transistor gate width, (20), (21), and (22) are used in conjunction with the values of u and N derived in subsection A, giving:

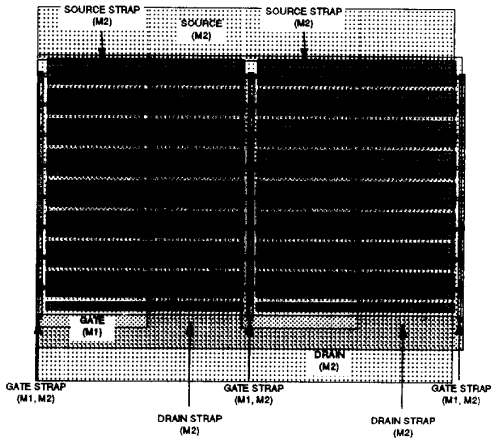

Fig. 10. Layout of a power PMOS device.

$$P_g \approx WC_{g0}V_{in}^2 f_s \bullet \left[\frac{K(C_o + C_i)}{\tau_{gs}W_o - KC_o - KC_i} + 1\right] \quad (23)$$

for a power transistor of gate-width W. To obtain (23), it is assumed that all capacitances increase linearly with gate-width and $u^N \gg 1$. In this way, gate-drive losses are expressed as a linear function of gate-width, identical in form to (9).

VI. Layout and Packaging Issues

The power transistors are arrayed as a number of parallel fingers whose gates are strapped in metal1 and metal2 (Figure 10). The length of each finger is determined by the maximum tolerable distributed RC delay of the gate structure. In order to reduce series source and drain resistance, the diffusion is heavily contacted, with source-body and drain running horizontally in metal1, and vertically in metal2. Because the ZVS of the power devices effectively eliminates their drain-body junction capacitance switching losses, increased drain diffusion area is traded for more reliable and efficient body diode conduction. Rather than sharing diffusion between adjacent fingers in the layout, well contacts are placed at a minimum distance from drain contacts, minimizing both the series resistance and transit time [12] of the body diode. Due to the potentially large magnitude of substrate current injection, healthy well contacts are placed throughout the structure. A guard ring surrounds each power device, eliminating latch-up and decoupling the ground and V_{dd} bounce from the analog regulation circuitry that can result from substrate current injection.

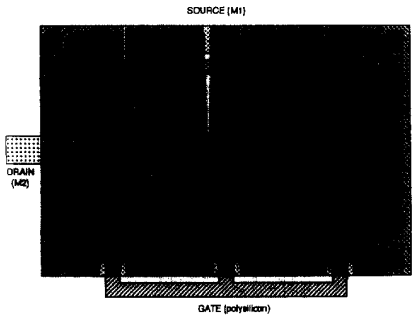

Fig. 11. Ring structure layout in the gate-drive buffers.

In contrast to the power transistors, the ideal layout of the gate-drive buffers minimizes their output diffusion capacitance. Thus, drain diffusion is shared wherever possible. For the larger buffers, a ring structure is employed [13]. In this scheme, illustrated in Figure 11, the gate polysilicon of two adjacent fingers is connected inside the diffusion, forming a ring of polysilicon which maximizes gate-width for a given drain diffusion area. The diffusion surrounding the ring is chosen to be the source of the device, leaving the small diffusion area within the ring as the drain. Not only is the drain area capacitance at a minimum for a given gate-width in this structure, but the sidewall capacitance, typically the dominant factor in processes with a sub-micron feature size, is completely eliminated.

In this design, the critical problems associated with packaging effects are the stray inductances in series with loop formed by the input decoupling capacitor C_{in} and the power FETs ($L_s I^2 f_s$ loss), and series resistance in V_{in}, ground, and the inverter node (I^2R loss). Therefore, a large number of pins are dedicated to reduce loss in the package: 14 V_{in} pins, 13 ground pins, and 16 inverter node pins. Because the power transistors are operated in a ZVS scheme, the pin capacitance at the inverter node is used as snubber capacitance and does not contribute additional loss.

VII. Measured Results

A prototype IC (Figure 12) was fabricated in a standard 1.2μ CMOS process through the MOSIS program. The circuit delivers 750mW at 1.5V from a 6V battery. Figure 13 shows the steady-state V_{g1}, V_{g2}, I_{L_f}, and V_x waveforms at full load. Tables 1 and 2 summarize the features of the prototype design and report the sources of dissipation.

While power transistor gate-drive and conduction loss are balanced and predicted well by theory and simulation, the measured efficiency of 79% at full load is substantially lower than anticipated. This can be attributed to several factors. First, due to an undetected layout error in the turn-on delay generators, dead-time adjustment was achieved at the board level with a biasing resistor. Because of the associated increase in capacitive parasitics over the monolithic implementation, comparatively large static currents were required to obtain the desired dead-times. Thus, the power consumption of the ADTC circuitry was greater than an order of magnitude larger than anticipated, comprising nearly 30% of the overall loss. Secondly, throughout the design, efficiency was traded for testability: a number of intermediate signals were brought off-chip at the expense of additional switching capacitance, resulting in a severe penalty in dynamic power consumption. For example, the dissipation of the VCO increased by a factor of three in order to enhance its testability. Finally, a major component of loss is accredited to the package. In particular, the series resistance in the V_{in}, ground, and V_x bonding wires contributed a total of 47.3mW of loss (28% of the total loss), and the stray inductance in the loop formed by the input decoupling capacitor and the power transistors contributed an additional 20mW of loss (10% of total loss). These components of dissipation will virtually be eliminated using a custom lead frame in an MCM or chip-on-board (COB) technology.

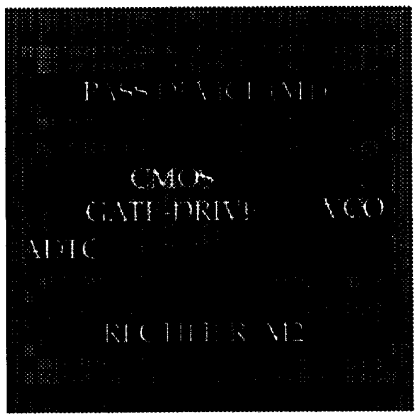

Fig. 12. Chip photograph: 6V to 1.5V 750mW DC-DC converter. Die size = 4.2mm × 4.2 mm.

The results measured on the prototype indicate that in this circuit, on-chip losses (including losses in the power transistors, and regulation and control circuitry) can be kept below 8% at full load. With a custom package, an efficiency greater than 90% may be achieved. The approach presented is evidently viable for realizing a high efficiency and compact power converter for portable battery-operated applications. When completed, this circuit would require one custom IC, three small ceramic chip capacitors, and a small inductor. The inductor might be

realized with a multi-turn air-core spiral in a custom substrate.

Table 1: Prototype Design Summary

Technology	1.2μ CMOS
	1 poly, 2 metal
Gate Oxide Thickness	21.4 nm
Minimum Gate Length	$L_{eff} = 0.9\mu$
Filter Inductor	$L_f = 675$ nH
Filter Capacitor	$C_f = 20\ \mu$F
Off-chip Snubber Capacitor	$C_{snubber} = 4$ nF
$M1$ Gate Width	$W_1 = 10.2$ cm
$M1$ Buffering	$u = 5.2$
	$N = 4$
$M2$ Gate Width	$W_2 = 10.5$ cm
$M2$ Buffering	$u = 8.7$
	$N = 4$
Operating Frequency	$f_s = 1$ MHz
Battery Input Voltage	$V_{in} = 6$ V
Output Voltage	$V_{out} = 1.5$ V
Output Power at Full Load	$P_{out} = 750$ mW
Predicted Efficiency at Full Load (Unpackaged)	92%
Measured Efficiency at Full Load (Packaged)	79%

Table 2: Sources of Dissipation

	$M1$	$M2$
Gate-Drive Loss	11.2 mW	13.9 mW
Channel r_{ds} Conduction Loss	10.1 mW	14.0 mW
Bonding r_{ds} Conduction Loss	5.1 mW	42.2 mW
Total Loss	3.5 %	9.3 %
L_s Stray Inductance		$\approx$ 20 mW
L_f Series Resistance		16.9 mW
C_f esr		2.3 mW
C_{in} esr		$<$ 1 mW
VCO (On-chip and Off-chip Pins)		6.2 mW
ADTC (Off-chip)		48.4 mW

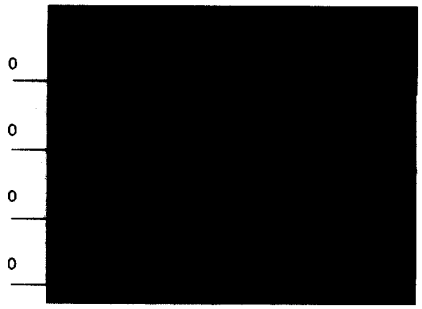

Fig. 13. Measured steady-state waveforms: V_{g2}, V_{g1}, I_{L_f}, V_x (top to bottom). The horizontal scale is 20 ns/div. The vertical scale is 2 V/div for the voltage waveforms, and 1 A/div for the inductor current waveform.

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