Analysis and Optimization of Switched-Capacitor DC–DC Converters

Michael D. Seeman, *Student Member, IEEE*, and Seth R. Sanders, *Member, IEEE*

***Abstract*—Analysis methods are developed that fully determine a switched-capacitor (SC) dc–dc converter's steady-state performance through evaluation of its output impedance. This analysis method has been verified through simulation and experimentation. The simple formulation developed permits optimization of the capacitor sizes to meet a constraint such as a total capacitance or total energy storage limit, and also permits optimization of the switch sizes subject to constraints on total switch conductances or total switch volt-ampere (V-A) products. These optimizations then permit comparison among several switched-capacitor topologies, and comparisons of SC converters with conventional magnetic-based dc–dc converter circuits, in the context of various application settings. Significantly, the performance (based on conduction loss) of a ladder-type converter is found to be superior to that of a conventional magnetic-based converter for medium to high conversion ratios.**

***Index Terms*—Analysis, dc–dc converter, output impedance, switched-capacitor.**

I. Introduction

THIS paper develops analysis methods that fully determine a switched-capacitor (SC) dc–dc converter's steady-state performance through evaluation of its output impedance. This resistive impedance is a function of frequency and has two asymptotic limits: one where resistive paths dominate the impedance, and another where charge transfers among idealized capacitors dominate the impedance. This work develops a network theoretic analysis of these two asymptotic limits, which can be used to evaluate both the converter efficiency and output regulation as a function of load for a broad class of SC converters. Simulations and experiments have been performed to verify the analysis methods.

The comprehensive analysis and design calculations given here are new, but connect with the analysis framework developed in the pioneering work of [1]. The work in [1], [2] offered a network theoretic formulation for computation of open-circuit dc–dc conversion ratios, and a rather involved method for computation of output impedance. Reference [1] and other previous analysis work [3]–[7] mainly focused on the performance analysis (i.e., output impedance computation) for a single converter topology.

The simple formulation developed permits optimization of the capacitor sizes to meet a constraint such as a total capacitance or total energy storage limit, and also permits optimization of the switch sizes subject to constraints on total switch conductances or total switch volt-ampere (V-A) products. These optimizations are carried out for a set of representative switched-capacitor topologies. These optimizations then permit comparison among several switched-capacitor topologies, and comparisons of SC converters with conventional magnetic-based dc–dc converter circuits. The performance (based on conduction loss) of a ladder-type converter is found to be superior to that of a conventional boost converter for medium to high conversion ratios.

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The authors are with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720 USA (e-mail: mseeman@eecs.berkeley.edu).

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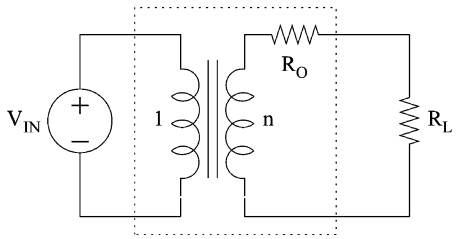

Fig. 1. Model of an idealized switched-capacitor converter.

II. Switched-Capacitor Converter Impedance Analysis

With the model in Fig. 1, the converter provides an ideal dc voltage conversion ratio under no load conditions, and all conversion losses are manifested by voltage drop associated with non-zero load current through the output impedance [1], [5]. The resistive output impedance accounts for capacitor charging and discharging losses and resistive conduction losses. Additional losses due to short-circuit current and parasitic capacitances, in addition to gate-drive losses, can be incorporated into the model. However, they will not be considered here since these effects are generally application and implementation dependent. Insight gained can be used to model effects of parasitic capacitances [8]. For the present, our aim is to provide a general analysis and design framework.

The low-frequency output impedance R_O in Fig. 1 sets the maximum converter power, constrained by a minimal efficiency objective, and also determines the open-loop load regulation properties. There are two asymptotic limits to output impedance, the slow and fast switching limits, as related to switching frequency. The slow switching limit (SSL) impedance is calculated assuming that the switches and all other conductive interconnects are ideal, and that the currents flowing between input and output sources and capacitors are impulsive, modeled as charge transfers. The SSL impedance is inversely proportional to switching frequency. The fast switching limit (FSL) occurs when the resistances associated with switches, capacitors and interconnect dominate, and the capacitors act

effectively as fixed voltage sources. In the FSL, current flow occurs in a frequency-independent piecewise constant pattern.

The set of converters considered in this paper is limited to two-phase converters made solely of ideal capacitors, resistive switches, and input and output voltage sources. Two-phase converters switch alternately between two configurations. Multiphase converters [4] are outside the scope of this paper, but can be considered using similar methods. This paper does not address the more fundamental topological conditions needed to determine whether or not a specific circuit constitutes a well-formulated two-phase converter. Rather, the paper assumes that the circuits under consideration all have well-defined two-phase operation. References [1], [2] begin to address the topological question of what constitutes a well-formulated two-phase SC dc–dc circuit, though the characterization given is not complete.

A. Slow-Switching Limit Impedance

For the slow-switching limit (SSL) impedance analysis, the finite resistances of the switches, capacitors, and interconnect are neglected. A pair of charge multiplier vectors $\boldsymbol{a^1}$ and $\boldsymbol{a^2}$ can be derived for any standard non-degenerate two-phase SC converter. The charge multiplier vectors correspond to charge flows that occur immediately after the switches are closed to initiate each respective phase of the SC circuit. Each element of a charge multiplier vector corresponds to a specific capacitor or independent voltage source, and represents the charge flow into that component, normalized with respect to the output charge flow. As outlined in [1], the charge multiplier vectors can be uniquely computed using the KCL constraints in each topological phase and the constraint that the two charge multiplier quantities on each capacitor are equal and opposite.

The charge multiplier vector $\boldsymbol{a^1}$ is defined as

$$\boldsymbol{a^1} = [\, q^1_{\rm out} \quad q^1_1 \quad \cdots \quad q^1_n \quad q^1_{\rm in} \,]^\top / q_{\rm out} \tag{1}$$

where each component is the ratio of charge transfer in each element during phase 1 of the switching period to the charge delivered to the output during a full period. If charge flows into the element during phase 1, the corresponding entry in the $\boldsymbol{a^1}$ vector is positive. Vector $\boldsymbol{a^2}$ is defined analogously, for phase 2. The charge multiplier vector can be partitioned into output, capacitor and input components, respectively

$$\boldsymbol{a^1} = [\, a^1_{\rm out} \quad \boldsymbol{a^1_c} \quad a^1_{\rm in} \,]^\top. \tag{2}$$

For the ladder network example of Fig. 2, the charge multiplier vectors can be obtained through network analysis using Kirchoff's Current Law (KCL) [1]. In this example, and in all other examples encountered by the authors, the charge multiplier vectors can be obtained by inspection (in Fig. 3). The charge from the input source flows into C4 during phase 2. In phase 1, that charge is transferred into C3. By considering alternating phases, the charge flow in each component can be found

$$\boldsymbol{a^1} = [\, 2/3 \quad -2/3 \quad 1/3 \quad -1/3 \quad 0 \,]^\top \tag{3}$$
$$\boldsymbol{a^2} = [\, 1/3 \quad 2/3 \quad -1/3 \quad 1/3 \quad -1/3 \,]^\top. \tag{4}$$

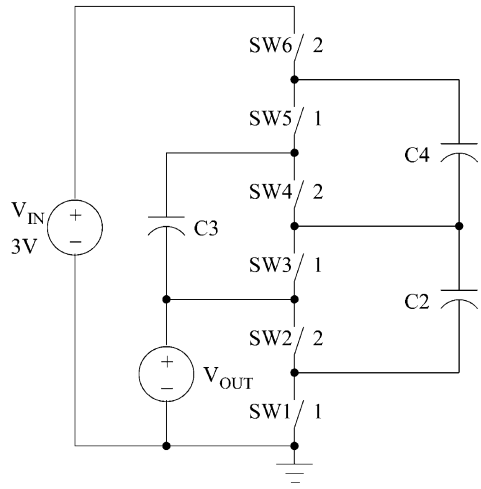

Fig. 2. 3 V to 1 V ladder circuit.

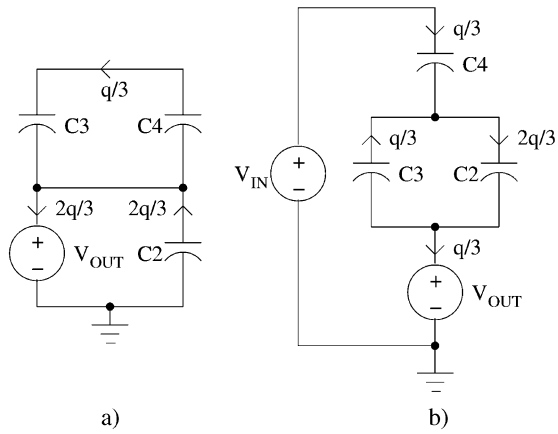

Fig. 3. Charge flow in ladder converter. (a) phase 1 (b) phase 2.

In each of these charge multiplier vectors, the first component corresponds to the output charge flow, thus these two components must sum to one. The last component of each charge multiplier vector corresponds to the charge flow into the input source, and is non-zero during only phase 2 in this example.

The charge multiplier vectors, the capacitor characteristics, and the switching frequency are the only data needed to determine the output impedance under the asymptotic SSL condition. The calculation, developed here, is based on Tellegen's Theorem [9] which states that for any network, any vector of branch voltages that satisfies KVL is orthogonal to any vector of branch currents (or equivalently charge flows) that satisfies KCL. This theorem is applied in each of the two configurations for a two-phase switched capacitor converter operating in periodic steady state, where the input is short-circuited and the output is connected to an independent dc voltage source. The charge flow per period (or average current flow) into the single independent source then defines the output impedance.

Application of Tellegen's theorem to the switched capacitor converter, in each of its two configurations, yields $\mathbf{a}^1 \cdot \mathbf{v}^1 = \mathbf{0}$ and $\mathbf{a}^2 \cdot \mathbf{v}^2 = \mathbf{0}$, where $\mathbf{v}^1$ and $\mathbf{v}^2$ are the respective steady

state network voltage vectors in phases 1 and 2. Additively combining these two applications of Tellegen's theorem, and noting that the input voltage source has value zero, yields

$$v_{\text{out}}\left(a^1_{\text{out}}+a^2_{\text{out}}\right)+\sum_{\text{capacitors}}\left(a^1_{c,i}v^1_{c,i}+a^2_{c,i}v^2_{c,i}\right)=0 \quad (5)$$

where the first term corresponds to the constant output voltage source and the terms under the summation correspond to the capacitor branches. Recall that $a^1_{\text{out}}+a^2_{\text{out}}=1$ and that $a^1_{c,i}=-a^2_{c,i}$ for each capacitor branch (due to charge conservation in periodic steady-state). By defining $a_{c,i}=a^1_{c,i}=-a^2_{c,i}$ and $q_i=a_{c,i}q_{\text{out}}$ and multiplying (5) by q_{out}, the net charge delivered to the output in a period, we obtain

$$q_{\text{out}}v_{\text{out}}+\sum_{\text{capacitors}}q_i\Delta v_i=0 \quad (6)$$

where $\Delta v_i=v^1_{c,i}-v^2_{c,i}$. In (6), the first term corresponds to the product of the constant output voltage and the total charge flow into this independent voltage source, and each term in the summation corresponds to energy loss associated with a specific capacitor. It is of direct interest here that none of the capacitor voltages need to be explicitly calculated for this analysis. Rather, Δv_i can be computed from

$$\Delta v_i=q_i/C_i \quad (7)$$

where C_i is the capacitance value of the ith capacitor, assuming linear capacitors. Introducing (7) into (6), and then dividing the result by q^2_{out} yields

$$\frac{v_{\text{out}}}{q_{\text{out}}}+\sum_{\text{capacitors}}\left(\frac{q_i}{q_{\text{out}}}\right)^2\frac{1}{C_i}=0. \quad (8)$$

We note that q_i/q_{out} corresponds to the ith entry of the charge multiplier vector $\boldsymbol{a_c}$, since these entries are for the capacitors. Dividing (8) by the switching frequency then directly yields the average output impedance for the slow-switching asymptotic limit

$$R_{\text{SSL}}=-\frac{v_{\text{out}}}{i_{\text{out}}}=\sum_i\frac{(a_{c,i})^2}{C_i f_{\text{sw}}}. \quad (9)$$

The converter's loss in terms of the series output impedance R_{SSL} can be expressed in terms of capacitor loss. The product $q_i\Delta v_i$ in (6) represents the energy loss by charging and discharging capacitor i in each cycle, and could be used to calculate the converter's loss even with a nonlinear capacitor. In the following discussion, attention is restricted to the case of linear capacitors. The sum of the energy lost through the capacitors is equal to the calculated loss associated with the output impedance for a given load.

This powerful result yields a simple calculation of this asymptotic output impedance and some intuition into the operation of SC converters. The output impedance directly models the losses in the circuit due to capacitor charging and discharging. This impedance can be determined by simply examining the charge flow in the converter without simulation or complicated network analysis.

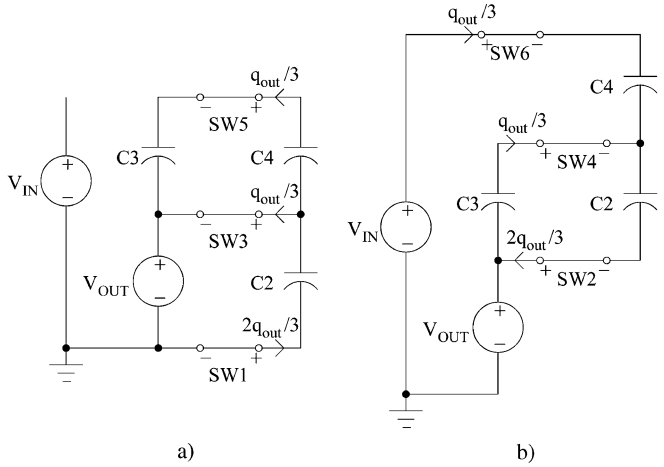

Fig. 4. Switch charge flow in ladder converter. (a) Phase 1, (b) Phase 2.

B. Fast Switching Limit Impedance

The other asymptotic limit, the fast switching limit (FSL), is characterized by constant current flows between capacitors. The switch on-state impedances and other resistances are sufficiently large such that during each phase, the capacitors do not approach equilibrium. In the asymptotic limit, the capacitor voltages are modeled as constant. The circuit loss is related only to conduction loss in resistive elements. The concept of the FSL impedance is introduced informally in [5].

The duty cycle of the converter is important when considering the FSL impedance since currents flow during the entirety of each phase. For this analysis, a duty cycle of 50% is assumed for simplicity. Duty cycle differing from 50% can be included in the following analysis without much difficulty if another duty cycle is used. Additionally, only the on-state switch resistance is considered; other parasitic resistance [e.g., capacitor equivalent series resistance (ESR)] can be similarly incorporated into the model if desired.

The $a_{r,i}$ values are defined as the charge flow through each switch during the phase in which the switch is on. Even in the FSL, the charge flows must follow the same pattern as in the SSL, constrained by $\boldsymbol{a^1}$ and $\boldsymbol{a}^2$. For the switches that are on during phase 1, the corresponding $a_{r,i}$ values can be determined from the $\boldsymbol{a^1}$ components. Analogously, corresponding $a_{r,i}$ values for switches that conduct during phase 2 can be determined from the $\boldsymbol{a^2}$ components. The values of $a_{r,i}$ are independent of duty cycle as they simply represent the charge flow through the switches that ensure charge conservation on the circuit's capacitors. The $a_{r,i}$ values for the switches in the ladder converter in Fig. 2 can be determined directly. The charge flows in the switches during both phases are shown in Fig. 4, resulting in an a_r vector of

$$\boldsymbol{a_r}=[-2/3 \quad -2/3 \quad 1/3 \quad 1/3 \quad 1/3 \quad 1/3]. \quad (10)$$

For positive power flow (i.e., from the input to output source), the sign of each component of the $\boldsymbol{a_r}$ vector indicates the direction of current flow with respect to the blocking voltage of a switch. A positive quantity indicates the switch conducts positive current while on and blocks positive voltage while off. This switch must be implemented using an active transistor. A negative quantity indicates the switch conducts negative current and blocks positive voltage and is suitable for diode implementation (if the forward voltage drop is tolerable). For power flow in the opposite direction, the switch types reverse.

In the FSL, the current through the on-state switches is assumed to be constant. Given the charge flow vector, the current in each switch is easily determined

$$i_{r,i} = 2q_{r,i}f_{\rm sw} \tag{11}$$

where $q_{r,i}$ is the charge flow through switch i during a single period. The factor of two appears because of the 50% duty cycle. Substituting $q_{r,i} = a_{r,i}q_{\rm out}$ and $q_{\rm out} = i_{\rm out}/f_{sw}$ into (11) yields

$$i_{r,i} = 2a_{r,i}i_{\rm out}. \tag{12}$$

The current through the switches is only dependent on the vector $\boldsymbol{a_r}$, which is obtainable by inspection. The network voltages never need to be found in this analysis, simplifying computation significantly.

The average power loss due to each individual switch is equal to the instantaneous on-state power loss multiplied by its duty cycle. Since the total loss of the SC converter in the FSL is just the sum of the switch losses, the total circuit loss is given by

$$P_{\rm FSL} = \sum_{\rm switches} \frac{1}{2}R_i(2a_{r,i}i_{\rm out})^2 \tag{13}$$

where R_i is the on-state resistance of switch i.

Since the input and output charge flow in the SC converter is constrained by the conversion ratio n, all the power loss in an ideal SC converter (as analyzed here) is modeled by the output voltage drop. Thus the output impedance can be determined by equating the actual power loss of the circuit with the apparent power loss due to the output impedance. Since this power loss is proportional to the square of the output current, the FSL output impedance can be obtained by inspection

$$R_{\rm FSL} = 2\sum_i R_i(a_{r,i})^2. \tag{14}$$

Similar to the SSL output impedance in (9), the FSL output impedance is given simply in terms of component parameters and the switch charge multiplier coefficients of each switch. The power loss due to these conduction losses is equal to the equivalent power loss through the output impedance. These two simple forms of the output impedance (given in (9) for the SSL and (14) for the FSL) can be used to provide strong guidance for the design of switched-capacitor power converters.

III. Component Optimization

Given that all converter losses attributed to the capacitors and resistive switches can be reflected in the computation of a single real output resistance, it is now possible to optimize the components in order to minimize that output impedance. Minimal output impedance corresponds to maximum efficiency for a given power delivered, and dually, corresponds to maximum power delivery for a given loss. This section develops optimality computations for the slow switching limit (SSL) and the fast switching limit (FSL) impedance. When optimizing over capacitances, one should minimize the output impedance that is associated only with the capacitances, namely the SSL impedance. Analogously, when optimizing over switch sizes, one should minimize the FSL output impedance. The final design step is to choose a maximum operating frequency for which the parasitic losses are acceptable. The total capacitance and switch conductance should be adjusted such that the total impedance meets the design goal and the SSL and FSL impedances are balanced. The last step ensures that the total switch and capacitor sizes (and costs) are minimized for the intended power level.

The optimization procedure requires knowledge of the component working voltages, unlike the output impedance analysis. The working voltage for a capacitor is the maximum voltage on the capacitor during steady-state converter operation. For a transistor (switch), the working voltage is the voltage it blocks during steady-state converter operation. For open-circuit operation, these working voltages can be found by inspection in most examples, or by the process outlined in [1]. This analysis is based on combining KVL constraints for the two phase topologies, in combination with a known source voltage. The result is the computation of vectors denoted v_c and v_r for the working voltages of the capacitors and switches, respectively, ratioed to the converter output voltage.

The optimization is based on a physical size (or cost) constraint for the devices. When capacitors are optimized, their total energy storage capability is held constant. Or, in the case when all capacitors must be rated for the same voltage, the total capacitance is held constant. Likewise, when the switch sizes are optimized, the total V-A capacity product is held constant. This V-A metric translates to a constraint on the G-$\rm V^2$ products summed over the switches (G refers to switch conductance). If all the switches are rated for the same voltage, the constraint reduces to holding the sum of the switch conductances constant.

A. SSL Capacitor Optimization

The capacitor optimization uses a constraint that holds the total energy storage capability, summed over all capacitors, fixed to a constant $E_{\rm tot}$. This constraint can be mathematically expressed as

$$\sum_i \frac{1}{2}(v_{c,i({\rm rated})})^2 C_i = E_{\rm tot} \tag{15}$$

where C_i represents the value of capacitor i and $v_{c,i({\rm rated})}$ represents the rated voltage of capacitor i. The energy storage capability of a capacitor is related to its rated voltage, as that dictates its size and cost, not the maximum voltage it sees during operation. However, the capacitor's working voltage must be less than the rated voltage to avoid damaging the component, and should be close to the rated voltage to achieve good utilization of the device.

A function $\mathcal{L}$ is defined to perform the constrained optimization

$$\mathcal{L} = \sum_i \frac{(a_{c,i})^2}{C_i} + \lambda \left(\sum_i \frac{1}{2} (v_{c,i(\text{rated})})^2 C_i - E_{\text{tot}} \right) \quad (16)$$

where the first term represents the SSL output impedance (scaled by switching frequency as it does not effect the minimization) and the second term incorporates the constraint in (15). The impedance is minimized by equating the partial derivatives of $\mathcal{L}$ with respect to C_i and λ with zero

$$\frac{\partial \mathcal{L}}{\partial C_i} = -\frac{(a_{c,i})^2}{C_i^2} + \lambda \frac{1}{2} (v_{c,i(\text{rated})})^2 = 0 \quad (17)$$

$$\frac{\partial \mathcal{L}}{\partial \lambda} = \sum_i \frac{1}{2} (v_{c,i(\text{rated})})^2 C_i - E_{\text{tot}} = 0. \quad (18)$$

Equation (18) simply repeats the constraint in (15).

The relationship in (17) sets up a proportionality between C_i, $a_{c,i}$, and $v_{c,i(\text{rated})}$. The energy constraint can be used to find an expression for the value of each capacitor

$$C_i = \left| \frac{a_{c,i}}{v_{c,i(\text{rated})}} \right| \frac{2E_{\text{tot}}}{\sum_k |a_{c,k} v_{c,k(\text{rated})}|}. \quad (19)$$

The optimal energy storage of each capacitor is proportional to the V–Q product of each capacitor

$$E_i = \frac{|a_{c,i} v_{c,i(\text{rated})}|}{\sum_k |a_{c,k} v_{c,k(rated)}|} E_{\text{tot}}. \quad (20)$$

When the total energy is constrained, the optimal capacitor energies are proportional to the product of their rated voltage and their charge multiplier coefficients. In addition, the ripple voltage on each capacitor is directly proportional to that capacitor's rated voltage.

The optimized output impedance can be calculated by combining (9) and (19)

$$R_{\text{SSL}}^* = \frac{1}{2E_{\text{tot}} f_{\text{sw}}} \left(\sum_i |a_{c,i} v_{c,i(\text{rated})}| \right)^2. \quad (21)$$

By optimizing the capacitors, the output impedance becomes proportional to the square of the sum of the products of voltages and charge flows (V-A product) of each capacitor. The optimization can improve the performance of an SC converter designed in an ad-hoc manner significantly, especially one with a large conversion ratio.

If all capacitors in a SC converter are rated for the same voltage, as in the ladder topology or in applications with integrated capacitors, the optimization results can be simplified. In this case, we constrain total capacitance to a value of C_{tot}, and the value of each individual capacitor is given by

$$C_i^* = \frac{|a_{c,i}|}{\sum_k |a_{c,k}|} C_{\text{tot}}. \quad (22)$$

Each capacitor is sized proportionally to its charge multiplier coefficient. With optimized capacitors, the voltage ripple on each capacitor is set equal in magnitude.

The optimized SSL output impedance (from (21)) thus simplifies to

$$R_{\text{SSL}}^* = \frac{1}{C_{\text{tot}} f_{\text{sw}}} \left(\sum_i |a_{c,i}| \right)^2. \quad (23)$$

These optimization results for the single-voltage technology are very simple to utilize in switched-capacitor converter design.

B. FSL Switch Optimization and Sizing

Like capacitors, the switches in a SC converter can be optimized, yielding dramatic performance increases. This optimization is carried out in the asymptotic fast switching limit where output impedance is directly related to switch conductance. This optimization assumes a duty cycle of 50%.

The switch VA product, summed over all switches, is used as the cost-based metric in this optimization. This V-A metric corresponds to a constraint on the G-V^2 product summed over the switches, for both discrete and integrated switches. Paralleling discrete switches increases total conductance, whereas placing switches in series increases voltage blocking while decreasing conductance. To increase voltage blocking without reducing conductance, the number of devices used scales quadratically, motivating the G-V^2 metric.

In an integrated application, the same total G-V^2 constraint applies. The transistor length and nominal voltage scale linearly with process feature size. In addition, switch conductance scales proportionally with transistor width and inversely with transistor length. A cost metric A_{sw}, related to the area (or width multiplied by length) of a specific transistor, can be written as $A_{\text{sw}} = GV^2$ (in units of GV^2, i.e., S-V^2).

This constraint, applicable to both discrete and integrated transistors, can be expressed as

$$A_{\text{tot}} = \sum_{\text{switches}} G_i (v_{r,i(\text{rated})})^2 \quad (24)$$

where G_i is the conductance of switch i and $v_{r,i(\text{rated})}$ is the rated voltage of switch i. As in the capacitor optimization, $v_{r,i(\text{rated})}$ is the voltage the device can support, not necessarily the voltage it blocks in normal operation. Naturally, the rated voltage must be larger than the nominal blocking voltage.

A Lagrange optimization function $\mathcal{L}$ is formed to minimize the FSL output impedance while satisfying the constraint in (24)

$$\mathcal{L} = \sum_i \frac{(a_{r,i})^2}{G_i} + \lambda \left(\sum_{\text{switches}} G_i (v_{r,i(\text{rated})})^2 - A_{\text{tot}} \right). \quad (25)$$

The first term corresponds to the FSL output impedance (the factor of two in (14) does not affect the optimization) and the second term corresponds to the constraint in (24). The minimization is performed by taking the partial derivative of (25) with respect to G_i and setting it to zero

$$\frac{\partial \mathcal{L}}{\partial G_i} = -\frac{(a_{r,i})^2}{G_i^2} + \lambda (v_{r,i(\text{rated})})^2 = 0. \quad (26)$$

Again, differentiating with respect to λ yields the constraint in (24).

Equation (26) yields a proportionality between G_i and the ratio between the switch's charge multiplier coefficient and its voltage rating. This proportionality, when combined with the G-V^2 constraint in (24), yields an expression for the optimal conductance of each switch

$$G_i^* = \frac{1}{R_i^*} = \left|\frac{a_{r,i}}{v_{r,i(\text{rated})}}\right| \frac{A_{\text{tot}}}{\sum_k |a_{r,k} v_{r,k(\text{rated})}|}. \tag{27}$$

Comparing the optimal conductance G_i to the optimal capacitance in (19) makes it evident that the two optimizations are analogous.

The optimal FSL output impedance is obtained by substituting (27) into (14)

$$R_{\text{FSL}}^* = \frac{2}{A_{\text{tot}}} \left(\sum_i |a_{r,i} v_{r,i(\text{rated})}|\right)^2. \tag{28}$$

Similar to the optimal SSL impedance, the optimal FSL output impedance is related to the square of the sum of the V-A products. This simple form of the optimal output impedance allows the comparison of various SC converter topologies. Several SC converter topologies are compared in Section IV.

Many SC converters use switches with a single voltage rating. For instance, many IC-based converters only use the native NMOS transistors of the process since these transistors perform the best. In addition, topologies such as the ladder converter utilize switches that must all block the same voltage. The switch-cost constraint discussed in the previous section simplifies into a constraint on total switch conductance G_{tot}. The optimal conductance of each switch simplifies to

$$G_i^* = \frac{|a_{r,i}|}{\sum_k |a_{r,k}|} G_{\text{tot}} \tag{29}$$

likewise, when all switches are rated for an identical voltage, the optimal FSL output impedance simplifies to

$$R_{\text{FSL}}^* = \frac{2}{G_{\text{tot}}} \left(\sum_i |a_{r,i}|\right)^2. \tag{30}$$

The performance of a converter is related to the square of the sum of the charge multiplier coefficients. Topologies with a small sum of these coefficients perform better for a given switch conductance than a topology with a large sum of coefficients. In integrated applications or other applications where single-voltage switches must be used, this optimization can be used. A comparison of SC converters based on single-voltage devices is performed in Section IV.

IV. Comparison of SC Converter Topologies

A number of SC converter topologies exist in the literature [1], [3]–[5], [10], [11]but the merits of each have never been compared in a methodical way. The optimizations in Sections III-A and III-B can be used to provide a performance comparison among different common SC converter topologies. Fig. 5 shows five converter topologies discussed in the literature.

The first comparison uses the cost metrics in Section III and assumes that devices of every voltage rating are available.

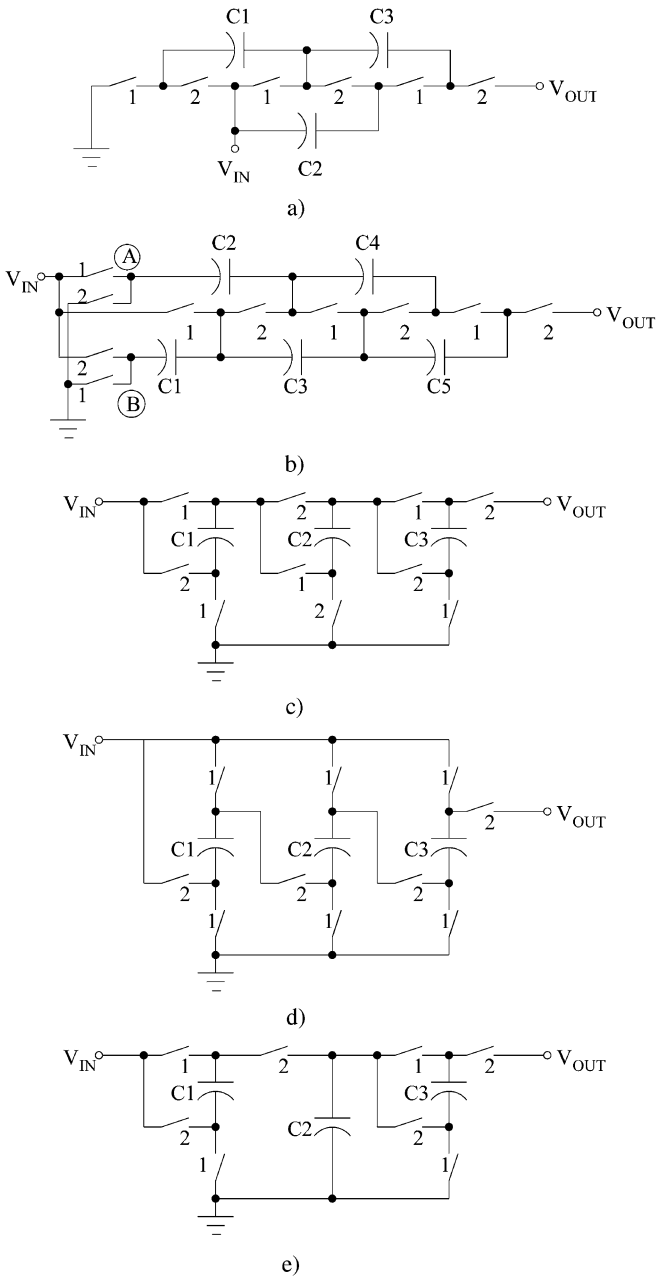

Fig. 5. Five step-up SC converter topologies. (a) Ladder. (b) Cockcroft–Walton Multiplier. (c) Fibonacci. (d) Series-Parallel. (e) Doubler.

Step-up versions of the topologies are considered, as shown in Fig. 5, although step-down versions would yield identical results. The commonly-used Dickson Charge Pump is a simple transformation of the Cockcroft–Walton multiplier, constructed by connecting the negative plate of each capacitor to either node A or B. The capacitors in the Dickson charge pump form two star networks while the capacitors in the Cockcroft–Walton multiplier form two linear strings. The optimal output impedance for all topologies in both asymptotic limits is evaluated for a range of conversion ratios (represented by n).

When evaluating the FSL output impedance, the converters are evaluated on the ratio $(V_{\text{OUT}}^2/R_{\text{FSL}}A_{\text{tot}})$ (the ratio between the G-V^2 product of the converter and the switch G-V^2 product

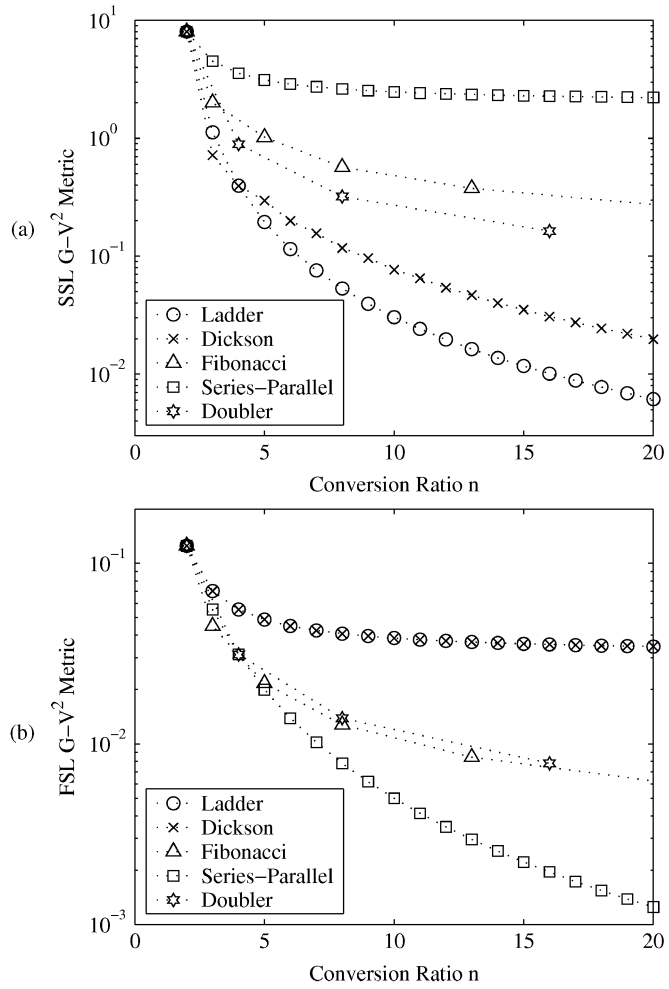

Fig. 6. (a) SSL and (b) FSL performance metrics with optimal-voltage devices.

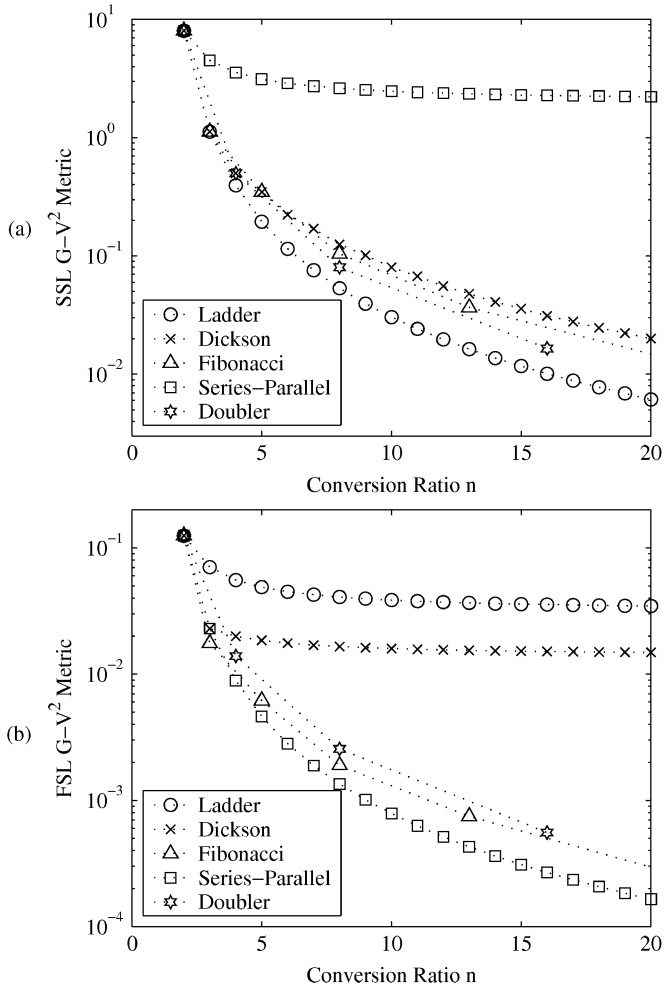

Fig. 7. (a) SSL and (b) FSL performance metrics with single-voltage devices.

summed over all switches). For a given cost constraint and conversion ratio, the converter with the highest metric is the one with the lowest FSL output impedance. Likewise, when the SSL output impedance is considered, the converters are evaluated on the ratio $V_{\rm OUT}^2/(R_{\rm FSL}/E_{\rm tot}f_{\rm sw})$, where a larger metric corresponds to a smaller SSL impedance.

After performing the optimization and comparison, the five topologies are compared in Fig. 6. At a conversion ratio of two, all topologies perform identically. Upon further inspection, for $n = 2$ only, these five topologies are actually identical. Converters that do well in the SSL comparison, such as the series-parallel topology, do poorly in the FSL comparison. Conversely, topologies such as the Cockcroft–Walton multiplier and the Ladder topology that perform well in the FSL comparison typically perform poorly in the SSL comparison. Some converters use capacitors efficiently and others use switches efficiently, but none of these converters are superior in both asymptotes. For converters designed using a capacitor-limited process, a series-parallel topology would work best, while switch-limited designs should use a topology such as the Cockcroft–Walton multiplier or ladder topology.

The exponential converters (where the conversion ratio is exponentially related to the number of capacitors), such as the Fibonacci and Doubler topologies, exhibit mediocre performance in both the SSL and FSL comparisons. However, since the switches and capacitors used in their implementations support a range of different voltages and most of the switches are not ground-referenced, practical implementation would be difficult if not impossible.

The second comparison performed assumes that all devices must be of the same voltage rating. In integrated applications using standard CMOS processes, the switches and capacitors are usually all rated for the same voltage. The process is chosen such that this voltage rating corresponds to the maximum voltage seen on any device. However, the switches and capacitors can be rated differently from each other, ie. if the highest-voltage switch is rated for 1 V, a 1 V process would be used, even if some capacitors support a higher voltage.

The comparative results using identically-rated switches and transistors are shown in Fig. 7. The series-parallel topology is still optimal in the SSL comparison, as all capacitors in that topology also support the same voltage. Likewise, the ladder topology is optimal in the FSL comparison, as all switches in that topology support the same voltage. However, the exponential converters are now relatively poor in both comparisons because they involve a wide range of device stresses, which is impractical in implementation. These comparisons can be used to

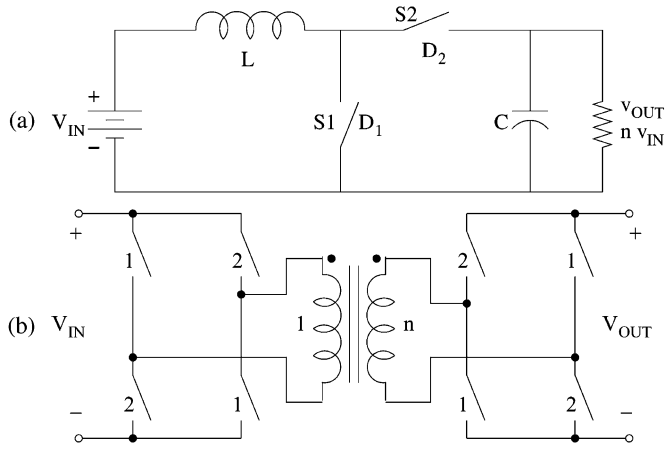

Fig. 8. (a) Standard boost converter. (b) Transformer-bridge converter.

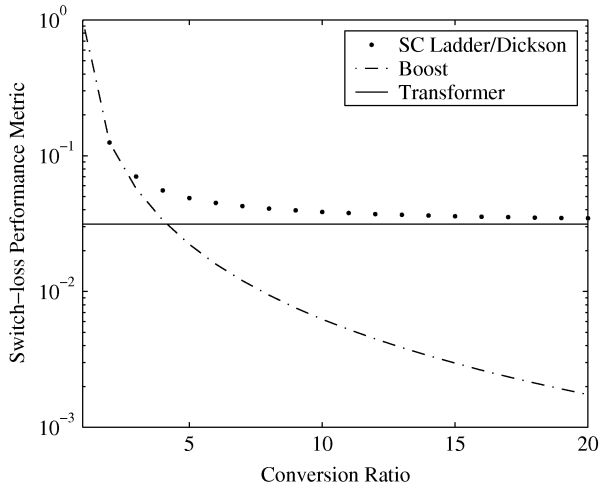

Fig. 9. Performance metric comparison.

select the best topology for any given application. Reference [8] includes more computational details for these converters.

V. Comparison With Conventional Designs

Switched-capacitor converters have several advantages over conventional inductor-based dc–dc converters. With a switched-capacitor converter, conduction and switching losses are not additional losses, but are already incorporated in the output impedance based losses calculated in Sections II–A and Sections II-B. The only losses that are not included in the output impedance are the gate drive losses, losses associated with parasitic capacitances and control power. Short-circuit (shoot-through) power can be eliminated by the use of sufficiently non-overlapping clocks. Stray capacitances from dynamic nodes must be minimized and their losses incorporated into the efficiency of the converter if the strays are not eliminated. These losses are further considered in [8].

A SC converter and a conventional dc–dc converter can be compared directly when conduction loss is considered. The silicon area (for the switches and control functions) is the dominant cost in many dc–dc converters. A converter with a significantly-lower switch conductance loss may have a cost advantage over a converter with a higher switch loss. For the SC converter, the conduction loss is equal to the loss corresponding to the FSL output impedance. The switch-related loss of an inductor-based converter is made up of conduction losses, due to switch on-state resistance, and switching losses during the switch state transitions. Only the conduction loss will be considered here, using the FSL performance metric $V_{\rm OUT}^2/(R_{\rm FSL}/A_{\rm tot})$ developed in Section IV.

A ladder-type step-up converter [such as the one in Fig. 5(a)] is considered, as it uses switches most efficiently in the FSL. Two magnetic-based converters are compared, the boost converter and transformer-bridge converter, both shown in Fig. 8. Total switch G-V^2 product is held constant for all converters, and the SC converter is assumed to operate in the FSL. Finally, all switches are sized optimally based on the optimization methods presented in this paper. All converters are designed and optimized for a given conversion ratio n, and without loss of generality, an input voltage of 1 V is assumed.

The step-up ladder-type SC converter is considered first. All switches in the ladder topology must be rated for 1 V. The lowest two switches in the ladder structure have an a_r component of $(n-1)$ while the other $2(n-1)$ switches simply have an a_r component of 1. Thus, the sum of the a_r components is

$$\sum_i |a_{r,i}| = 2(n-1) + 2(n-1) = 4(n-1). \tag{31}$$

The optimal FSL output impedance of this converter (constrained such that $\sum_{\rm switches} G_i V_i^2 = A_{\rm tot} = 1$) is thus

$$R_{\rm out} = 2\left(\sum_i |a_{r,i} v_{r,i({\rm rated})}|\right)^2 = 32(n-1)^2. \tag{32}$$

Computing the ratio of this output resistance to the square of the output voltage yields the performance metric of the ladder circuit, $(n^2)/(32(n-1)^2)$. This metric is also plotted in Fig. 9.

The boost converter in Fig. 8(a) is operated at duty cycle $D = 1/n$ to achieve a step-up ratio of n. The duty cycle of switch S1 is $D_1 = D = 1/n$ and the duty cycle of switch S2 is $D_2 = 1-D = (n-1)/n$. The conduction loss in this circuit is directly computed as

$$P_{\rm cond} = \left(\frac{D}{G_1} + \frac{1-D}{G_2}\right) I_{\rm in}^2 = R_{\rm out} I_{\rm out}^2. \tag{33}$$

The equivalent loss impedance $R_{\rm out}$ can be directly compared to the output impedance of the SC converter. Optimizing the ratio of the two switch conductances for a given duty cycle, the following constraint can be derived

$$\left(\frac{G_1}{G_2}\right)^2 = \frac{D}{1-D}. \tag{34}$$

Since the total G-V^2 product of the switches is again constrained at one and each switch in the boost converter must be rated for the output voltage of n, the total conductance is restricted to $G_{\rm tot} = 1/n^2$. From this constraint, the equivalent

loss impedance can be determined (note that $D = 1/n$ to achieve the correct conversion ratio):

$$R_{\text{out}} = n^4\left(\frac{D}{G_1} + \frac{1-D}{G_2}\right) = n^4\left(1 + 2\sqrt{\frac{n-1}{n^2}}\right). \tag{35}$$

Computing the ratio of the square of the output voltage to this optimal output resistance yields the performance metric of the boost circuit, $1/(n^2(1 + 2\sqrt{(n-1)/(n^2)}))$. This metric is plotted in Fig. 9.

Finally, the transformer-based direct converter in Fig. 8(b) is considered. The transformer is assumed to be ideal and to have an up-conversion ratio of n. The output switches are all identical and must be rated for the output voltage of n V. The on-current of these switches is equal to the output current I_{out}. Likewise, the input switches must be rated for 1 V and conduct a current of nI_{out}. To constrain the total G-V^2 product equal to one, the output switches must have conductances of $1/8n^2$ and the input switches must have conductances of $1/8$. The conduction loss can then be calculated as

$$P_{\text{cond}} = 2(8n^2)I_{\text{out}}^2 + 2(8)(nI_{\text{out}})^2 = 32n^2I_{\text{out}}^2. \tag{36}$$

The resulting performance metric for this converter is then constant at $1/32$ for any conversion ratio. This makes intuitive sense as only the transformer turns ratio is changed to achieve different conversion ratios.

The conduction losses of the three converters, represented by theperformance metric $V_{\text{OUT}}^2/(R_{\text{FSL}}/A_{\text{tot}})$ developed in Section IV, are compared in Fig. 9. The SC and boost converters' performance metrics decrease as the conversion ratio increases, but the SC converter approaches an asymptotic limit at $1/32$ (the same as the transformer-based converter), but the boost converter's performance continues to decrease.

At large conversion ratios, the step-up ladder-type SC converter is significantly superior to the boost converter as the switches in the ladder topology block only the input voltage and most switches carry less than the input current. However, the boost converter's switches carry the full input current and block the full output voltage. Even though the SC converter has many more switches, the low working V-A product of these switches yields a lower conduction loss than that of the boost converter, with its much higher working V-A product switches.

In an application where switches are the limiting factor in performance or cost, switched-capacitor converters are evidently advantageous over conventional magnetics-based dc–dc converters at high or moderate conversion ratios.

VI. Verification by Simulation

As this analysis method is based on idealized devices, circuit-level simulation, through SPICE or spectre is appropriate for verification of this analysis. Ideal capacitor and voltage-controlled resistances are used in the simulation. Parasitics, while an important consideration in real-world implementations, are not considered in this paper, and are not considered in the verification simulation.

Five step-up switched-capacitor converters have been simulated over a range of switching frequencies. By varying the switching frequency, both the SSL and FSL output impedances can be determined and compared with those from the mathematical analysis. The converters simulated are the 1:4 (i.e., 1 V input to 4 V output) ladder converter, 1:4 Cockcroft-Walton multiplier, 1:4 doubler, 1:5 Fibonacci converter, and a 1:4 series-parallel converter, all shown in Fig. 5. The capacitors and switches in all converters are optimized using the methods in this paper using a switch GV^2 product of 1 VA and a total capacitor energy of 1 μJ. The output impedance was determined by measuring the current transfer between the input and output voltage sources in a transient simulation.

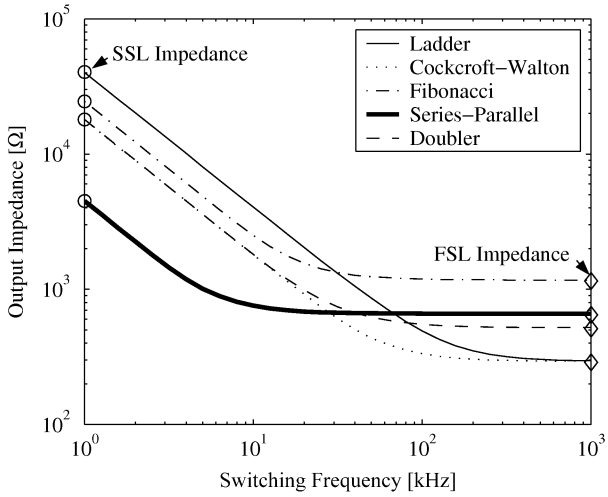

Fig. 10. Simulated output impedance versus switching frequency.

TABLE I
SSL and FSL VA-Products and Impedances for Five Converters (R_{SSL} at 1 kHz)

	$\sum\lvert a_c v_c\rvert$	$\sum\lvert a_r v_r\rvert$	R_{SSL}	R_{FSL}
1:4 Ladder	9	12	40.5 kΩ	288 Ω
1:4 Cockcroft-Walton	6	12	18 kΩ	288 Ω
1:5 Fibonacci	7	24	24.5 kΩ	1152 Ω
1:4 Series-Parallel	3	18	4.5 kΩ	648 Ω
1:4 Doubler	6	16	18 kΩ	512 Ω

The charge-multiplier-voltage products and output impedances of the five converters found via the methods in Section II are shown in Table I. These calculations and detailed converter analysis are given in [8]. Fig. 10 shows the simulated impedance of the converters between 100 Hz and 1 MHz. The symbols in the plots indicate the calculated FSL and SSL impedances, showing a match between the theoretical and simulated values.

Five very different switched-capacitor converters were simulated for a range of frequencies encompassing both the SSL asymptote and the FSL asymptote. The simulation results verify that the analysis methods developed in Section II determine the correct output impedance in both asymptotes for all five converters. This simulation verifies that the methods developed in this paper accurately predict the performance of any two-phase SC converter.

VII. Experimental Verification

An ultra-low-power switched-capacitor power conversion integrated circuit (IC) has been fabricated and tested with design

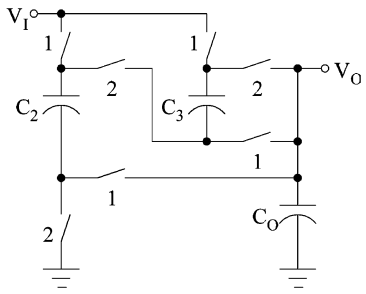

Fig. 11. 3:2 Series-parallel converter topology.

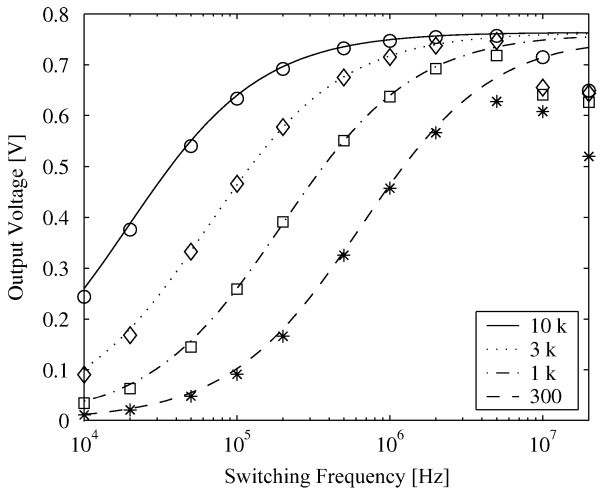

Fig. 12. Measured and calculated output voltage versus load and switching frequency.

guidance from the analysis method developed here. The design and experimental results of this IC are presented in [12]. The results from the 3:2 converter (1.2 V to 0.8 V) is presented here as an example circuit further verifying the calculations for a single converter topology.

A schematic of this converter is shown in Fig. 11. It is similar to the series-parallel circuit in that the capacitors are placed in series in one phase and parallel in the other phase. Capacitors C_1 and C_2 both have a charge multiplier of 1/3 in this circuit and capacitor C_0 is ignored as it is in parallel with the output. Each of the seven switches also has a charge multiplier of 1/3. In the IC, each capacitor has a value of 1.15 nF and each switch has a resistance of 4.75 Ω. Thus, the predicted output impedances in both limits, calculated using (9) and (14), are

$$R_{\mathrm{SSL}} = \frac{2(1/3)^2/1.15nF}{f_{\mathrm{sw}}} = \frac{193\ M\Omega}{f_{\mathrm{sw}}} \tag{37}$$

$$R_{\mathrm{FSL}} = 2 \cdot 7(4.75(1/3)^2) = 7.39\ \Omega. \tag{38}$$

Fig. 12 shows the output of the 3–2 converter for various switching frequencies and resistive loads. The plotted curves indicate the ideal output voltage calculated by considering a resistor divider between the load resistance and converter output impedance. The data indicate that the model accurately predicts the converter performance for low frequencies. At high switching frequencies, parasitic losses hurt the converter's performance. The most influential parasitics, in this case the capacitor bottom-plate capacitance and drain-source capacitance, need to be carefully considered in any realization of switched-capacitor converters.

VIII. Conclusion

An analysis method has been presented to determine the performance of any switched-capacitor power converter using easily-determined charge multiplier vectors. The capacitors and semiconductor switches of the converter were optimized to minimize output impedance for several conditions and constraints. Five separate converter topologies were considered for their effectiveness in utilizing capacitors and switches. This comparison allows the use of an optimal topology suited to its application and implementation technology. Significantly, the performance (based on conduction loss) of a ladder-type converter was found to be superior to that of a conventional boost converter for medium to high conversion ratios.

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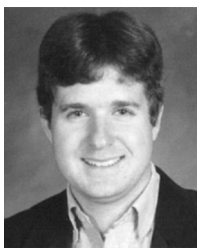
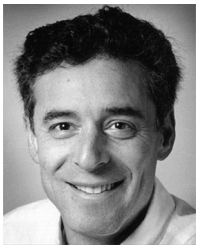


Michael D. Seeman (S'03) received the B.S. degree in electrical engineering and the B.S. degree in physics from the Massachusetts Institute of Technology, Cambridge, in 2004 and the M.S. degree in electrical engineering from the University of California, Berkeley, in 2006 where he is currently pursuing the Ph.D. degree. His work centers on the implementation of advanced integrated switched-capacitor converters.

His research interests also include low-power analog integrated circuits and energy conversion circuits for scavenged-energy wireless sensor nodes.

Mr. Seeman is a member of Eta Kappa Nu and Phi Beta Kappa.



Seth R. Sanders (M'88) received the S.B. degrees in electrical engineering and physics and the S.M. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1981, 1985, and 1989, respectively.

He was a Design Engineer with Honeywell Test Instruments Division, Denver, CO. Since 1989, he has been on the faculty of the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, where he is presently a Professor. During the 1992 to 1993 academic year, he was on industrial leave with National Semiconductor, Santa Clara, CA. His research interests are in high frequency power conversion circuits and components, in design and control of electric machine systems, and in nonlinear circuit and system theory as related to the power electronics field. He is presently actively supervising research projects in the areas of renewable energy, novel electric machine design, and digital pulse-width modulation strategies and associated IC designs for power conversion applications.

Dr. Sanders received the NSF Young Investigator Award in 1993 and multiple Best Paper Awards from the IEEE Power Electronics and IEEE Industry Applications Societies. He has served as Chair of the IEEE Technical Committee on Computers in Power Electronics, and as a Member-At-Large of the IEEE PELS Adcom.