

Active Clamp Circuits for Switchmode Regulators Supplying Microprocessor Loads *

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Abstract

Present day microprocessors such as the Intel Pentium Pro require over 10amps of supply current at voltages in the range of 2-3.3volts. The load demand can exhibit abrupt changes from light load (<0.5amps) to full load in a matter of few hundred nanoseconds. Future processor generations are projected to require greater current (up to 60amps) at supply voltages as low as 1volt. Furthermore, these future processors are projected to impose load steps with $\frac{di}{dt}$ on the order of 5amp/nS when the processor switches between inactive and active modes, or vice-versa. In this paper, we discuss some of the ramifications for the design of the power supply required to supply these microprocessor loads. We focus on the use of a paralleled active circuit which can be thought of as an active clamp which is designed to support the load during transients. Breadboards of these circuits have been built and tested. A prototype IC design is currently under test.

1 Introduction

Present day microprocessors such as the Intel Pentium Pro require over 10amps of supply current at voltages in the range of 2-3.3volts. The load demand can exhibit abrupt changes from light load (<0.5amps) to full load in a matter of a few hundred nanoseconds. Future processor generations are

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The paper is organized as follows. Section 2 outlines the application. Section 3 outlines the design of an active clamp device that may be used in parallel with a switchmode converter to alleviate the demand on the passive filter components. Breadboards of these circuits have been built and tested, and test results are reported in Section 4. Additional discussion is given in Section 5.

2 Application

Figure 1 shows the interconnection of the active clamp circuit with a standard dc-dc converter. The active clamp circuit is designed to work in parallel with the output of a conventional switching regulator. Its function is to do nothing, i.e. appear as a high impedance terminal, during normal steady state switching regulator operation. In the event of a load transient that would drive the output of the switching regulator beyond a specified tolerance band, the clamp activates to hold the output voltage within this

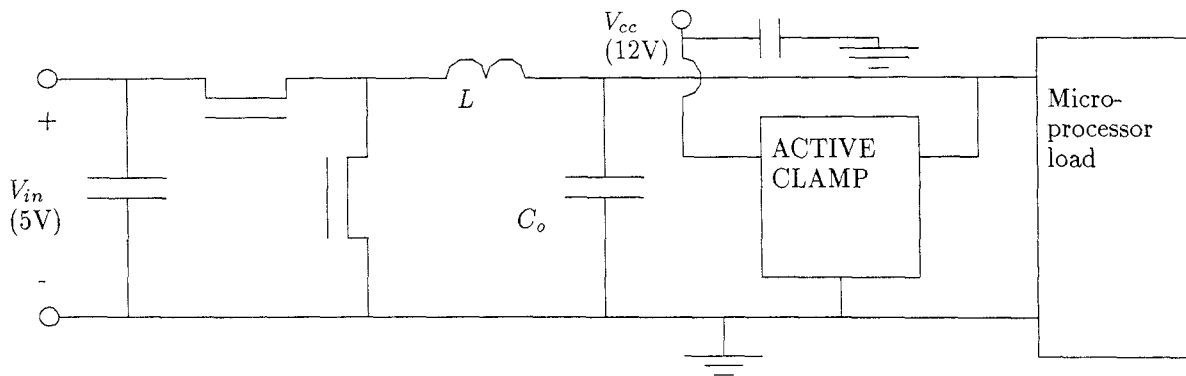


Figure 1: Interconnection of Active Clamp Circuit with Switchmode Regulator

specified band. As such, the active clamp must be specified to handle the full load current, but only for short intervals on the order of tens of microseconds. Hence, the active clamp circuit must be designed for high peak current and high peak power capability, but need not handle significant continuous steady state power. In order to provide a useful function, the device must be able to sink or source rated current within a few hundred nanoseconds.

In order to understand the potential benefit in an application, we shall focus on the Pentium Pro application requiring about 10 amps from a switching regulator operating at about 300Khz since this is typical of the current state-of-the-art. For the 5V to 3.3V buck application, a filter inductor of $L = 1.5\mu\text{H}$ will yield a peak-peak current ripple of about 2.5amp. a typical design. In order to achieve a peak-peak output ripple of 50mV, a capacitor of only about 20uF is needed if ESR is neglected. With a 20uF ceramic chip capacitor with ESR typically less than 10mΩ, the ESR contribution to the output ripple voltage will only be on the order of 20mV peak-peak. It is likely that some designers would select a larger capacitor when considering ripple, in order to further reduce the voltage ripple and to avoid the possibility of a capacitor reliability problem because of the large ripple current. Nevertheless, designs in the range from 20uF to 50uF are feasible with ceramic chip capacitors, or with solid tantalum chip capacitors requiring total capacitance approaching 200uF, due to higher ESR.

When considering transient response to step load changes, the requirement on the output capacitor may be far more stringent. We note that a Maxim test board rated at 15amps is designed with 2,000uF of electrolytic capacitance at the output [1]. A very simple analysis based on an averaged model (Fig. 2)

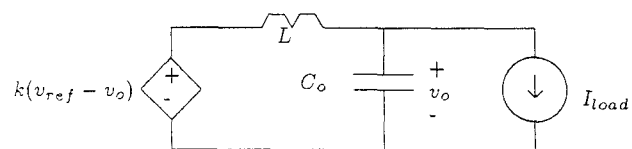


Figure 2: Simple Average Circuit Model for Voltage-Mode Controlled Buck Converter

of a voltage feedback scheme predicts a step response of the form

$$v(t) = -\frac{I_o}{\omega_c C_o} \sin(\omega_c t) \quad (1)$$

to a load current step of magnitude I_o amps, where C_o is the output capacitance, and ω_c is the cross-over frequency of the feedback loop. Assumptions here are that all forms of damping including output capacitor ESR are negligible, current feedback is not used, the input impedance is stiff, and that the duty cycle control does not saturate. The latter is the most significantly unrealistic assumption, as will be discussed below. We use the approximation (1) to estimate the first peak of the voltage in the transient response, for a scenario where duty cycle saturation does not play a role. With an aggressive cross-over frequency of 100Khz, $C_o=20\mu\text{F}$, and a load step of 10amps, the peak voltage transient would be about 800mV. With a $\pm 5\%$ tolerance band about say 3.3volts, this peak voltage is unacceptable since the tolerance band amounts to only $\pm 165\text{mV}$. With the same conditions, except for an output capacitance $C_o=200\mu\text{F}$, we would see a voltage peak of 80mV with this simple model. For a design with $C_o=2,000\mu\text{F}$, and other conditions the same, we would expect to see only 8mV of voltage disturbance.

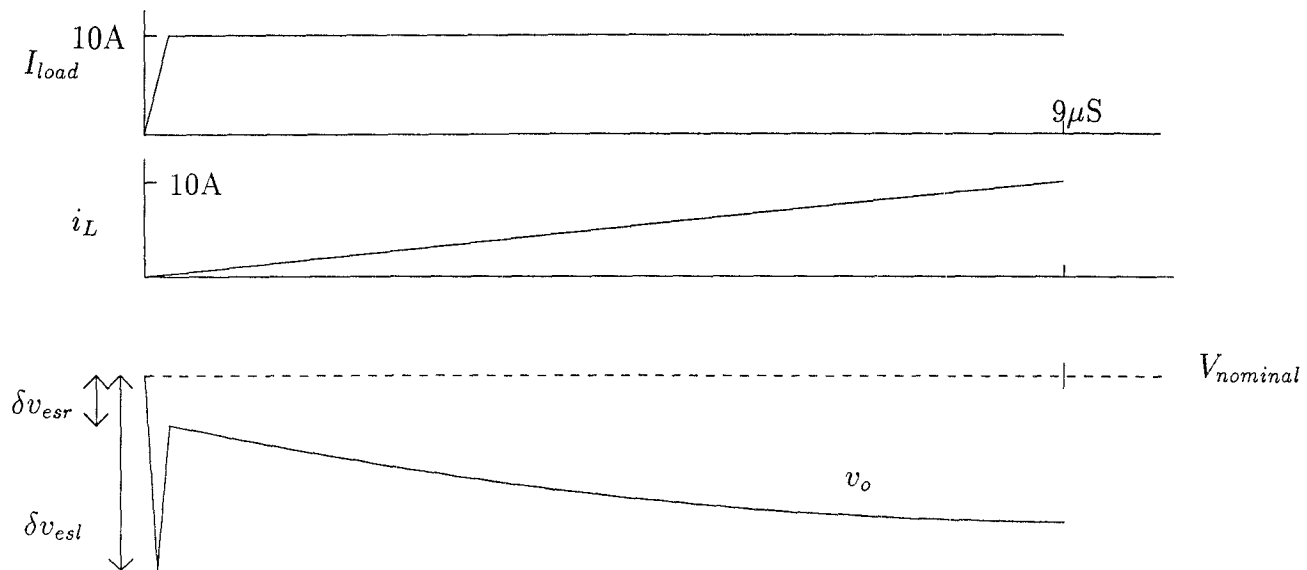


Figure 3: Circuit Waveforms under Duty Cycle Saturation

The above analysis is unrealistic due to the fact that the duty ratio control will nearly always saturate (i.e. reach its maximum or minimum) under a large load transient. A simple analysis incorporating saturation is depicted in Figure 3, and described here. Assume the converter output is initially at 3.3V, supplying zero load current. The load then steps to 10amps. The converter reacts by applying full duty cycle. If the input is stiff at 5V, the voltage across the inductor is about 1.7V if the output does not sag very much. With 1.7V on the inductor, it requires about 9μs for the current in the 1.5μH inductor to ramp up to 10amps. At the end of this 9μs transient, the output voltage can begin its recovery, hence this is the approximate time point where the voltage bottoms out. The total charge removed from the output capacitor, assuming a ramp current waveform, is 45μC. This analysis is independent of the output capacitor value and assumes a stiff (i.e. large input capacitance) input voltage and also assumes that 100% duty cycle can be applied. Now with a 20μF output capacitance, the voltage transient will be about 2.25V peak. With 200μF or 2,000μF, the transient voltage would peak at 225mV or 22.5mV, respectively. Since these estimates are optimistic (stiff input voltage and 100% duty cycle assumptions), a design choice of 2,000μF does indeed make some sense.

The advantage of the active clamp is that the output capacitor will only need to be designed to handle

the ripple current, and not to contain the output voltage during load transients. As such, for the application discussed here, ceramic chip capacitors as small as 20μF may be feasible when incorporating an active clamp circuit, whereas output capacitances of at least 400μF would otherwise be needed. In reference [2], a slightly different application is analyzed. In this application, the load is specified at 20amps maximum at 3.3volts, but the tolerance is considerably tighter at $\pm 2\%$. The output capacitor bank required to support a full step load transient in this application includes 20,000μF of bulk hold-up capacitance in conjunction with a network of paralleled high frequency (lower inductance, lower ESR) tantalum and ceramic capacitors. In this scenario and that involving the specification of future microprocessors, the active clamp will yield far greater benefits.

Note that during the activation of the clamp circuit following a load increase, charge is supplied from a bypass capacitor on the V_{cc} supply. This supply level would likely be set at a higher voltage (eg. 12V) than the 5V supply, which would likely be used to supply the main dc-dc converter. As such, the total capacitance required to bypass the V_{cc} supply will be much smaller than would be required to hold up the output voltage directly at the output pin, in the absence of the clamp circuit. This is because the V_{cc} supply rail can be allowed to sag, perhaps by a few volts during a transient.

3 Design

As previously discussed, the active clamp circuit is actually built from two independent half-circuits, the lower clamp and the upper clamp. We begin by discussing the overall scheme of one of the half-circuits. A functional schematic and control loop diagram for the upper clamp function is shown in Figure 4. This is the half-circuit that is activated whenever the output voltage goes above the high reference V_h .

The current sensing feedback around the op-amp constitutes a minor feedback loop, forcing the clamp output transistor current to be approximately

$$i_{out} = -(V_o - V_h)R_f / (R_i R_s) \quad (2)$$

at low frequency. Dynamically, this minor loop has the response of the op-amp connected in a standard differential gain of 25 connection. For an op-amp such as the LM6171 [3], the corner frequency for this minor loop occurs at around 3Mhz. The outer loop determines the overall speed of response. With an output capacitance of 20uF, the outer loop would exhibit a corner frequency at about 4MHz. As such, one would expect to see a second order, i.e. ringing, transient response, characterized by about a 45 degree phase margin. With larger output capacitances, the outer loop response will be slowed down further, yielding larger phase margins and more damped transient responses. However, this will in no way impede the function of the clamp circuit since the minor current loop responds equally fast with any output capacitance.

Equation (2) is also of interest in determining the dc load regulation characteristic of the active clamp. This is governed by an effective impedance of 2m Ω for our prototype design, which at 10amps yields a voltage regulation of 20mV. Note that it is essential to include separate sensing and forcing pins in an IC package since the IC package and board traces leading to the output capacitor may very well impose more than 2mohm of resistive and/or inductive impedance.

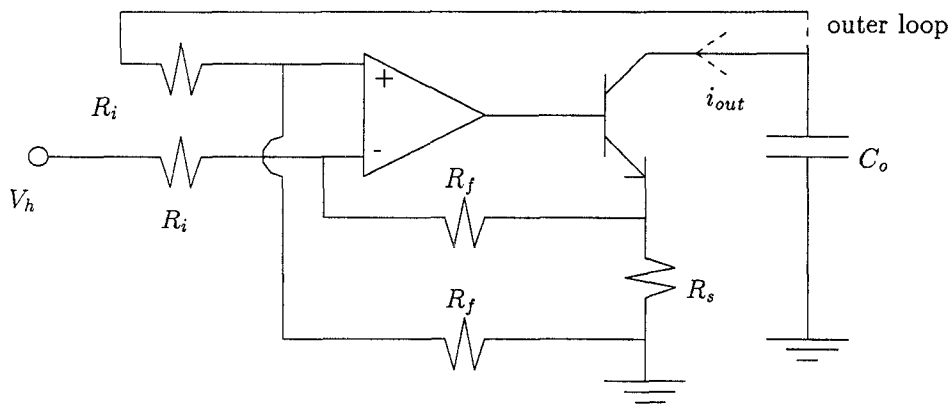
Figure 5 shows a schematic for the complete active-clamp circuit. This is essentially the circuit of Figure 4, but with compound transistor connections used to realize the large output stages. A candidate process for fabrication of the circuit is the National Semiconductor VIP-3 process [4] since it is a state-of-the-art high speed bipolar process, in terms of performance, minimum device feature size, and availability of high performance op-amp cells. A test board was built using IC kit parts in the VIP-3 process.

Note that there is not very much characterization data available on the devices for the type of operation that will be of interest, namely very high current density operation either saturated or unsaturated. The reason for operating with very high current densities is to conserve die area. Some data on the kit parts was obtained in curve tracer evaluations, and was used to guide the design. One of the consequences of operation at very high current densities, on the order of 10-20 times the nominal design current density, is a degradation in device speed. This will be discussed briefly in the following section.

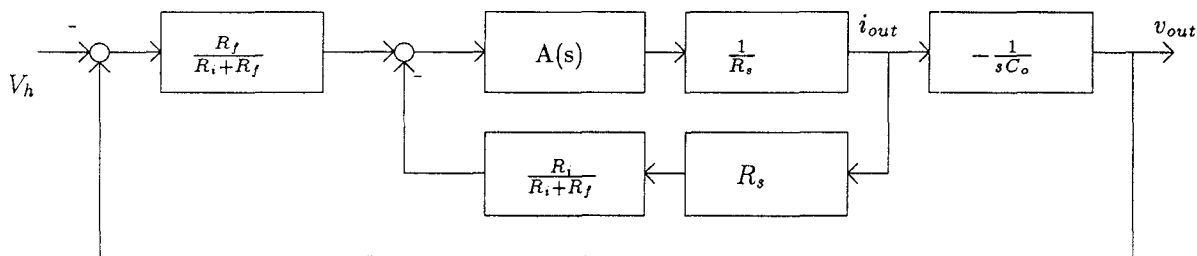
An overall strategy for the design of each of the two large compound transistor connections was to design for a minimum current gain of five in each stage, and to use four stages to avoid overloading the op-amp output. A significant base-emitter "leak" resistor was designed into each of the stages of the compound transistor, in order to provide a turn-off mechanism for each stage. Typical sizing of these base-emitter resistors was made to allow for a leak current on the order of one-fifth of the base current.

4 Test Results

A prototype of the active clamp circuit scaled for a 2.5amp load has been built using discrete op-amps [3] and IC kit parts all built in the high speed complementary bipolar VIP-3 process [4]. Although designed for 2.5amps, the breadboard prototype was tested at 3 amps to demonstrate functionality. The prototype active clamp circuit test circuit was interconnected with a dc-dc converter, operating at a switching frequency of 300KHz, as shown in Figure 1. For this interconnection, an oscilloscope photo of the response to a step load change from 0 to 3 amps is shown in Figure 6(a). Note that the dc-dc converter is running at about its nominal output of 3.3V with an output ripple of about 50mV peak-peak and approximate frequency of 300KHz. A time-scale blow-up of this transient is shown in Figure 6(b), where the scale is 200nS/division. In this figure, the voltage spike due to the parasitic inductance (ESL) associated with the output capacitance and layout is evident. As is evident from the waveform for the op-amp output that drives the compound pull-up PNP device, the recovery of the clamp circuit occurs in about 300 nS. Note that the recovery is considerably slower than would be computed for the nominal rated base transit time τ_F and rated transition frequency $f_t \approx 3\text{GHz}$ for the process. This is likely due to high level injection effects,



(a) Functional Schematic



(b) Loop Dynamics Model

Figure 4: (a) Functional Schematic of Clamp and (b) Corresponding Loop Dynamics Model

especially the Kirk effect which effectively broadens the base region of a bipolar device [5, 6]. In order to conserve die area, the output devices are driven at emitter current densities as high as 10-20 times the level at which the onset of Kirk effect occurs.

Waveforms complementary to those of Figures 6(a,b) are shown in Figure 6(c,d). For these latter two photos, the dc-dc converter is supporting a 3 amp steady state load, which is interrupted. The upper clamp function is seen to behave analogously to the lower clamp function.

5 Comments

The development described above is evidently a potential route for easing the constraints imposed on power supply systems by microprocessor loads. One potential complication is in the need for two reference levels that are application dependent, and that must be coordinated with the internal reference voltage of the main dc-dc converter. One possible coordination scheme that has proven effective is to develop the two reference levels for the clamp circuit by real time low-

pass filtering of the dc-dc converter output. This is illustrated in Figure 7. With this approach, the reference levels are directly tied to the dc-dc converter output voltage level. Hence, the tolerance bands may be tightened substantially, limited mainly by the output ripple voltage.

Another approach for the design would be to implement the clamping function as part of an active filtering scheme, as reported in various publications (see for example [7] and references therein). This approach was not taken in the present work to allow for maximum efficiency. Nevertheless, such an approach may be warranted in higher current, lower voltage applications where the basic ripple filtering function may become more difficult.

The authors would like to acknowledge the similar effort by engineers at Maxim Integrated Products, as reported in the recent article [8].

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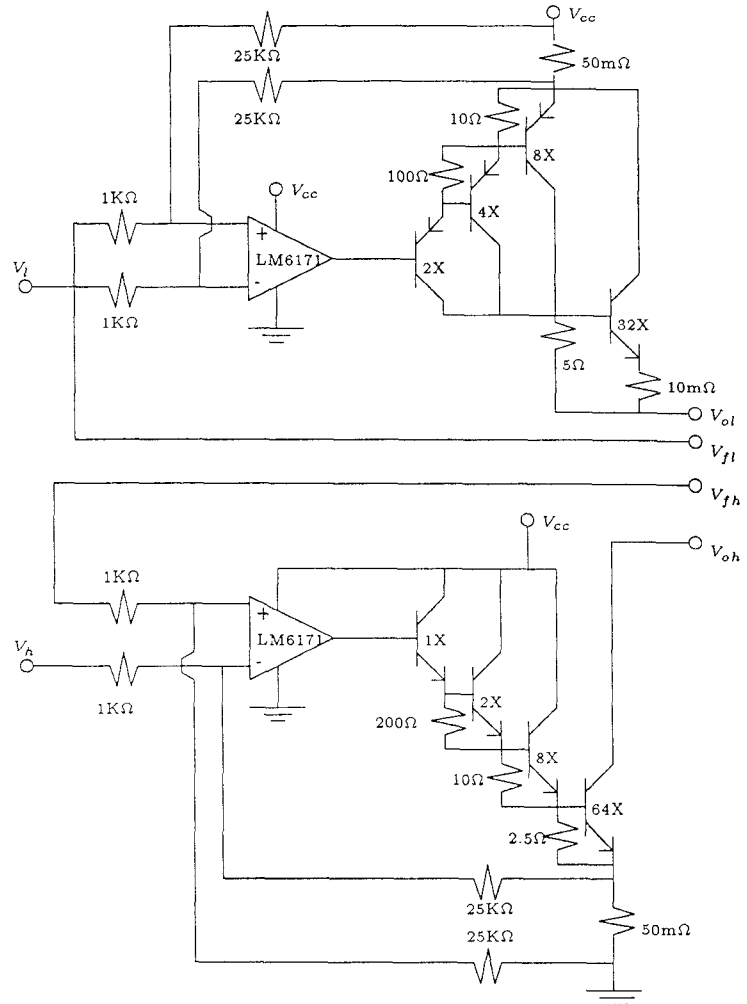


Figure 5: Schematic of Active Clamp Circuit. Device sizes are relative to a $960 \mu\text{m}^2$ emitter area cell.

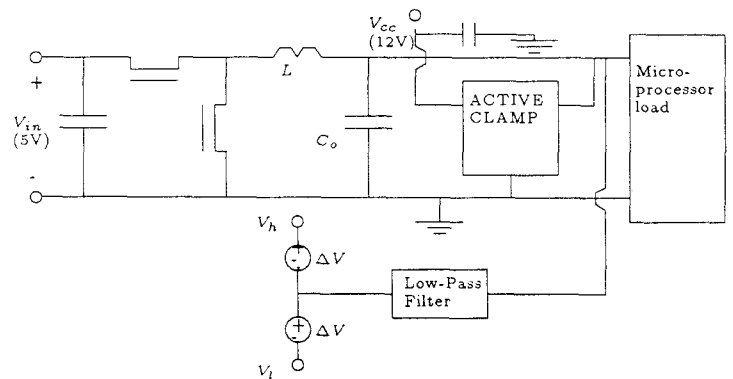
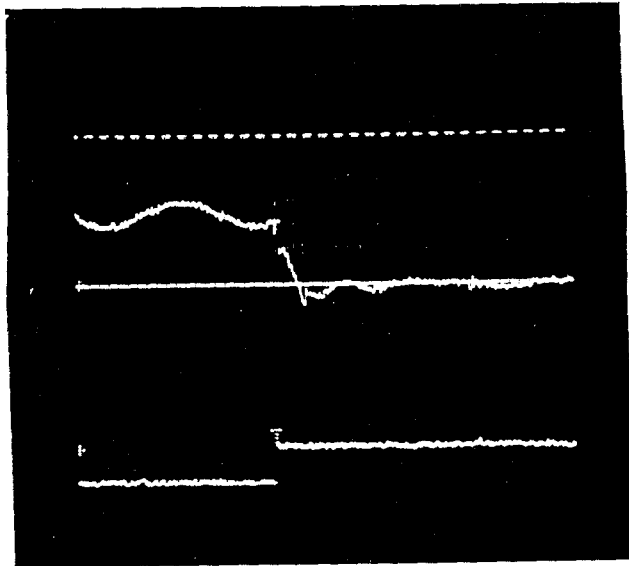
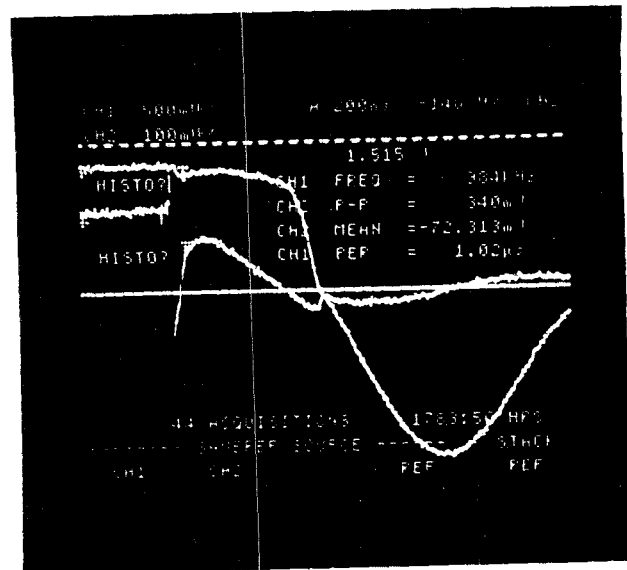


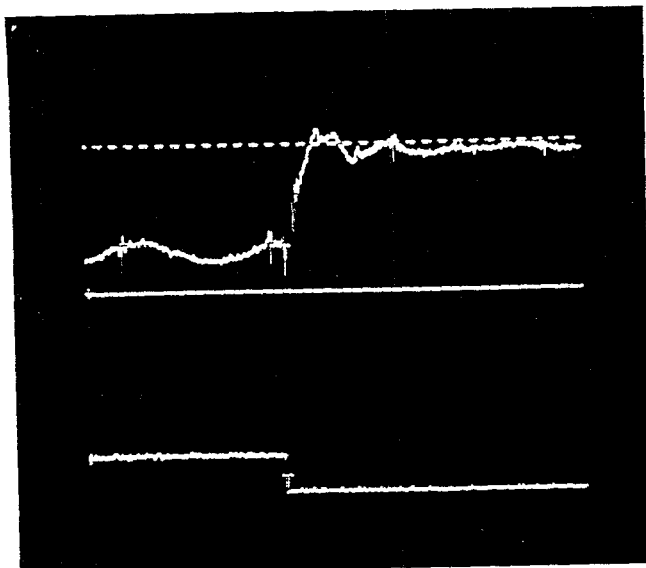
Figure 7: Possible Scheme for Supplying Reference Levels to Clamp Circuit



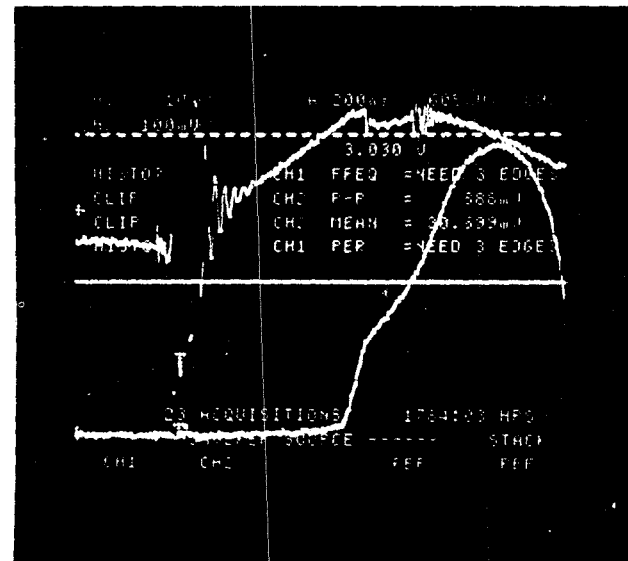
(a)



(b)



(c)



(d)

Figure 6: (a) Clamp function under 3 amp step load. Upper waveform is the output node. The dashed horizontal trace depicts the upper clamp reference level of 3.45V, and the solid horizontal trace depicts the lower clamp reference level of 3.15V. Although divisions are not visible, the scale is $1\mu\text{S}$ per division. The total time depicted is thus about $10\mu\text{S}$. Lower waveform is the gate signal for the pulse load circuit. (b) Time-scale expansion to $200\text{nS}/\text{division}$ of (a), except that second waveform shown at $500\text{mV}/\text{division}$ is the op-amp output waveform that drives the compound pnp pull-up device. (c) Clamp function when 3 amp load is interrupted. Upper waveform is the output node. Lower waveform is gate signal for the pulse load. Scales as in (a). (d) Time-scale expansion to $200\text{nS}/\text{division}$ of (c), except that second waveform shown at $500\text{mV}/\text{division}$ is the op-amp output waveform that drives the compound npn pull-down device.