# A Single-Stage Single-Phase Bi-Directional Grid Interface Circuit with Digital Lookup Table Based Control

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***Abstract*—Emerging load-side commercial and residential building technologies are driving the need for high performance, low cost line-interface systems. This paper reports on the design and test of a single-stage single-phase bi-directional line interface circuit and controller that provides high quality AC line waveforms along with load-line regulation of the DC bus. The circuit is based on a series-parallel connected interleaved flyback topology, with a single integrated coupled magnetic device. A digital controller relies on a lookup table based approach, which utilizes either on-line training or pre-training of the controller so that the internal current waveform loop is effectively run open-loop within a given half-line cycle.**

## I. INTRODUCTION

Emerging technological and societal trends such as renewed interest in distributed photovoltaic generation, electric vehicles, consumer electronics with high full-spectrum efficiency (including low power and standby modes), and other "smart grid" applications are driving the need for a new generation of versatile, high performance, low-cost line-interface converters. In order to meet these needs, power interface system architectures for everything from consumer appliances to electric vehicle battery chargers are moving toward standard two-stage architectures [1] [2] [3] [4].

In this type of architecture, the first stage is generally an AC-DC conversion step, which is necessary to achieve an appropriate interface with the grid such as power factor correction (PFC), as required by standards such as IEC/EN 61000-3-2. However, in the age of the "smart grid" this block is likely to encompass more complex functions such as bi-directional power flow and reactive and harmonic power compensation. This stage is usually itself a two-stage process in order to provide a power-ripple-free DC bus. The second stage in the architecture typically carries out a DC side load regulation function. Here the goal might be as simple as providing galvanic isolation, and a stable noise-free DC voltage, or more complex functions such as load-line regulation [5] [6] or the generation of high-frequency AC [1] [3].

In the case of a rectifier, the front-end AC/DC stage is often accomplished with a boost converter for PFC followed by an isolated DC-DC converter to block the 100Hz or 120Hz ripple. An alternative arrangement that has been proposed in [7] is a single AC/DC stage that incorporates a third power port in order to reduce the size of the DC-link capacitance. This arrangement can be viewed as a variation of the two-stage approach where the second stage lies tangential to the main power path rather than in the direct path. However, in order to achieve both PFC and a regulated output, another power stage must be introduced somewhere in the frontend architecture.

Another possible arrangement for the front-end involves a single-stage converter that utilizes the 120 Hz power ripple for a useful purpose rather than attempting to eliminate it. This is the approach taken in the Enphase Microinverter [8] where the power ripple is used to perform the maximum power point tracking (MPPT) function for the attached solar panel. While this is an exciting approach, since it eliminates the need for a second stage load-side regulation step, it is not easily transferrable to other applications. Another potential application that may tolerate some 120 Hz power ripple is in a battery interface architecture where the battery handles some of the ripple power.

The focus of this work is on a single-stage converter and control methodology to meet the needs of the first stage AC-DC conversion block in the two-stage architecture. Rather than attempt to eliminate the power ripple in the frontend stage, it is presumed that this power ripple will be eliminated in a second point-of-load stage of the architecture. A 1kW interleaved flyback converter topology with coupled magnetics is designed and tested to meet this goal. The circuit is controlled using a feed-forward lookup table based method. Simulation and experimental results are presented below.

## II. CONVERTER TOPOLOGY

A simplified schematic of the proposed topology is shown in Fig. 1. The topology is based on the two-switch flyback

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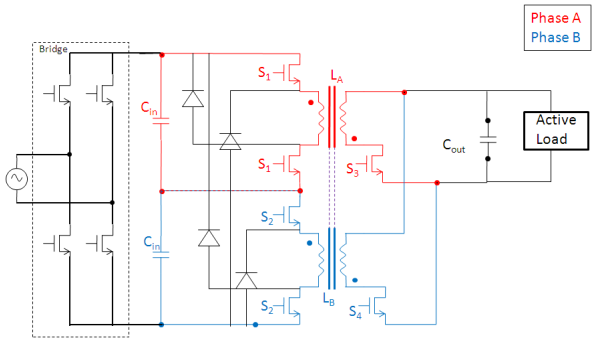


Figure 1. Series/parallel interleaved flyback topology. The two flyback transformers are magnetically coupled.

circuit [9]. Two of these cells are connected in series on the primary and in parallel on the secondary. Much work has been published on active balancing of interleaved power converters [10] [11] [12]. In this circuit, power balance is achieved passively between the two halves, as easily explained here for operation in continuous conduction mode (CCM). In CCM, the voltage and current conversion ratios across a cell are set solely by the duty cycle and the turns ratio. Since the two phases are controlled with identical duty cycles (perhaps phase-shifted) and have matched turns ratios, the parallel secondary connection forces primary side voltage balance, and similarly, the series primary connection forces secondary side current balance. This argument can easily be extended to discontinuous conduction modes.

The two-switch version of the flyback is preferred in this case because the diode clamps (shown in the figure) can be used to protect the primary switches and recover the leakage energy in a lossless manner. Connecting the clamp circuit across the two series-connected phases allows this circuit to achieve DC duty cycles as high as two-thirds, referred to the primary (AC) side without compromising the transformer reset time.

This clamping circuit imposes a fundamental limit on the converter that must be accounted for during the design process. For the flyback topology the output voltage ($V_o$) to input voltage ($V_i$) conversion ratio is shown in (1), where $D$ represents the commanded duty cycle. A maximum duty cycle of two-thirds implies that the maximum conversion ratio is two for a unity turns ratio transformer. In the context of AC line rectification, where the AC-side input is varying while the DC output remains relatively constant, this implies that no energy can be transferred when the input is below one half of the (reflected) output voltage. This limit manifests itself as a limited conduction angle during each line cycle, which is important when considering the harmonic content of the current drawn from the grid. Care should be taken to restrict the lower harmonics to below the limits set by the appropriate standard for the given application. Higher harmonics are less of a concern as they can be controlled with appropriate input filtering.

$$V_o/V_i = D/(1\text{-}D) \qquad (1)$$

The two circuit cells can be operated with a 180° phase shift between their switching waveforms in order to achieve partial ripple cancellation. The extent of the cancellation is duty cycle dependent with the most benefit occurring at a duty cycle of one-half. Further, the use of a coupled magnetic structure implemented by winding both transformers on a common core (see Fig. 2), with a shared gap, leads to further ripple cancellation and potential cost savings in the core. Further current ripple cancellation within the transformer occurs because the MMFs appearing across each transformer outer leg are forced to be equal modulo finite core permeability, which ensures magnetizing ripple current balance between the two stages. Additionally, ripple flux cancellation is achieved in the middle leg, enabling further reduced core losses in this portion of the core.

As explained above, the interleaved flyback topology is most efficient when operated at a duty cycle of one-half. However, to achieve PFC the circuit must be operated over a wide range of conversion ratios. The maximum ratio was set by the use of the clamp circuit at two ($D$ = *2/3)*. The minimum ratio occurs at the maximum input voltage (the peak of the line). In order to achieve high efficiency the commanded duty cycles should nominally be balanced about $D$ = one-half. It is assumed that the grid voltage may vary by as much as 20%. Since the minimum input voltage implies both the highest currents (lowest efficiency) and the smallest conduction angle, this operating point is used to design the primary-referred output voltage. The actual output voltage can then be matched to the desired load using the turns ratio of the transformer. Fig. 3 illustrates the desired design point using the nominal single-phase voltages of the United States. Note that in the figure only half the line voltage is used since this is the input voltage seen by each (half) flyback phase of the circuit.

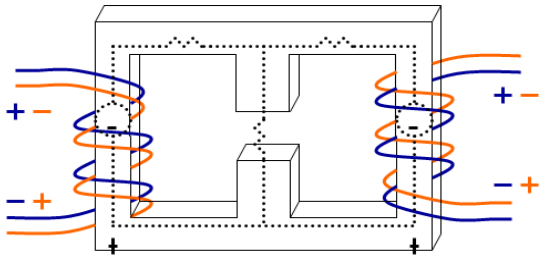

Figure 2. Winding structure of a two phase coupled flyback transformer.

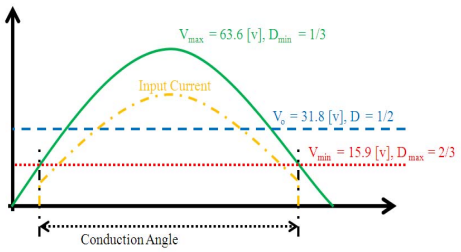


Figure 3. Design of the output voltage referred to the primary. Top curve represents half of the line voltage which is the full voltage seen by each flyback converter. Second curve represents input current waveform. Third curve represents desired output voltage (referred to primary). Fourth curve represents minimum input voltage at which flyback converter will operate due to maximum duty cycle limit.

The topology is capable of bi-directional power flow as well. In order to achieve this, the secondary switches must be implemented with synchronous FETs and the input bridge must be implemented with 60 Hz synchronous switches, as well.

Another consideration is the clamping circuit for the DC-side transistors during inverter operation. Though not shown in Fig. 1, a clamping circuit must be implemented.

The coupled magnetic configuration introduces a more complex set of operating modes if the secondary switches are implemented as diodes or synchronous operated to emulate diodes. In this case, there are two distinct discontinuous conduction modes along with the continuous conduction mode. This multi-mode operating characteristic along with the need to achieve high quality AC waveforms demands that special attention be given to the control scheme. This is the subject of the next section.

## III. Control Design

The trend in control research and practice for PFC and other line-connected applications has been toward fully digital implementations [13] [14] [15] [16]. Much of the effort has been on minimizing sensing requirements, data conversion steps, and the number of calculations that must be performed in the current control loop. In this work a digital technique is proposed and developed that relies on lookup tables to minimize current sensing requirements, data conversion steps, and the amount of calculation that needs to be done in real-time. This is similar to the predictive techniques discussed in [17] [18]. These authors attempt to limit the calculations so that they occur only once per half-line cycle. In the technique developed here, the on-line calculations are eliminated all together. Instead, the necessary duty cycles are pre-programmed using a dedicated on-line or off-line training algorithm.

This control technique works as follows. A lookup table holding the duty cycle trajectory of a single half AC line cycle is used to achieve the current waveform control function. This lookup table could, in principle, have the full resolution of the switching frequency of the circuit. In practice, to save space it is only necessary to have as much resolution as needed to effect control. Typically, this is about 20-30 times the fundamental or ~1-2 kHz of resolution. An interpolating algorithm is used to determine the individual duty cycle commands at each switching instance.

The lookup table is indexed off of the line angle and is populated using a separate training algorithm to be discussed shortly. In addition to the PFC function, it is desired that the output voltage be controlled as well. Since this circuit topology involves a single power conversion stage, removing the 120Hz ripple while achieving PFC is impossible. Instead, a point-of-load regulation stage is responsible for insulating the load from the remainder of the double-line-frequency power ripple.

It is useful to be able to control the DC component of the output. It may be that a specific stiff dc bus voltage is desired, or it may be that more complex behavior is desirable such as load line regulation. This is easily achieved with a relatively slow outer control loop. This loop can operate as slow as 120Hz, in which case, synchronous sampling is effective to alias out the 120Hz ripple. If faster performance is desired, the output ripple can be estimated and removed from the output sampling through digital filtering.

In order to achieve the outer control loop functions while maintaining PFC, the lookup table is expanded into two dimensions where the new axis is indexed off of the output power. At each power level, a full half-line duty cycle trajectory is stored that achieves the PFC function on the input while providing the appropriate output voltage and current. A third dimension may be added as well that is indexed off of the line voltage magnitude. This is particularly useful if the circuit is intended for universal line input. The difference between stiff voltage regulation and load-line techniques is simply utilizing a different set of stored trajectories. Movement between trajectories can be achieved with basic PID control techniques.

The training algorithm involves simple feedback of the input current in order to update the trajectory for the next half-line cycle. In this manner the duty cycle path quickly converges to a fixed periodic trajectory. A trajectory must be stored for each load level; however, interpolation can once again be used to minimize the amount of data that must be stored. Once the correct trajectories are stored, the inherent open-loop stability of the circuit ensures that the control will remain stable without sampling of the input current provided the controller is synchronized to the line. Due to robustness against moderate parameter variation, this training operation can occur purely in off-line simulation with the resulting lookup table applied to the actual circuit. Both control algorithms – operational and training – are shown schematically in Fig. 4.

## IV. Simulation and Experimental Results

A 1kW converter was designed and tested. The estimated loss budget for the primary components of the design is summarized in Table I. The circuit is designed to operate at a

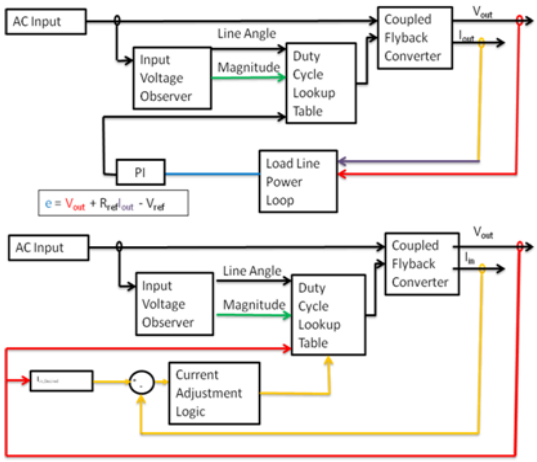


Figure 4. (top) Primary control loop. This control loop uses voltage and/or current feedback to regulate the dc output characteristic. Stiff voltage control or load-line control are possible. (bottom) This control loop implements the training algorithm. The training can be achieved off-line using simulation or one time per nominal design in production.

TABLE I. ESTIMATED LOSS BUDGET

| Component | 1 kW Input Power | |
|---|---|---|
| | *Loss (W)* | *Loss (%)* |
| Bridge | 8.26 | 0.83 |
| Primary Switches | 16.53 | 1.65 |
| Secondary Switches | 12.53 | 1.25 |
| Magnetics | 18.18 | 1.82 |
| TOTAL | 55.50 | 5.52 |

125 kHz switching frequency. The bridge and AC side switches are implemented using two parallel CoolMOS IPP60R099 transistors at each switch. The DC side switches are implemented using two parallel Fairchild FDB28N30 MOSFETs. The coupled flyback transformers were constructed using the Magnetics Inc. core OP49928EC. The windings are constructed using Litz wire with a 14:9 AC to DC side turns ratio. Simulation of the circuit was accomplished using the PSIM power circuit simulator while the control was co-simulated in Matlab using Simulink. Fig. 5 shows the steady state response after training is completed for an average output voltage of 20 V and an output current of 20 A. In all of the simulation and experimental results reported here the load was assumed to be a constant current type. Fig. 6 and 7 show the transient response (input current and output voltage) of the circuit during a step change in the output load. In this case the output current was suddenly switched from 10 A to 20 A.

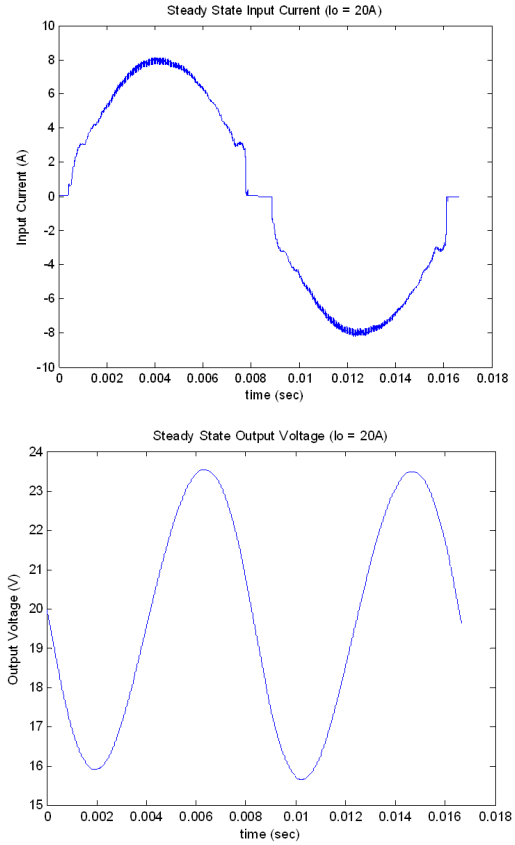


Figure 5. Simulated steady state response for an output current of 20A and an input voltage of 110Vrms. (top) Input Current. (bottom) Output Voltage.

A prototype of the circuit has been built and is currently being tested. Fig. 8 shows the steady state operation for an input of $110V_{rms}$ and an output current of 15 A. The input voltage, input current and output voltage are all shown. Fig. 9 shows the harmonic content of the input current for the case when the output current is 15 A. Fig. 10 shows the duty cycle trajectories for several operating points.

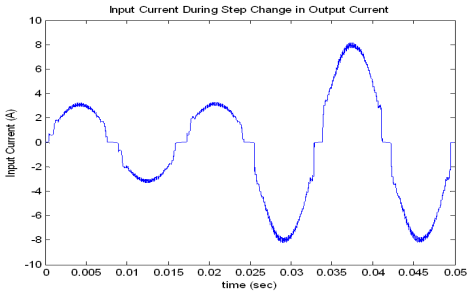


Figure 6. Input current response to a step change in the output current (10A to 20A). The (average) output voltage is constant at 20V.

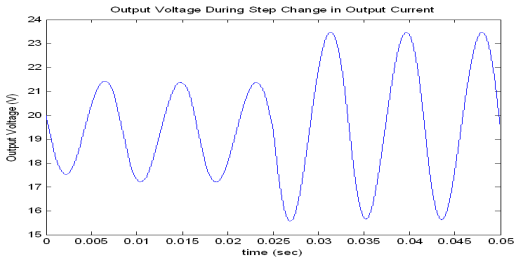


Figure 7. Output voltage response to a step change in the output current (10 A to 20 A).

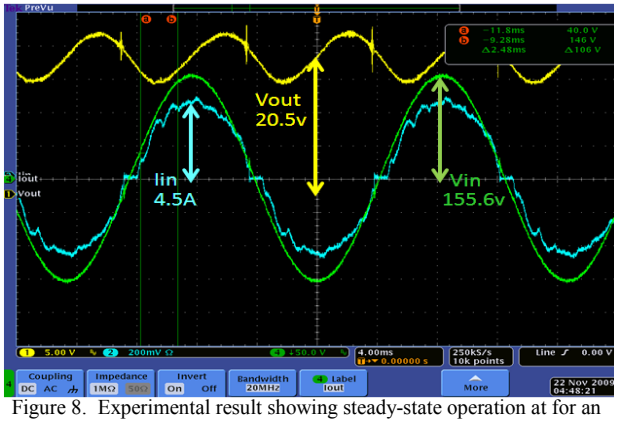


Figure 8. Experimental result showing steady-state operation at for an input voltage 110 Vrms and an output current of 15 A. The top curve shows the output voltage (5V/div). The middle curve shows the input voltage (50V/div). The lowest curve represents the input current (2A/div).

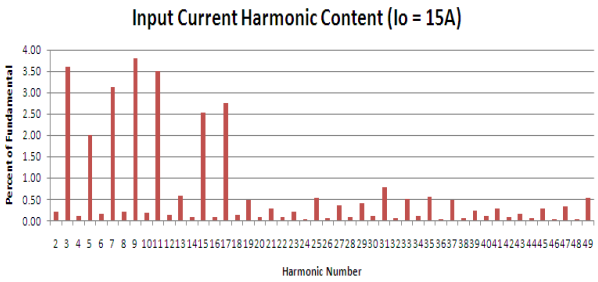


Figure 9. Harmonic content as a percentage of the fundamental of the input current during steady state operation of the circuit with a 15 A load. The input voltage is 110 Vrms.

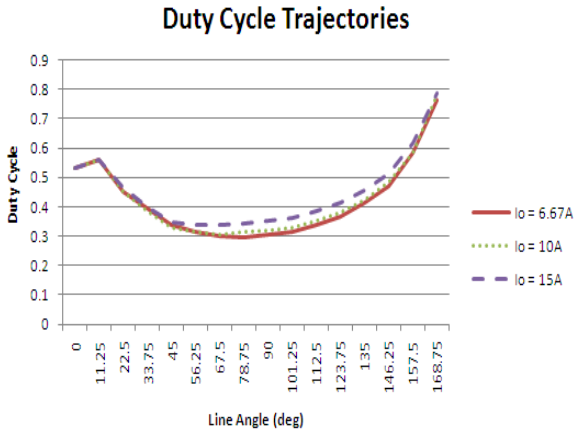


Figure 10. Several steady-state duty cycle trajectories as a function of line angle. Each trajectory has been trained to produce a 20V output at the given output current level. From top to bottom they are 15A, 10A, 6.67A.

## V. Conclusions and Further Work

This work demonstrates a circuit topology and its control scheme for single-phase PFC rectification and inversion using the flyback converter as a building block. A control technique based on lookup table "open-loop" PFC with closed loop power control is demonstrated. The lookup table is trained in advance either using simulation tools or another control loop implemented in hardware.

Work is continuing on the experimental platform. In the future we will demonstrate the closed loop control as well as experimentally verify the efficiency of the circuit. Bi-directional power flow will also be demonstrated.

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