Design of Ceramic–Capacitor VRM's with Estimated Load Current Feedforward

Angel V. Peterchev Seth R. Sanders
Department of Electrical Engineering and Computer Science
University of California, Berkeley, USA
Email: peterch@eecs.berkeley.edu, sanders@eecs.berkeley.edu

***Abstract*— For voltage regulator module (VRM) designs with ceramic output capacitors, the capacitor size has to be chosen sufficiently large to allow for the use of relatively large inductor values. This enables operation at conventional switching frequencies, while meeting load transient response specifications. Due to the small effective series resistance (ESR) time constant of ceramic capacitors, this may result in designs with output capacitor ESR substantially lower than the desired output impedance. This is in contrast to conventional VRM implementations with electrolytic capacitors, where the desired output impedance is closely related to the output capacitor ESR. In ceramic capacitor designs with conventional feedback control, the required loop bandwidth is inversely proportional to the output capacitor size. The feedback bandwidth is limited by stability constraints linked to the switching frequency. The use of load current feedforward can extend the useful bandwidth beyond the limits imposed by feedback stability constraints. Load current feedforward is used to handle the bulk of the regulation action, while feedback is used only to compensate for imperfections of the feedforward and to ensure tight DC regulation. An experimental converter demonstrates tighter output regulation with estimated load current feedforward, than with pure feedback control.**

I. Introduction

The specifications for modern voltage regulator modules (VRM's) require that the microprocessor supply voltage V_o follows a load line,

$$V_o \rightarrow V_{ref} - R_{ref} I_o, \tag{1}$$

where V_{ref} is the reference voltage, R_{ref} is the desired load line slope (or regulator output impedance), and I_o is the current drawn by the microprocessor load (see Table I). A method for load-line regulation (a.k.a. adaptive voltage positioning), where the closed-loop output impedance is set equal to the output capacitor effective series resistance (ESR), was introduced in [1] and widely adopted. Load-line regulation implementations based on feedback current-mode control [1], [2] and voltage-mode control with feedback load current injection [3], [4], have been presented, using power trains with electrolytic output capacitors. With this approach, the nominal system closed-loop bandwidth is tightly related to the output capacitor ESR time constant [1], [2]. With conventional electrolytic capacitors having such a time constant on the order of 10 μs, it is straightforward for this approach to work with conventional switching frequencies in the range of 200–500 kHz. For modern VRM applications, ceramic capacitors present an attractive alternative to electrolytics due to their low ESR and low effective series inductance (ESL), better reliability, and low profile. However, ceramic capacitors have ESR time constants of about 0.2 μs, yielding the conventional load-line design framework unworkable, since it would require switching frequency on the order of 10 MHz [2].

TABLE I
VRD/VRM SPECIFICATIONS

V_{in}	input voltage	12 V
V_{ref}	reference output voltage	0.84–1.60 V
$I_{o,max}$	max load current	75–90 A
ΔI_o	max dynamic load step	55 A
τ_I	load step time const.	85 ns
R_{ref}	closed-loop output impedance	1.3 mΩ
ΔV_o	output tolerance band	$\pm$ 25 mV
ΔV_p	max extra unloading overshoot	50 mV
Δt_p	max extra overshoot duration	25 μs

Source: Intel Corp. [5], [6]

In this paper, we show that for representative VRM designs with ceramic output capacitors, the capacitor size has to be chosen sufficiently large to allow for the use of inductor values in the range of hundreds of nH. This enables efficient operation at conventional sub-megahertz switching frequencies, while meeting load transient response specifications. Due to the small ESR time constant of ceramic capacitors, this may result in designs with output capacitor ESR substantially lower than the desired output impedance. This is in contrast to conventional VRM designs with electrolytic capacitors, where the desired output impedance is closely related to the output capacitor ESR.

In ceramic capacitor designs with conventional feedback control, the required loop bandwidth is inversely proportional to the output capacitor size. Extending the bandwidth can result in cost and board area savings, since it can reduce the required number of capacitors. However, bandwidth in a feedback-controlled converter is limited by stability constraints linked to the switching frequency. We propose and demonstrate the use of load current feedforward to extend the useful bandwidth beyond the limits imposed by feedback stability constraints. In this approach, the load current feedforward is used to handle the bulk of the regulation action, while the feedback is used only to compensate for imperfections of the feedforward and to ensure tight DC regulation. A scheme for load current estimation based on lossless inductor and capacitor current sensing, is discussed. Finally, we present experimental converter data, which demonstrates tighter output regulation with estimated load current feedforward, than with pure feedback control.

II. Power Train Design

Fig. 1 shows the simplified structure of a representative four-phase microprocessor VRM. In the analysis in this paper, the multi-phase converter is modeled as a single-phase converter for simplicity, unless stated otherwise. In this section, we

0-7803-8399-0/04/$20.00 ©2004 IEEE.

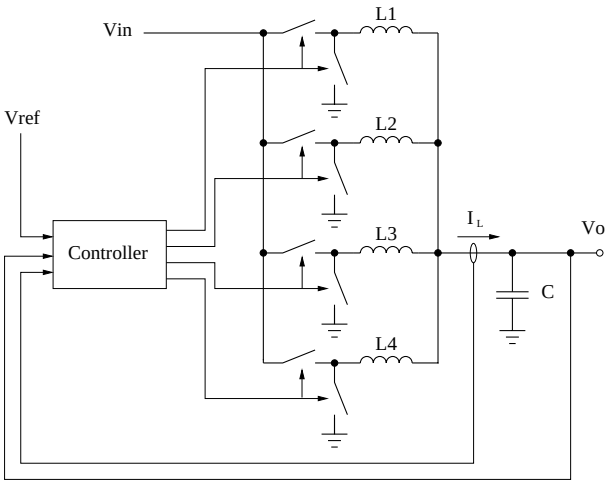

Fig. 1. Four-phase VRM structure.

discuss VRM power train design based on load transient response specifications, with a focus on VRM's using only ceramic output capacitors.

A. Critical Inductance

In low-conversion ratio VRM's, the unloading current transient represents the critical conditions for converter performance. During a large unloading transient, only the (low) output voltage can be imposed across the inductors to slew down the inductor current, while the output still has to follow (1), possibly with some allowed extra overshoot ΔV_p (Fig. 2). The critical inductance L_{crit} is the largest total inductance value (all phase inductors in parallel) for which this condition is met during a worst-case unloading current step.

Previous derivations of the critical inductance in [3] and [7], use assumptions which yield the critical inductance value directly proportional to the output capacitor ESR time constant $\tau_C = r_C C$, where C is the output capacitance and r_C is the ESR. As a result, these analyses suggest the need for very low critical inductance values for VRM's using low-ESR ceramic output capacitors, implying, in turn, the need for high switching frequencies. Further, these derivations assume infinite load current slew rates ($\tau_I = 0$), and no unloading overshoot ($\Delta V_p = 0$), while VRM specification list finite values (Table I). Here, we present an extended analysis, which reveals a more detailed relation between the critical inductance value and other key power train parameters.

Fig. 2 shows a model of the VRM response for a large unloading transient. The unloading current step can be modeled by a magnitude ΔI_o and a time constant τ_I which characterizes the slew rate,

$$I_o(t) = I_o(0) - \Delta I_o(1 - e^{-t/\tau_I}), \tag{2}$$

for $t \geq 0$. The maximum control effort the VRM controller can exert after a large unloading transient, is to saturate the duty ratio to zero after some delay t_d inherent in a physical implementation (Fig. 2). The behavior of the output voltage is

$$V_o(t) = \frac{\Delta I_o}{C}\left[t + (\tau_C - \tau_I)\left(1 - e^{-t/\tau_I}\right)\right] + V_o(0), \tag{3}$$

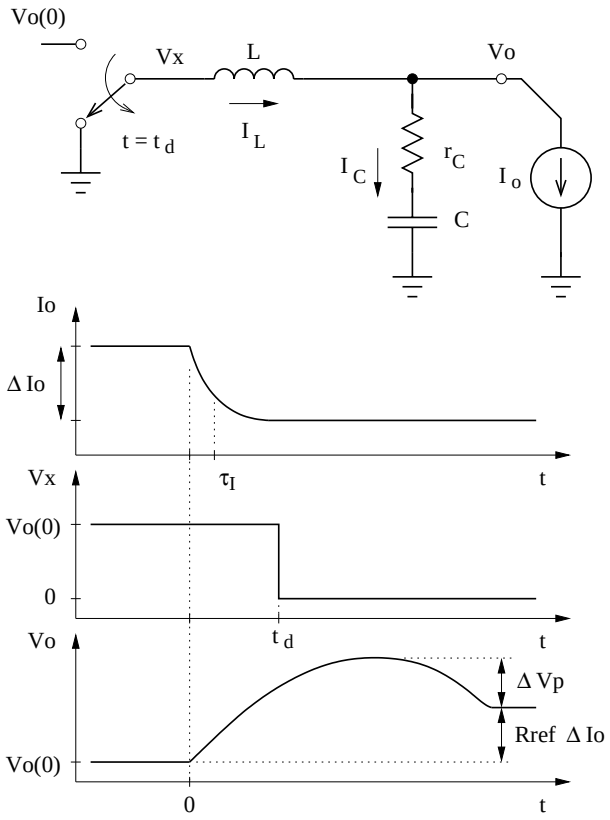

Fig. 2. VRM transient response model for a large unloading current step.

for $0 \leq t < t_d$, and

$$V_o(t) = \frac{\Delta I_o}{C}\left[t - \frac{V_{ref}}{2L\Delta I_o}(t - t_d)^2 - \frac{V_{ref}\tau_C}{L\Delta I_o}(t - t_d) + \right. \\ \left. + (\tau_C - \tau_I)\left(1 - e^{-t/\tau_I}\right)\right] + V_o(0), \tag{4}$$

under duty ratio saturation, for $t \geq t_d$. The maximum voltage value $max(V_o)$ is reached for $t \geq t_d$, thus the critical inductance can be derived from (4), by setting

$$max(V_o) - V_o(0) \triangleq R_{ref}\Delta I_o + \Delta V_p, \tag{5}$$

yielding

$$L_{crit} \approx \frac{V_o}{\Delta I_o}\left(\tau_* + \sqrt{\tau_*^2 - \tau_C^2}\right), \tag{6}$$

where

$$\tau_* = C\left(R_{ref} + \frac{\Delta V_p}{\Delta I_o}\right) + \tau_I - t_d, \tag{7}$$

and

$$V_o = V_{ref} - R_{ref}(I_{o,max} - \Delta I_o). \tag{8}$$

The critical inductance per phase in an N-phase converter is $L_{i,crit} = NL_{crit}$. Equations (6)–(8) take into account the load time constant (modeling the slew rate) and the unloading overshoot. Further, they treat as independent parameters the capacitor ESR and the output impedance, as well as the controller bandwidth (or delay) and the output capacitor ESR time constant, which were previously treated as equivalent. For $R_{ref} = r_C$, $\tau_I = 0$, $t_d = 0$, and $\Delta V_p = 0$, the results are consistent with those in [3] and [7].

The most important observation from (6) and (7) is that the critical inductance depends strongly on the output capacitance, rather than on the ESR time constant, when the output impedance is allowed to assume values different from the capacitor ESR. This implies that in ceramic capacitor VRM designs, the output capacitance has to be chosen sufficiently large to allow for a reasonably high inductance value, and thus enable operation at conventional switching frequencies (e.g., $<$ 1 MHz). Due to the small ceramic capacitor ESR time constant, this results in designs where the ESR is smaller than the specified output impedance R_{ref}.

For a design example, consider the critical inductance for the VRM specifications in Table I. Assume a 4-phase converter with V_{ref} = 1.3 V, C = 800 μF, τ_C = 0.2 μs, and t_d = 100 ns. Then from (6)–(8), we obtain $L_{i,crit} \approx$ 318 nH per phase. These power train parameters allow efficient operation with a 1 MHz switching frequency. Note that if unloading overshoot is not allowed ($\Delta V_p = 0$), the critical inductance is reduced substantially, $L_{i,crit} \approx$ 185 nH. Further, the critical inductance for the *loading* transient is approximately 1.58 μH—much larger than $L_{i,crit}$. This confirms the observation that the unloading transient presents the critical conditions for the transient design. Finally, note that the output capacitor ESR is 0.25 mΩ, five times less than R_{ref}.

III. Controller Architecture and Design

While the previous section addressed power train design considerations for all-ceramic capacitor VRM's, here we discuss the appropriate control strategies for regulating the output impedance to meet the specifications in Table I.

A. Output Impedance Regulation

Conventional load-line VRM control sets the desired closed-loop impedance equal to the output capacitor ESR [1]. However, the discussion in Section II indicates that in ceramic capacitor VRM designs, the output capacitor ESR may be substantially smaller than R_{ref}, to enable operation at moderate switching frequencies. Under these circumstances, it is natural to modify the load line so that the output impedance is

$$Z_{ref} \triangleq R_{ref} \frac{1 + s\tau_C}{1 + sR_{ref}C}, \tag{9}$$

instead of R_{ref}. With this approach the output impedance is specified *dynamically*, as a generalization of the resistive output impedance specified in conventional load-line control. This behavior is illustrated in Fig. 3. Importantly, the controller has to be designed so that the output impedance is regulated to Z_{ref} and not to R_{ref}, since the latter approach will result in undesirable behavior, when during a load transient, the controller initially acts to change the inductor current in direction *opposite* to the load step, eventually producing additional output voltage overshoot.

B. Output Current Feedforward

It has been shown that for conventional VRM designs with current-mode control, where $R_{ref} = r_C$, the voltage-loop bandwidth should be equal to $1/\tau_C$ rad/s, to ensure appropriate output impedance control [1], [2]. Further, the current-loop should have wider bandwidth than the voltage-loop. In VRM designs with voltage-mode load-line control [3], [4], the loop bandwidth has to be larger than $1/\tau_C$, to provide tight load-line regulation. Since in both cases the feedback controller bandwidth is constrained by the switching frequency for stability reasons [8], these approaches require very high switching frequencies, on the order of 10 MHz, for ceramic capacitor designs.

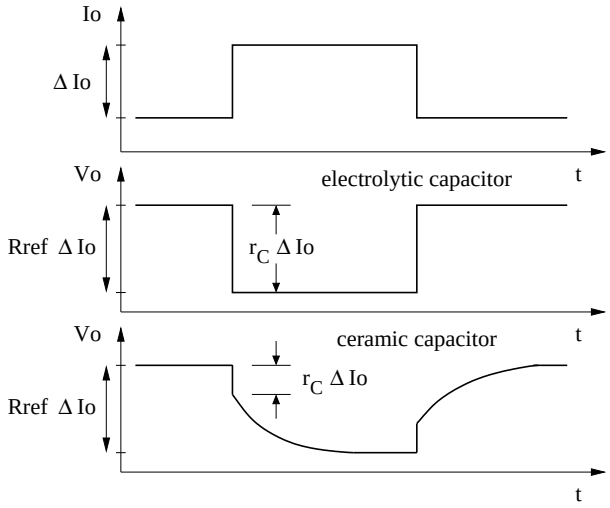

Fig. 3. Current step transient response with load-line regulation, with electrolytic and ceramic capacitors, assuming no duty ratio saturation occurs.

On the other hand, in the generalized load-line regulation approach discussed here, for $R_{ref} \geq r_C$, the feedback loop bandwidth should exceed $1/R_{ref}C$, which corresponds to the dominant time constant characterizing the output impedance (9). Thus, if conventional feedback control is used, the output capacitor should be selected sufficiently large, so that $1/R_{ref}C$ is less than the practical feedback loop bandwidth. Clearly, in this case there is a trade-off between the number of output capacitors required and the switching frequency used. To eliminate this constraint, and thus enable operation at moderate switching frequencies ($f_{sw} <$ 1 MHz), with a small number of ceramic capacitors ($C <$ 1 mF), we introduce load current feedforward. Load current feedforward can decrease the converter response time, without an increase of the switching frequency, since *the gain and bandwidth of the feedforward are not limited by stability considerations*, in contrast to pure feedback regulation. The use of load current feedforward to speed up the load transient response in current-mode converters with stiff voltage regulation, has been demonstrated in [9].

The discussion in Section III-A suggests that the VRM output should follow a dynamic load line given by

$$V_o \rightarrow V_{ref} - Z_{ref} I_o. \tag{10}$$

The problem of V_o following accurately a load line can be approached as a reference tracking problem, where V_o has to track the right-hand side of (10). An effective approach in tracking problems is to use feedforward from the reference

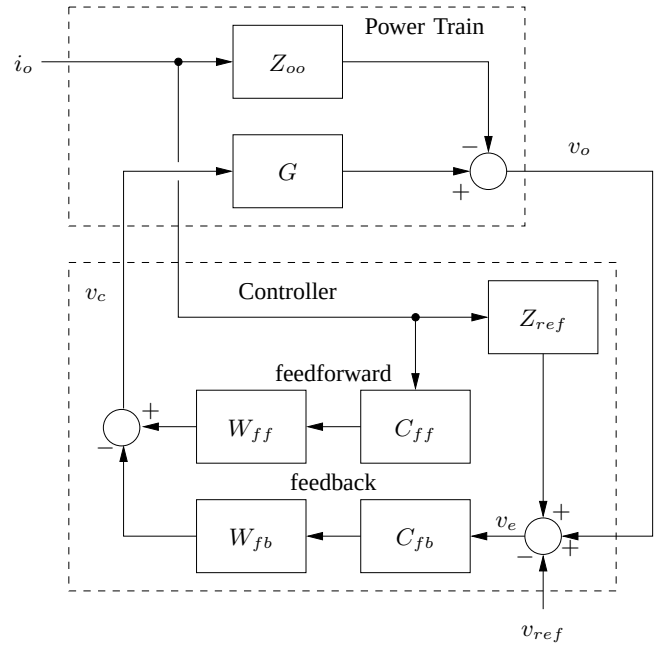

Fig. 4. VRM control block diagram with voltage-mode control.

signal (the load current I_o in this case[1]) to the controller output (the PWM duty ratio) to handle the bulk of the regulation action, and use the feedback only to damp resonances, and compensate for the imperfections of the feedforward [10].

C. Controller Structure

A control block diagram of the VRM with voltage-mode control and load current feedforward is shown in Fig. 4. Here,

$$G(s) = \frac{sr_C C + 1}{s^2 LC + s(r'_L + r_C)C + 1} \tag{11}$$

is the transfer function between the controller command and the output voltage, $L = L_i/N$ is the total power train inductance for an N-phase converter, and r'_L is the series combination of the inductor resistance and the average switch resistance. The open-loop output impedance is

$$Z_{oo}(s) = \frac{r'_L(sr_C C + 1)(sL/r'_L + 1)}{s^2 LC + s(r'_L + r_C)C + 1}. \tag{12}$$

Transfer functions C_{fb} and C_{ff} represent the feedback and feedforward control laws, respectively. The delay and bandwidth of the feedback and feedforward paths are modeled by

$$W_{fb}(s) = \frac{e^{-st_{d,fb}}}{s/\omega_{BW} + 1} \quad \text{and} \quad W_{ff}(s) = \frac{e^{-st_{d,ff}}}{s/\omega_{BW} + 1}. \tag{13}$$

From Fig. 4 the converter closed-loop output impedance is calculated to be

$$Z_o = \frac{Z_{oo} + G(Z_{ref} W_{fb} C_{fb} - W_{ff} C_{ff})}{1 + G W_{fb} C_{fb}}. \tag{14}$$

[1]In this discussion we are assuming that V_{ref} is constant. In modern microprocessor systems V_{ref} can be adjusted during operation, but this happens at slow rates compared to changes in I_o, and hence tracking it does not present a substantial challenge. In fact, a simple and effective reference voltage feedforward, providing good tracking up to the LC cutoff frequency, can be accomplished by directly adding V_{ref} to the input of the PWM modulator.

Finally, note that in previously proposed VRM controller architectures in [3], and replicated in [4], the load current was injected only in the feedback (C_{fb}) path to provide load line regulation. However, it has not been used for direct feedforward (via C_{ff}), thus not utilizing its potential to increase the controller speed of response.

D. Feedforward Control Law

The feedforward control law can be derived by setting the closed-loop output impedance (14) equal to the desired value Z_{ref}, yielding

$$C_{ff}(s) \triangleq \frac{Z_{oo} - Z_{ref}}{W_{ff} G}. \tag{15}$$

Note that if the ideal feedforward in (15) could be implemented, the output impedance would have the desired value $Z_o = Z_{ref}$ and no feedback is necessary. In reality, this is impossible due to parameter uncertainties and the fact that W_{ff} contains delay, thus C_{ff} would be anticausal. A practical implementation C'_{ff} can approximate C_{ff} with an error δC_{ff},

$$C'_{ff} = C_{ff} + \delta C_{ff}. \tag{16}$$

Then the output impedance (14) becomes

$$Z_o = Z_{ref} - \delta C_{ff} \frac{G W_{ff}}{1 + G W_{fb} C_{fb}}. \tag{17}$$

Thus, the feedforward carries out the bulk of the regulation action, and the feedback acts only to decrease the uncertainty δC_{ff} of the feedforward. In particular, at low frequencies the uncertainty term in (17) approaches zero due to the high feedback gain, while at very high frequencies it is attenuated by the rolloff of G.

Expanding (15) yields the exact expression for the feedforward law,

$$C_{ff}(s) = \Big\{ s^2 LC r_C \left(1 - \tau_C R_{ref}/L\right) + \\ + s\big[L + \tau_C (r'_L - 2R_{ref})\big] + r'_L - R_{ref} \Big\} \Big/ \\ \Big/ \Big\{ (s\tau_C + 1)(sR_{ref}C + 1) W_{ff}(s) \Big\}. \tag{18}$$

Noting that $L/R_{ref} \gg \tau_C$ and $L \gg |\tau_C(r'_L - 2R_{ref})|$, and further ignoring the delay term and the DC term, since DC regulation is handled by the integral feedback, the feedforward law can be approximated as

$$C_{ff}(s) \approx \frac{sL}{sR_{ref}C + 1}. \tag{19}$$

Thus, the design of the feedforward law with voltage-mode control requires knowledge of the power train inductance and output capacitance.

E. Feedback Control Law

The feedback control can use a standard approach, such as a PID law with an additional high-frequency pole $1/\tau_{hf}$,

$$C_{fb}(s) = K \left(1 + \frac{1}{T_I s} + T_D s\right) \frac{1}{s\tau_{hf} + 1}. \tag{20}$$

The derivative term zero provides a -20 dB/dec rolloff above the LC cutoff frequency, to ensure a good phase margin.

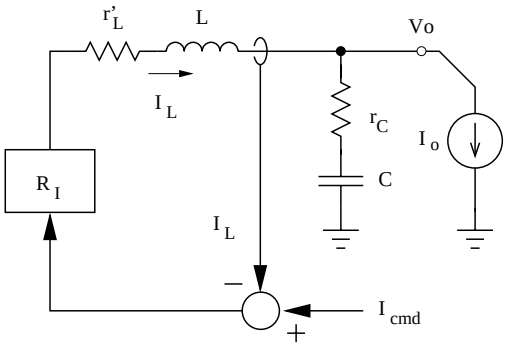

Fig. 5. Model of current modulator with current (inner) loop closed.

The high-frequency pole limits the derivative gain beyond the unity-gain frequency. Conventional design procedures can be used to choose the PID parameters to yield good phase and gain margins [11].

F. Current-Mode Control

Fig. 5 gives the model of a buck converter with a current mode controller. Parameter I_{cmd} is the current command provided by the voltage (outer) control loop. The block diagram of the whole system, with the current (inner) loop closed, has the same structure as that in Fig. 4, except now the voltage-loop controller generates a current command I_{cmd} which is fed to the current controller. The transfer function between the current command and the output voltage, with the current-loop closed, is

$$\mathcal{G}(s) = \frac{R_I(sr_C C + 1)}{s^2 LC + s(R_I + r'_L + r_C)C + 1}, \tag{21}$$

where R_I models the current-loop gain. The corresponding open-voltage-loop output impedance is

$$\mathcal{Z}_{oo}(s) = \frac{(R_I + r'_L)(sr_C C + 1)\left(s\frac{L}{R_I + r'_L} + 1\right)}{s^2 LC + s(R_I + r'_L + r_C)C + 1}. \tag{22}$$

Transfer functions $\mathcal{C}_{fb}$ and $\mathcal{C}_{ff}$ represent the feedback and feedforward control laws, respectively, with the corresponding delay and bandwidth modeled by $\mathcal{W}_{fb}$ and $\mathcal{W}_{ff}$. Note that for high current-loop gain R_I, both (21) and (22) become independent of the inductor value L, since the current loop provides for this desensitivity [11]. In practice, R_I is limited by current-loop stability considerations [11], [8].

The feedforward control law is derived analogously to that in the voltage-mode case in Section III-D,

$$\mathcal{C}_{ff}(s) = \Big\{ s^2 LCr_C\,(1 - \tau_C R_{ref}/L) + \\ + s\big[L + \tau_C(R_I + r'_L - 2R_{ref})\big] + R_I + r'_L - R_{ref} \Big\} \Big/ \\ \Big/ \Big\{ R_I(s\tau_C + 1)(sR_{ref}C + 1)W_{ff}(s) \Big\}. \tag{23}$$

Assuming high current-loop gain R_I and ignoring the delay term, the feedforward law can be approximated by

$$\mathcal{C}_{ff}(s) \approx \frac{1}{sR_{ref}C + 1}. \tag{24}$$

The feedback control can use a simple PI law,

$$\mathcal{C}_{fb}(s) = \mathcal{K}\left(1 + \frac{1}{\mathcal{T}_I s}\right), \tag{25}$$

since current-mode control provides a -20 dB/dec rolloff up to the current-loop bandwidth, and hence no derivative term is necessary. One major advantage of current-mode control is that, unlike the voltage-mode case, no precise knowledge of L is needed for the design of $\mathcal{C}_{ff}$ and $\mathcal{C}_{fb}$, thus allowing for more *robust* controller designs.

G. Estimating the Load Current

The control strategy discussed above assumes that the load current is measured. Sensing the load current directly is not practical since it will require inserting a sense resistor in the load current path, thus increasing the output impedance and power loss, or using an expensive Hall-effect current sensor. Alternatively, the load current can be reconstructed from estimates of the inductor and capacitor currents since $I_o = I_L - I_C$ [3], [4].

The inductor current I_L can be estimated with individual RC networks connected in parallel with the inductors. This approach has been used successfully in commercial products [12]. A two-phase VRM implementation block diagram is shown in Fig. 6 to illustrate a variation of this approach. Since the two inductors are identical, we use a single estimator capacitor $C_{L,s}$ and two resistors $R_{L,s1}$ and $R_{L,s2}$, connected to the switching nodes. This approach has been used in [4], and can be extended to any number of phases. If the time constant of the estimator matches the time constant of the inductor,

$$R_{L,s}C_{L,s} = \hat{\tau}_L \triangleq \tau_L = L/r_L, \tag{26}$$

where $R_{L,s} = R_{L,s1}||R_{L,s2}$, the voltage across $C_{L,s}$ is equal to the average voltage across r_{L1} and r_{L2}. The *total* inductor current can then be obtained by dividing the voltage across $C_{L,s}$ by an estimate of the series resistance $\hat{r}_L$ of the two inductors in parallel. For good matching, the temperature dependence of r_L has to be compensated in the sensing amplifier [12].

Analogously, the capacitor current I_C can be estimated from the output voltage with an RC network matching the time constant of the output capacitor. In Fig. 6, $R_{C,s}$ and $C_{C,s}$ are chosen such that

$$R_{C,s}C_{C,s} = \hat{\tau}_C \triangleq \tau_C. \tag{27}$$

The capacitor current is derived by dividing the voltage drop across $R_{C,s}$ by an estimate of the output capacitor ESR, $\hat{r}_C$. It should be noted that in an actual implementation, the signal fed to the capacitor current estimator should be sensed across the bulk capacitors, while the output voltage signal for the feedback regulation is sensed at the microprocessor package.

In the case of perfect matching of the estimator and power train parameters, $\hat{I}_o = I_o$, the injection of $\hat{I}_o$ in the controller does not affect the closed-loop poles and zeros of the system. In practice, there typically is some mismatch between the estimator and power train parameters, resulting in $\hat{I}_o$ becoming a function of the converter state variables and hence altering the system pole and zero locations. For small mismatches this

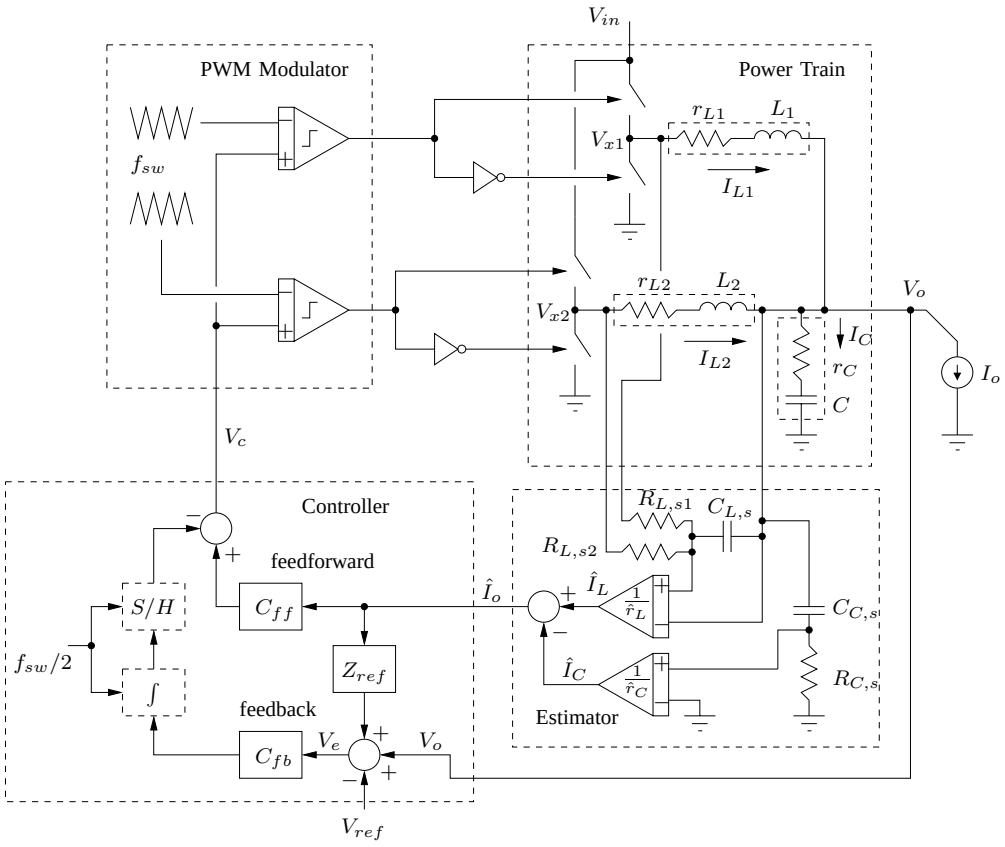

Fig. 6. Two-phase VRM implementation block diagram.

effect is small, and can be tolerated in a properly designed controller.

H. PWM Modulator

The control signal fed into the PWM modulator is the sum of the outputs of the feedforward and feedback control laws (Fig. 6). The load current feedforward signal ideally is not related to the converter state variables since it is derived from an exogenous variable I_o. Thus, the output of the feedforward control law C_{ff} can be fed directly to the PWM modulator *without bandwidth limitations related to the switching frequency*. The modulation of the feedback signal, however, can possibly cause subharmonic instability resulting from the closed-loop bandwidth approaching relatively near the switching frequency due to the small power train energy storage element values [8]. To prevent this from happening, a sample-and-hold (S/H) operating at the effective switching frequency $f_{sw,eff} = f_{sw}/N$ of an N-phase converter, could be introduced in the feedback path, thus eliminating switching ripple and reducing the bandwidth of the control signal. The sample-and-hold could be preceded by a resettable integrator ($\int$) averaging the feedback signal over each effective switching period ($1/f_{sw,eff}$), and thus providing good DC accuracy of the feedback control. The sample-and-hold and the resettable integrator would introduce some additional delay in the feedback path, however this is not critical to the overall speed of response since fast load changes are handled by the feedforward path. As pointed out in Sections III-B and III-D, the feedback path only compensates for imperfections in the feedforward control, and ensures DC accuracy.

A switch modulation scheme having a very low latency for unloading transients, is essential for achieving a fast controller response with load current feedforward. Good candidates include unlatched PWM, leading-edge latched PWM, two-sided latched PWM [13], and valley current-mode control [14]. All of these have turn-off latency equal to or less than the steady-state on-pulse-width, which is about a tenth of the switching period in 12-V VRM's. Hysteretic modulation also offers very fast response [9], however its switching frequency is not fixed, and it is difficult to generalize it to multi-phase power trains.

IV. Experimental Results

To test the concepts discussed in this paper, a 1 MHz, 120 A, 4-phase synchronous buck converter board (International Rectifier IRDCiP2002-C) was modified to incorporate estimated load current feedforward and load-line regulation with the controller structure in Fig. 6. The on-board voltage mode PWM modulator with phase current balancing (Intersil ISL6558) was used. The converter parameters follow the design example in Section II-A, except that the phase inductors are larger, $L_i \approx 390$ nH @ 60 A, and $t_d \approx 300$ ns due to limitations of the PWM modulator. The PID control law was designed to provide 48° phase margin and 10 dB gain margin with 190 kHz crossover frequency.

Figures 7 and 8 show the VRM transient response, with and without estimated load feedforward, for 52 A loading

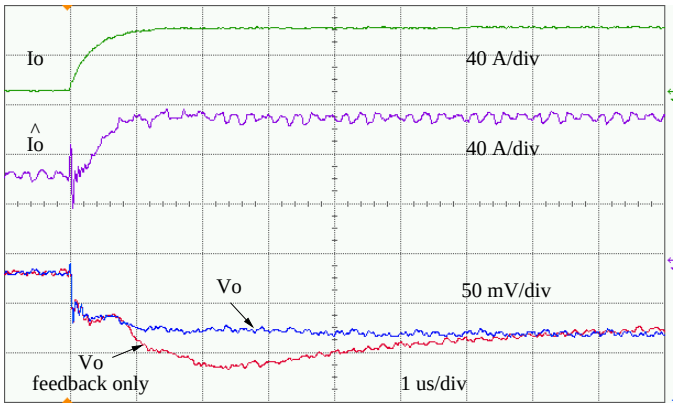

Fig. 7. A 52 A loading transient with corresponding estimated load current and output voltage with and without load current feedforward.

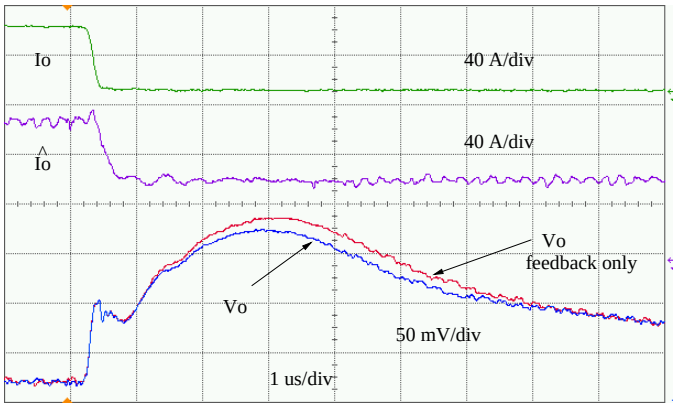

Fig. 8. A 52 A unloading transient with corresponding estimated load current and output voltage with and without load current feedforward.

and unloading transients between 60 A and 112 A. Due to hardware constraints on the pulsed load circuit, the loading current step is relatively slow with a time constant of about 500 ns. The unloading current step, which tests the critical performance of the converter, is much faster, completing the step in 200 ns commensurate with the specifications in Table I.

From the figures it can be seen that the estimated load current follows very well the measured current with a delay of about 100 ns. The 4 MHz switching noise present in the load current estimate results from parasitic coupling to the sense wires which were soldered on top of the VRM board. The switching noise does not affect the DC regulation precision because it is attenuated by the PID controller. Further, in a dedicated implementation, the sensing can be done through buried PCB traces, thus reducing both electrostatic and magnetic pickup.

From the loading transient in Fig. 7 it can be seen that with combined feedback and feedforward control, the output voltage follows very well the desired load line. With only feedback, however, there is an extra sag of about 40 mV reflecting the inability of the feedback controller to tightly regulate the output impedance. Note that this overshoot is due to bandwidth limitations of the feedback controller, since the feedback loop crossover frequency is not significantly larger than $1/R_{ref}C$, as required in Section III-B. The observed

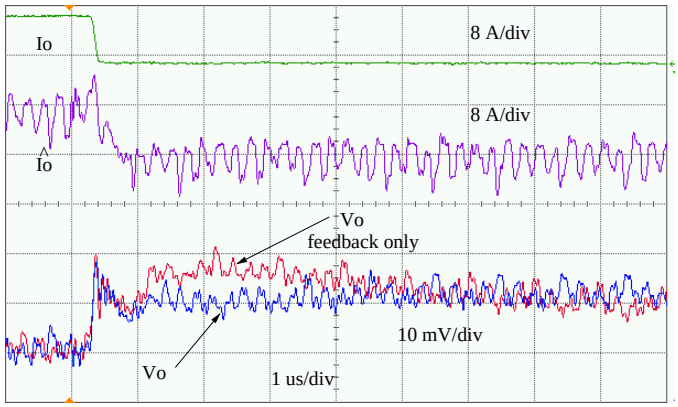

Fig. 9. A 8 A unloading transient with corresponding estimated load current and output voltage with and without load current feedforward.

overshoot is not a result of duty ratio saturation, since the phase inductor value is substantially smaller than the critical inductance of 1.58 μH for *loading* transients, calculated in Section II-A.

In the unloading transient in Fig. 8, an extra overshoot of about $\Delta V_p \approx 85$ mV can be observed, which is expected given the prototype parameters listed above. This response corresponds to the duty ratio being saturated to zero about 300 ns after the beginning of the load step. Here too, the combined feedback and feedforward control produces a better voltage response than the feedback alone, implying a faster transition to duty ratio saturation. In implementations using a faster modulator, the advantage of the feedforward scheme is expected to be even greater for large unloading transients, since the duty ratio can be driven to saturation even faster. Finally, Fig. 9 shows a smaller 68-to-60 A unloading transient which does not drive the duty ratio to saturation. Analogously to the loading transient example in Fig. 7, it is clear that the combination of feedback and feedforward provides tighter output impedance regulation than feedback alone.

V. Conclusion

For representative VRM designs with ceramic output capacitors, the capacitor size has to be chosen sufficiently large to allow for the use of inductor values in the range of hundreds of nH, thus enabling efficient operation at conventional sub-megahertz switching frequencies. Due to the small ESR time constant of ceramic capacitors, this may result in designs with output capacitor ESR substantially lower than the desired output impedance. This is in contrast to conventional VRM designs with electrolytic capacitors, where the desired output impedance is closely related to the output capacitor ESR. For designs with ceramic capacitors, the loop bandwidth required with conventional feedback control, is inversely proportional to the output capacitor size. Extending the bandwidth can result in cost and board area savings, since it can reduce the required number of capacitors. However, bandwidth in a feedback-controlled converter is limited by stability constraints linked to the switching frequency. In both current-mode and voltage-mode control, load current feedforward can extend the useful bandwidth beyond that achievable with pure feedback, since feedforward is not limited by stability constraints. The load

current feedforward is used to handle the bulk of the regulation action, while the feedback is used only to compensate for imperfections of the feedforward and to ensure tight DC regulation. The load current can be estimated from the inductor and capacitor voltages with simple RC networks. More sophisticated and robust estimation schemes, using the input current, for example, can be developed in the future. Different types of modulators can be used with the load feedforward scheme, as long as they have low latency with respect to unloading transients. The ability of estimated load current feedforward to provide tighter output impedance regulation than that with pure feedback control, was demonstrated with an experimental 12-to-1.3 V, all-ceramic capacitor VRM.

ACKNOWLEDGMENT

Thanks to Jianhui Zhang for laying out the controller PCB.

REFERENCES

[1] R. Redl, B. P. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter," in *Proc. IEEE Applied Power Electron. Conf.*, 1999, vol. 1, pp. 170–176.

[2] Kaiwei Yao, Ming Xu, Yu Meng, and F. C. Lee, "Design considerations for VRM transient response based on the output impedance," *IEEE Trans. on Power Electron.*, vol. 18, no. 6, pp. 1270–1277, Nov. 2003.

[3] A. V. Peterchev, Jinwen Xiao, and S. R. Sanders, "Architecture and IC implementation of a digital VRM controller," *IEEE Trans. on Power Electron.*, vol. 18, no. 1, pp. 356–364, Jan. 2003.

[4] Xin Zhang, Gary Yao, and Alex Q. Huang, "A novel VRM control with direct load current feedback," in *Proc. IEEE Applied Power Electron. Conf.*, 2004.

[5] Intel Corp., "Voltage regulator–down (VRD) 10.0," [Online]. Available: http://www.intel.com/design/Pentium4/guides/25288501.pdf, April 2003.

[6] F. Kern, H. Koertzen, and D. Hiller, "Intel VRD processor voltage and current specifications," in *Intel Technology Symposium*, Sept. 2003.

[7] P.-L. Wong, F. C. Lee, P. Xu, and K. Yao, "Critical inductance in voltage regulator modules," *IEEE Trans. on Power Electron.*, vol. 17, no. 4, pp. 485–492, July 2002.

[8] S. Banerjee and G. C. Verghese (Editors), *Nonlinear Phenomena in Power Electronics: Attractors, Bifurcations, Chaos, and Nonlinear Control*, New York: IEEE Press, 2001.

[9] R. Redl and N. O. Sokal, "Near-optimum dynamic regulation of DC–DC converters using feed-forward of output current and input voltage with current-mode control," *IEEE Trans. on Power Electron.*, vol. PE-1, no. 3, pp. 181–192, July 1986.

[10] J.-J. E. Slotine and W. Li, *Applied Nonlinear Control*, New Jersey: Prentice-Hall, 1991.

[11] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Kluver Academic Publishers, second edition, 2001.

[12] International Rectifier Corp., "IR3081: XPHASE^{TM} VR 10.0 control IC," Data Sheet. [Online]. Available: http://www.irf.com/product-info/datasheets/data/ir3081.pdf, April 2003.

[13] P. Midya and K. Haddad, "Two sided latched pulse width modulation control," in *Proc. IEEE Power Electron. Spec. Conf.*, 2000, pp. 628–633.

[14] N. Rossetti and S. R. Sanders, "Valley design techniques outperform peak current mode approach for CPU supplies," *PCIM Power Electronic Systems*, July 2001.