Quantization Resolution and Limit Cycling in Digitally Controlled PWM Converters

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Abstract— **This paper discusses the presence of steady-state limit cycles in digitally controlled pulse-width modulation (PWM) converters, and suggests conditions on the control law and the quantization resolution for their elimination. It then introduces single-phase and multi-phase controlled digital dither as a means of increasing the effective resolution of digital PWM (DPWM) modules, allowing for the use of low resolution DPWM units in high regulation accuracy applications. Bounds on the number of bits of dither that can be used in a particular converter are derived.**

I. Introduction

DIGITAL controllers for pulse-width modulation (PWM) converters enjoy growing popularity due to their low power, immunity to analog component variations, ability to interface with digital systems and to implement sophisticated control schemes, and potentially faster design process. Their applications include microprocessor voltage regulation modules (VRM's), audio amplifiers, portable electronic devices, and others.

This paper discusses the presence of steady state oscillations (limit cycles) in digitally controlled PWM converters, as well as techniques for increasing the effective resolution of digital PWM (DPWM) modules. Section II gives an overview of the structure of digital PWM controllers. Section III describes limit cycles and presents conditions for their elimination. Section IV introduces controlled digital dither as a technique that effectively increases the resolution of the DPWM module, allowing for the use of low resolution DPWM modules in applications requiring high regulation accuracy, such as VRM's and audio amplifiers. The ability to use low resolution DPWM modules in these applications, without incurring limit cycles, can result in substantial power and silicon area savings.

II. Digital Controller Structure

A block diagram of a digitally controlled PWM converter is shown in Fig. 1. Controllers with similar structure have been discussed in a number of publications (e.g. [1], [2], [3], [4]). The controller consists of an Analog-to-Digital Converter (ADC) which digitizes the regulated quantity (typically the output voltage V_{out}), a DPWM module, and a discrete-time control law. A typical discrete-time PID control law has the form

$$\begin{aligned} D_c(k+1) &= K_p D_e(k) + K_d[D_e(k) - D_e(k-1)] + \\ &\quad + K_i D_i(k) + D_{ref}(k) \end{aligned} \tag{1}$$

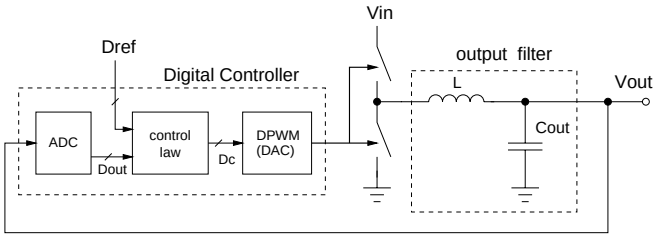


Fig. 1. Block diagram of a digitally controlled PWM converter.

where $D_c(k)$ is the duty cycle command at discrete time k, $D_e(k)$ is the error signal

$$D_e(k) = D_{ref}(k) - D_{out}(k),$$

and $D_i(k)$ is the state of an integrator

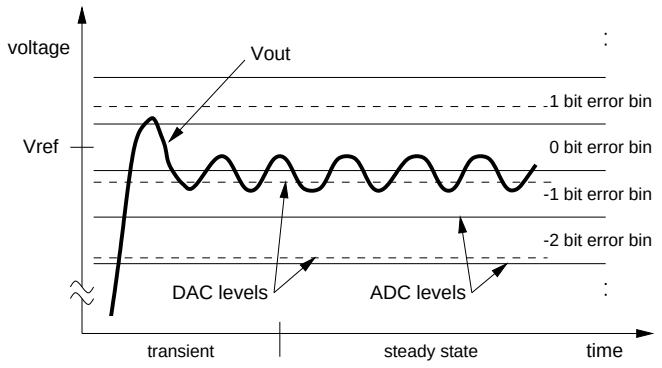
$$D_i(k) = D_i(k-1) + D_e(k).$$

Further, K_p is the proportional term constant, K_d is the derivative term constant, and K_i is the integral term constant. All variables are normalized to the input voltage, V_{in}; $D_{ref}(k)$ represents the reference voltage, and $D_{out}(k)$ is the digital representation of V_{out}. Variable D_{ref} is used as a feedforward term in (1). Note that D_{ref} by itself would give the correct duty cycle command for steady state operation with constant load, if there were no load-dependent voltage drop along the power train and no other non-idealities in the output stage [2].

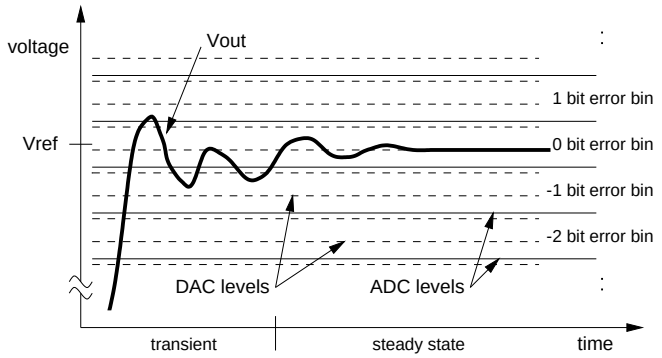
III. Limit Cycles

For the converter of Fig. 1, limit cycles refer to steady-state periodic oscillations of V_{out} that are not due to the PWM switching activity. Limit cycles may result from the presence of signal amplitude quantizers like the ADC and DPWM modules in the feedback loop. Steady-state limit cycling is undesirable, since its amplitude and frequency are hard to predict, and, consequently, it is difficult to analyze the resulting V_{out} noise and the electro-magnetic interference (EMI) produced by the converter.

Let us consider a system with ADC resolution of N_{adc} bits and DPWM resolution of N_{dpwm} bits. For a buck converter, this will correspond to voltage quantization of $\Delta V_{adc} = V_{in}/2^{N_{adc}}$ steps for the ADC, and $\Delta V_{dpwm} = V_{in}/2^{N_{dpwm}}$ for



(a)



(b)

Fig. 2. Qualitative behavior of V_{out} for: (a) DPWM resolution lower than the ADC resolution, and (b) DPWM resolution two times the ADC resolution and with integral term used in the control law.

the DPWM. Fig. 2(a) [1] shows the behavior of V_{out} in steady state when the DPWM resolution is less than the ADC resolution, and there is no DPWM level that maps into the ADC bin corresponding to the reference voltage V_{ref} (this ADC bin will be referred to as the *zero-error bin*). In steady state, the controller will be attempting to drive V_{out} to the zero-error bin, however due to the lack of a DPWM level there, it will alternate between the DPWM levels around the zero-error bin. This results in non-equilibrium behavior, such as steady-state limit cycling.

The first step towards eliminating limit cycles is to ensure that under all circumstances there is a DPWM level that maps into the zero-error bin. This can be guaranteed if the resolution of the DPWM module is finer than the resolution of the ADC. A one-bit difference in the resolutions, $N_{dpwm} = N_{adc} + 1$, seems sufficient in most applications since it provides two DPWM levels per one ADC level.

No Limit Cycle Condition # 1

$$\boldsymbol{resolution(DPWM) > resolution(ADC)}$$

[1] In all simulations the data is sampled at the switching frequency, therefore the switching ripple on V_{out} cannot be seen. For the discussions in this paper the switching ripple is not of interest and its omission makes the plots clearer.

Yet, even if the above condition is met, limit cycling may still occur if the feedforward term is not perfect and the control law has no integral term ($K_i = 0$). In this case, the controller relies on non-zero error signal D_e to drive V_{out} towards the zero-error bin. However, once V_{out} is in the zero-error bin, the error signal becomes zero, and V_{out} droops back into the -1 bit error bin. This sequence repeats over and over again, resulting in steady-state limit cycling. This problem can be solved by the inclusion of an integral term in the control law. After a transient, the integrator will gradually converge to a value that drives V_{out} into the zero-error bin, where it will remain as long as $D_e = 0$, since a digital integrator is perfect (Fig. 2(b)) .

No Limit Cycle Condition # 2

$$\boldsymbol{1 \geq K_i > 0}$$

An upper bound of unity is imposed on the integral term gain, since the digital integrator is intended to fine-tune the output voltage, therefore it has to be able to adjust the duty cycle command by steps as small as an LSB.

The two conditions suggested above are not sufficient for the elimination of steady-state limit cycles, since the non-linearity of the quantizers in the feedback loop may still cause limit cycling for high loop gains. Non-linear system analysis tools, such as describing functions ([5], [6], [3]), can be used to determine the maximum allowable loop gain not inducing limit cycles. The feedback loop of the converter includes two quantizers—the ADC and the DPWM—however in the present analysis we will consider only the ADC non-linearity, since it performs coarser quantization if the DPWM resolution is made higher than that of the ADC (as recommended above). The describing function of an ADC represents its effective gain as a function of the input signal amplitude and DC bias. When the control law contains an integral term, only limit cycles that have zero DC component can be stable, since the integrator drives the DC component of the error signal to the zero-error bin. Thus the describing function of a round-off quantizer with zero DC bias can be used to analyze the stability of the system. This describing function, $N(A)$, is plotted in Fig. 3, where A is the AC amplitude of the signal being quantized, and ΔV_{adc} is the quantization bin size corresponding to one LSB. From the plot it can be seen that the describing function has a maximum value of about 1.3, corresponding to maximum effective ADC gain. The control law can then be designed in the same way as for linear systems, provided the effective gain of the ADC is included in the loop gain calculations. Namely, to prevent limit cycles it has to be ensured that

No Limit Cycle Condition # 3

$$\boldsymbol{1 + N(A)L(j\omega) \neq 0}$$

holds for all non-zero finite signal amplitudes A and frequencies ω, where $L(j\omega)$ is the loop transmission from the output of the ADC to its input.

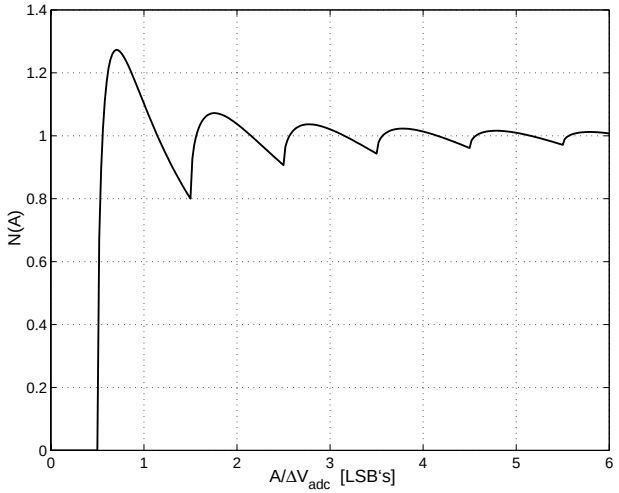


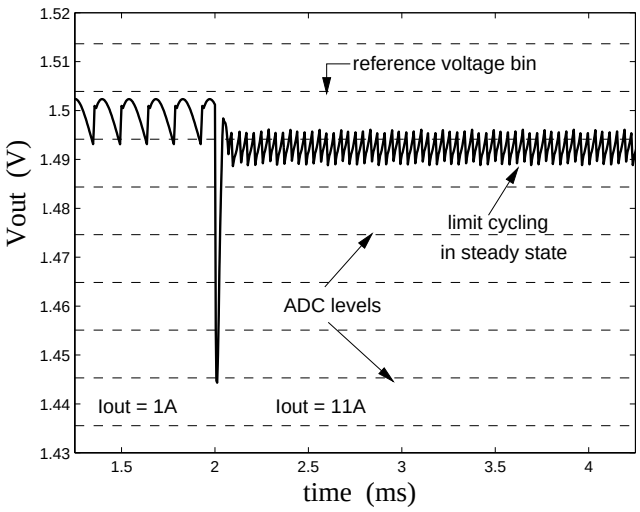
Fig. 3. The describing function of a round-off quantizer with zero DC bias.

Fig. 4(a) shows a simulation of the transient response of a digitally controlled PWM converter. The resolution of the DPWM module, $N_{dpwm} = 10$ bits, is higher than the resolution of the ADC, $N_{adc} = 9$ bits, however steady-state limit cycling is observed both before and after the load current step, since no integral term was used in the control law. On the other hand, in Fig. 4(b) an integral term is added to the control law, and the steady-state limit cycling is eliminated.

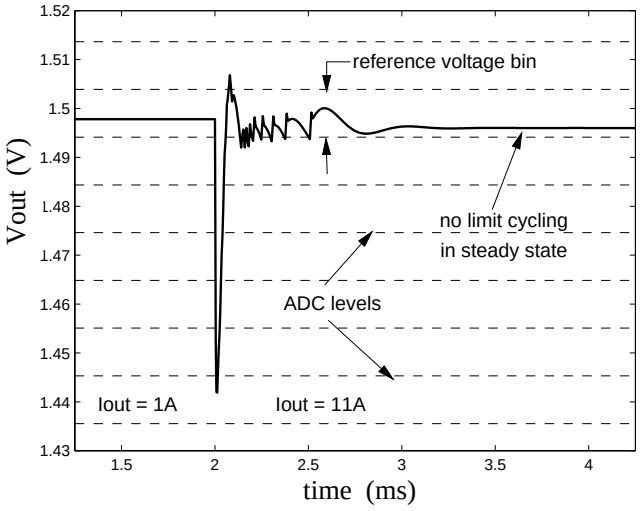
IV. Controlled Dither

The precision with which a digital controller regulates V_{out} is determined by the resolution of the ADC. In particular, V_{out} can be regulated with a tolerance of one LSB of the ADC. Many present-day applications, such as microprocessor VRM's, demand regulation precision at the order of tens of millivolts [7], requiring ADCs and DPWM modules with very high resolution. For example, regulation resolution of 10mV at $V_{in} = 5$V corresponds to ADC resolution of $N_{adc} = \log_2(5V/10mV) = 9$ bits, implying DPWM resolution of at least $N_{dpwm} = 10$ bits to avoid steady-state limit-cycling. For a converter switching frequency of $f_{sw} = 1$MHz, such resolution would require a $2^{10} \cdot f_{sw} = 1$GHz fast clock in a counter-comparator implementation of the DPWM module, or $2^{10} = 1024$ stages in a ring oscillator implementation, resulting in high power dissipation or large area ([8], [3], [4]). Thus, it is beneficial to look for ways to use low-resolution DPWM modules to achieve the desired high V_{out} resolution.

One method which can increase the effective resolution of a DPWM module is dithering. It amounts to adding high-frequency periodic or random signals to a certain quantized signal, which is later filtered to produce averaged DC levels with increased resolution. Analog dither has been used to increase the effective resolution of a DPWM module [9], however in this case an analog controller was used. Analog dither



(a)



(b)

Fig. 4. Simulation of a DPWM converter output voltage under a load current transient. $V_{in} = 5$V, $V_{ref} = 1.5$V, $f_{sw} = 250$kHz, $N_{adc} = 9$ bits, and $N_{dpwm} = 10$ bits. In (a) no integral term was included in the control law, while in (b) an integral term was added.

is difficult to generate and control, it is sensitive to analog component variations, and it can be mixed only with analog signals in the converter, and not with signals inside a digital controller. On the other hand, a digital dither generated inside the controller is simpler to implement and control, it is insensitive to analog component variations, and it can offer more flexibility. Therefore, the use of digital dither to improve the resolution of DPWM modules is discussed in the present section.

A. Single-phase Dither

The idea behind controlled digital dither is to vary the duty cycle by an LSB over a few switching periods, so that the *av-*

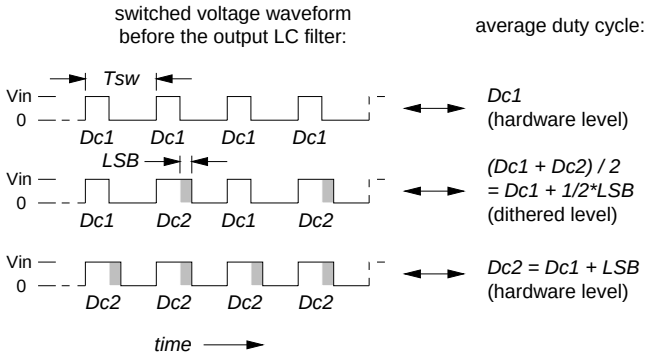


Fig. 5. Use of duty cycle dither to realize a $\frac{1}{2}LSB$ DPWM level (1-bit dither).

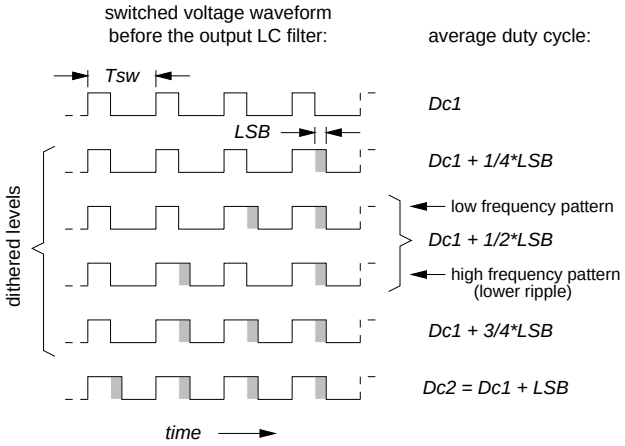


Fig. 6. Duty cycle dither patterns realizing $\frac{1}{4}LSB$, $\frac{1}{2}LSB$, and $\frac{3}{4}LSB$ DPWM levels (2-bit dither).

erage duty cycle has a value *between* two adjacent quantized duty cycle levels. The averaging action is implemented by the output LC filter. The dither concept is illustrated in Fig. 5. Let D_{c1} and D_{c2} correspond to two adjacent quantized duty cycle levels put out by the DPWM module, $D_{c2} = D_{c1} + LSB$. If the DPWM module is made to alternate between D_{c1} and D_{c2} every next switching period, the average duty cycle over time will equal $(D_{c1} + D_{c2})/2 = D_{c1} + \frac{1}{2}LSB$. Thus, an intermediate $\frac{1}{2}LSB$ level can be implemented between every two adjacent duty cycle levels, resulting in an increase of the effective DPWM resolution of one bit. From Fig. 5 it can be seen that to produce this intermediate $\frac{1}{2}LSB$ level, *two* subsequent switching periods are necessary (putting out D_{c1} and D_{c2}, respectively). Using the same reasoning, the implementation of $\frac{1}{4}LSB$ and $\frac{3}{4}LSB$ levels can be envisioned (Fig. 6): If D_{c1} is put out in three subsequent switching periods, followed by one period of D_{c2}, the average duty cycle value will be $D_{c1} + \frac{1}{4}LSB$. Analogously, if one period of D_{c1} is followed by three periods of D_{c2}, the average duty cycle value will be $D_{c1} + \frac{3}{4}LSB$. Clearly, the feasibility of $\frac{1}{4}LSB$ steps adds yet one more bit of effective resolution to the DPWM. In this case, the dither patterns associated with the $\frac{1}{4}LSB$ and $\frac{3}{4}LSB$ levels span *four* switching periods. Finally, it can be seen that using the dither approach, any sub-bit duty cycle level can be achieved. To increase the effective DPWM resolution ($N_{dpwm,eff}$) by M bits, dither patterns spanning 2^M switching periods are necessary:

$$N_{dpwm,eff} = N_{dpwm} + M \tag{2}$$

where N_{dpwm} is the number of bits of hardware DPWM resolution.

B. Dither Ripple

Of course, the effective increase in DPWM resolution by dithering does not come for free. The dithering of the duty cycle creates an additional AC ripple at the output of the *LC* filter, which is superimposed on the ripple from the converter switching action. In the above discussion it was shown that the longer the dither patterns used, the larger the effective resolution. However, longer dither patterns can cause higher output AC ripple, since they contain lower frequency components, and the *LC* filter has less attenuation at lower frequencies. For example, the dither pattern implementing the $\frac{1}{2}LSB$ duty cycle level has a fundamental frequency component at $f_{sw}/2$, while for the $\frac{1}{4}LSB$ level it is at $f_{sw}/4$. Assuming a second order filter rolloff of 12 dB/oct, the attenuation of the $\frac{1}{4}LSB$ level fundamental frequency is four times less than the attenuation of the $\frac{1}{2}LSB$ level ripple. This consideration puts a practical limit on the number of bits of dithering that can be added to increase the resolution of the DPWM module.

Some simple mathematical analysis (see the Appendix) can give an estimate of the AC ripple added to the output voltage as a result of the dither:

$$v_{r,dith} \leq \left(\frac{f_c}{f_{sw}}\right)^2 \cdot 2^{2M} \cdot \frac{4}{\pi}\frac{V_{in}}{2^{N_{dpwm}}} \tag{3}$$

for $f_c < f_{dith} < f_z$, and

$$v_{r,dith} \leq \frac{{f_c}^2}{f_z f_{sw}} \cdot 2^M \cdot \frac{4}{\pi}\frac{V_{in}}{2^{N_{dpwm}}} \tag{4}$$

for $f_c < f_z < f_{dith}$, where $v_{r,dith}$ is the peak-to-peak dither ripple, f_{dith} is the fundamental frequency of the dither,

$$f_{dith} = \frac{f_{sw}}{2^M}, \tag{5}$$

f_c is the LC filter cutoff frequency, and f_z is the ESR zero frequency.

Once the amplitude of the dither is known, a condition on how many bits of dither, M, can be used in a certain system can be developed (see the Appendix):

$$M < \frac{1}{3}\log_2\left[\frac{\pi}{4}\left(\frac{f_{sw}}{f_c}\right)^2 (2^{\Delta N} - 1)\right] \tag{6}$$

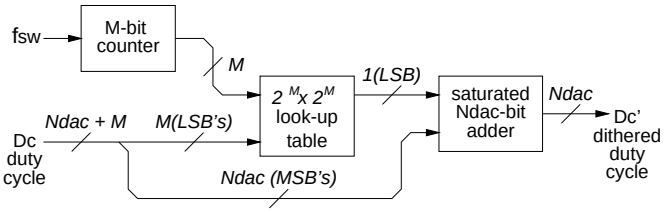


Fig. 7. Structure for adding arbitrary dither patterns to the duty cycle.

for $f_c < f_{dith} < f_z$, and

$$M < \frac{1}{2}\log_2\left[\frac{\pi}{4}\frac{f_z f_{sw}}{{f_c}^2}(2^{\Delta N}-1)\right] \quad (7)$$

for $f_c < f_z < f_{dith}$, where

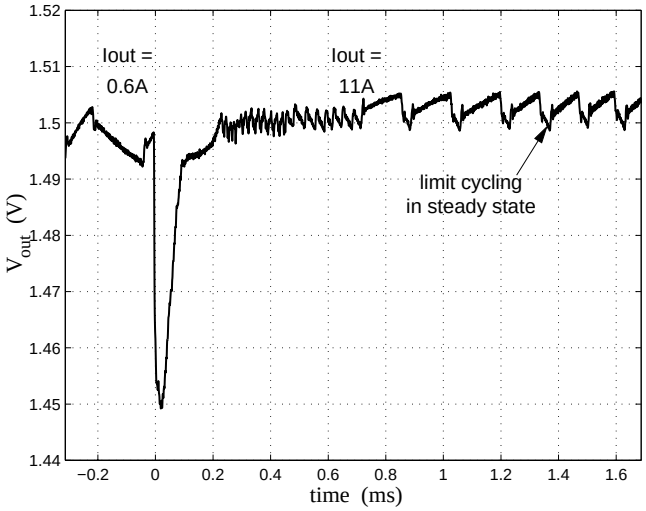
$$\Delta N = N_{dpwm,eff} - N_{adc} = (N_{dpwm} + M) - N_{adc} \quad (8)$$

is the difference between the effective resolutions of the DPWM and the ADC (in bits). For example, in Section III it was suggested that making the resolution of the DPWM one bit higher then that of the ADC adequately satisfies the condition to eliminate steady-state limit cycling, hence $\Delta N = 1$. The above equations can be used by starting with a guess for M, obtaining the corresponding dither frequency from (5), and then using (6) or (7), respectively, to obtain a bound on M. If the result is not consistent with the initial guess for M, the procedure should be repeated with a reduced value of M. On the other hand, if the inequalities are satisfied, the value of M can be increased, and the procedure can be repeated.

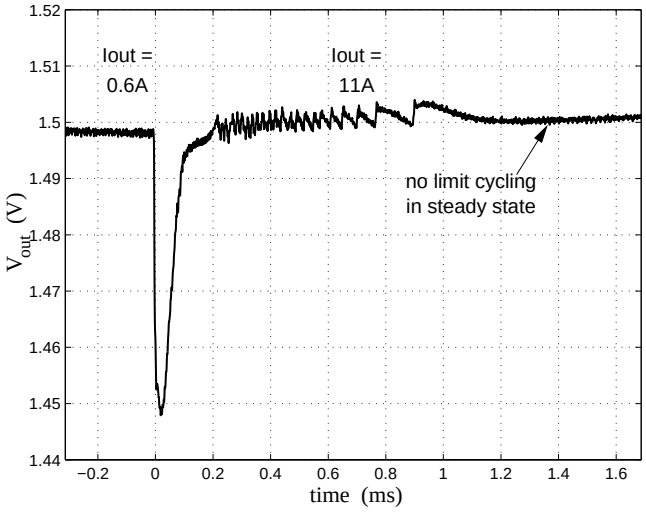
As it was established above, if a 2-bit dither is used, the dither patterns should span $2^2 = 4$ switching periods. While there are unique duty cycle sequences implementing the $\frac{1}{4}LSB$ and $\frac{3}{4}LSB$ levels, the $\frac{1}{2}LSB$ level can be implemented with two different sequences: $D_{c1}, D_{c1}, D_{c2}, D_{c2}$ or $D_{c1}, D_{c2}, D_{c1}, D_{c2}$ (see Fig. 6). Both sequences produce the same DC time average, however the former has fundamental frequency component at $f_{sw}/4$, while the latter—at $f_{sw}/2$. Thus the $D_{c1}, D_{c2}, D_{c1}, D_{c2}$ sequence will produce much less ripple. For a particular sub-bit level it is advantageous to use dither patterns that minimize the output voltage ripple, which implies patterns with higher frequency components. If this rule is followed, (3) and (4) give an overestimate, while (6) and (7) yield an underestimate.

C. Dither Generation Scheme

A dither generation scheme that can produce dither patterns of *any* shape, is presented in Fig. 7. A look-up table stores 2^M dither sequences, each 2^M bits long, corresponding to the sub-bit levels implemented with M-bit dither. The M LSBs of the duty cycle command D_c select the dither pattern corresponding to the appropriate sub-bit level, while the M-bit counter sweeps through the bits of this particular dither pattern. The dither pattern is then added to the N MSBs of D_c to produce the duty cycle command D_c' which is sent to the hardware DPWM module.



(a)



(b)

Fig. 8. Experimental 4-phase buck converter transient response under a load current step. $V_{in} = 5$V, $V_{ref} = 1.5$V, $f_{sw} = 250$kHz, $N_{adc} = 9$ bits, and (a) N_{dpwm} = 7 bits, (b) $N_{dpwm,eff}$ = 7 bits + 3-bit dither = 10 bits.

D. Experimental Results

The digital dither technique was tested on a prototype 4-phase buck converter with results confirming the theoretical expectations. In the prototype, the ADC had 9-bit resolution and the DPWM had 7 bits of hardware resolution. The transient response of the converter due to a load current step is shown in Fig. 8(a). The system exhibits steady-state limit cycling since

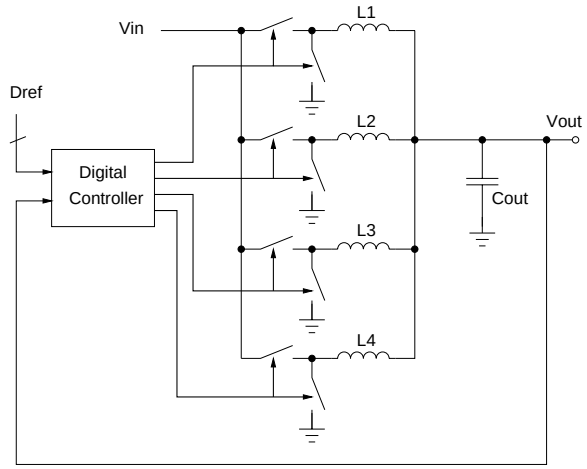


Fig. 9. Block diagram of a 4-phase buck converter.

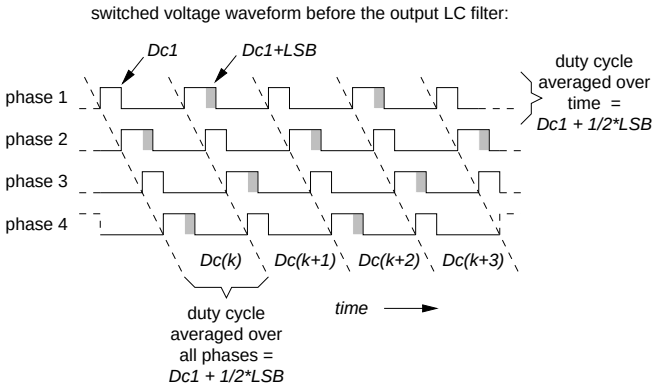


Fig. 10. 4-phase dither patterns implementing a $\frac{1}{2}LSB$ DPWM level.

the condition $resolution(DPWM) > resolution(ADC)$ is not met. Subsequently 3-bit digital dither was introduced, increasing the effective resolution of the DPWM module to 7 + 3 = 10 bits. The step response of the modified system is shown in Fig. 8(b). The effective resolution of the DPWM is now higher than that of the ADC, and steady state limit cycles are eliminated. It should be noted that in this case the steady state ripple is only due to the multi-phase switching and the dither, and it does not exceed a few millivolts. This example illustrates the effectiveness of the controlled dither concept.

E. Multi-phase Dither

The concept of controlled dither can be extended to multi-phase (interleaved) VRM's. In a multi-phase converter, multiple single-phase power trains are connected to a common output capacitor and switched with the same duty cycle, but out of phase, which decreases the ripple in the output voltage and input current. For example, the block diagram of a 4-phase buck converter is shown in Fig. 9. In this case, the four power train legs are switched $360°/4 = 90°$ out of phase.

The controlled dither technique developed for single phase converters can be applied directly to the multi-phase case. For example, to achieve a $D_{c1} + \frac{1}{2}LSB$ level, duty cycle D_{c1} is applied to *all* phase for one switching period, followed by $D_{c2} = D_{c1} + LSB$ applied to all phases, and so on. However, in a multi-phase converter we can exploit the additional degrees of freedom associated with the independent switching of the different phases to further reduce the dither ripple, and thus allow more bits of dither, and respectively less bits of hardware resolution.

Consider again the case of a $D_{c1} + \frac{1}{2}LSB$ level. This level can be implemented by commanding, in the same switching period, D_{c1} to two of the phases and D_{c2} to the other two, so that the *average duty cycle over all phases* is $D_{c1} + \frac{1}{2}LSB$ for that period. The next switching period the duty cycle commands are toggled, so that the average over all phases is still $D_{c1} + \frac{1}{2}LSB$, however the *average over time* for each phase is $D_{c1} + \frac{1}{2}LSB$ as well (Fig. 10). The equal averaging over time for each phase is necessary to avoid DC current mismatch among the phases. This approach can be extended for other sub-bit levels, like $D_{c1} + \frac{1}{4}LSB$, noting that for a multi-phase converter with N_ϕ phases, $log_2 N_\phi$ bits of dither can be implemented by averaging over the phases. The advantage of this "multi-phase dither" technique is that the resulting output ripple is smaller, since for any switching period the average duty cycle over all phases is the same. As a result of the ripple reduction, approximately $log_2 N_\phi$ more bits of DPWM resolution can be implemented with dither.

V. Conclusion

This paper discussed the presence of steady-state limit cycles in digitally controlled PWM converters, and suggested conditions on the control law, and the ADC and DPWM resolutions for their elimination. It then introduced single-phase and multi-phase controlled digital dither as a means of increasing the effective resolution of DPWM modules, allowing for the use of low resolution DPWM units in high regulation accuracy applications. Bounds on the number of bits of dither that can be used in a particular converter were derived.

Appendix
Dither Ripple Calculations

Since the dither constitutes switching between two adjacent quantized duty cycle levels, it can be modeled as a square wave with peak-to-peak amplitude of one hardware LSB of the DPWM module equal to $V_{in}/2^{N_{dpwm}}$. For M-bit dither, the dither waveform with the largest low frequency component is a square wave with 50% duty ratio at frequency

$$f_{dith} = \frac{f_{sw}}{2^M}. \quad (9)$$

This waveform can be used to study the worst case dither ripple. Since the dither is smoothed by the converter output LC

filter, it is sufficient to consider only its fundamental frequency component, which is a sine wave with frequency f_{dith} and peak-to-peak amplitude

$$A_{p-p,dith} = \frac{4}{\pi} \cdot \frac{V_{in}}{2^{N_{dpwm}}}. \quad (10)$$

The peak-to-peak output voltage ripple can then be bounded approximately as

$$v_{r,dith} \leq H(f_{dith}) \cdot A_{p-p,dith} \quad (11)$$

where $H(f_{dith})$ is the attenuation of the output LC filter at frequency f_{dith}.

The LC filter has a cutoff frequency at $f_c = 1/2\pi\sqrt{L_o C_o}$ after which it rolls off at -40 dB/dec. Real capacitors have finite effective series resistance (r_{ESR}) which causes a zero in the filter characteristic at frequency $f_z = 1/2\pi r_{ESR} C_o$, changing the rolloff to -20 dB/dec. Thus,

$$H(f) \approx \left(\frac{f_c}{f}\right)^2 \quad \text{for} \quad f_c < f < f_z, \quad (12)$$

and

$$H(f) \approx \left(\frac{f_c}{f_z}\right)^2 \cdot \frac{f_z}{f} = \frac{{f_c}^2}{f_z \cdot f} \quad \text{for} \quad f_c < f_z < f. \quad (13)$$

Substituting back in (11), we obtain upper bounds for the peak-to-peak output voltage ripple due to dither:

$$v_{r,dith} \leq \left(\frac{f_c}{f_{sw}}\right)^2 \cdot 2^{2M} \cdot \frac{4}{\pi} \frac{V_{in}}{2^{N_{dpwm}}} \quad (14)$$

for $f_c < f_{dith} < f_z$, and

$$v_{r,dith} \leq \frac{{f_c}^2}{f_z f_{sw}} \cdot 2^M \cdot \frac{4}{\pi} \frac{V_{in}}{2^{N_{dpwm}}} \quad (15)$$

for $f_c < f_z < f_{dith}$.

Once the amplitude of the dither is known, a condition on how many bits of dither, M, can be used in a certain system can be developed. To ensure that the dither does not cause steady-state limit cycling, there should always be an effective DPWM level that completely fits into one ADC quantization bin, taking into account the dither ripple. With M-bit dither, the effective DPWM quantization bin size is

$$\Delta V_{dpwm,eff} = V_{in}/2^{N_{dpwm,eff}} = V_{in}/2^{N_{dpwm}+M}. \quad (16)$$

Geometric considerations show that the case which allows for the smallest dither ripple amplitude is when the effective DPWM levels are located at one-half effective DPWM bin size from the center of the ADC bin. Then the tolerable peak-to-peak dither ripple amplitude is bounded by

$$\begin{aligned} v_{r,dith} &< 2\left(\frac{1}{2}\Delta V_{adc} - \frac{1}{2}\Delta V_{dpwm,eff}\right) \\ &= \Delta V_{adc} - \Delta V_{dpwm,eff}. \end{aligned} \quad (17)$$

Assuming that the ADC has resolution ΔN bits coarser than the effective resolution of the DPWM module,

$$N_{adc} = N_{dpwm,eff} - \Delta N = N_{dpwm} + M - \Delta N, \quad (18)$$

the ADC bin size is

$$\Delta V_{adc} = V_{in}/2^{N_{adc}} = V_{in}/2^{N_{dpwm}+M-\Delta N}. \quad (19)$$

Substituting (16) and (19) in (17), we obtain

$$v_{r,dith} < V_{in} \cdot \frac{2^{\Delta N} - 1}{2^{N_{dpwm}+M}}. \quad (20)$$

Combining (20) with (14) and (15) we obtain an upper bound on M:

$$M < \frac{1}{3}\log_2\left[\frac{\pi}{4}\left(\frac{f_{sw}}{f_c}\right)^2 (2^{\Delta N} - 1)\right] \quad (21)$$

for $f_c < f_{dith} < f_z$, and

$$M < \frac{1}{2}\log_2\left[\frac{\pi}{4}\frac{f_z f_{sw}}{{f_c}^2}(2^{\Delta N} - 1)\right] \quad (22)$$

for $f_c < f_z < f_{dith}$.

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