Digital Loss-Minimizing Multi-Mode Synchronous Buck Converter Control

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***Abstract*— A multi-mode control strategy for a synchronous buck converter operating over a wide load range, is presented. For heavy loads, the converter runs in fixed-frequency continuous conduction mode (CCM). At light loads, it enters discontinuous conduction mode (DCM) with synchronous rectification. At still lighter loads, synchronous rectification is disabled in DCM. At very light loads, the converter operates in variable-frequency pulse skipping mode. The synchronous rectifier (SR) timing is scheduled as a function of the load current, enabling appropriate transition among the modes. An on-line adaptive algorithm to optimize the SR timing, based on power loss minimization, is presented. This control strategy is particularly well suited for a digital controller implementation, since it uses sophisticated computations, while not requiring high analog-to-digital conversion rates.**

I. Introduction

Under different load conditions a synchronous fixed-frequency PWM buck converter (Fig. 1) has different optimal gating patterns for the switches. For large load currents the converter runs in continuous conduction mode (CCM). In CCM, the control switch M_1 has an approximately constant on-time determined by the conversion ratio. The synchronous rectifier (SR) M_2 has a complementary switching pattern with deadtimes $t_{d,on}$ and $t_{d,off}$ to prevent short-circuit losses, while not allowing the body diode of M_2 to turn on and contribute conduction and recovery losses [1]–[3]. At light load, the converter runs in discontinuous conduction mode (DCM), if the inductor current is not allowed to go negative. In DCM, under constant switching frequency, the control switch on-time varies proportionally to the square root of the load current, and so does the optimal SR on-time: the SR is on while the inductor discharges, and turns off when the inductor current reaches zero. For evenlighter loads, it is beneficial to not turn on the SR at all, since the power used to switch the SR outweighs the corresponding decrease of conduction loss. Further, since switching losses dominate at no load or very light load conditions, it is advantageous to impose a minimum pulse width on the control switch, forcing the converter to skip pulses, thus reducing the switching losses. In modern portable applications, minimizing power loss at light load or standby is of paramount importance, hence appropriate SR timing and mode switching is crucial.

Existing methods for SR control in buck converters rely on high-bandwidth sensing of some combination of gate and drain voltages of the switch MOSFET's, using these signals to adjust the SR timing in order to emulate an ideal diode [1]–[3]. We present an alternative approach based on directly controlling (scheduling) the SR timing as a function of load current. The input current can be used instead of the load current, and other parameters, such as the input voltage, can be added as scheduling variables. The function relating the optimal SR gating to the load current can be determined off-line and programmed in the controller, or can be obtained on-line by dynamically minimizing the converter power loss via multi-parameter extremum seeking [4]–[6]. This method requires only coarse sampling of the scheduling variable (e.g., the output current) at a rate equal to the switching frequency, and low-bandwidth sensing of a single quantity characterizing the converter performance (e.g., power loss, input current, or temperature). This method is particularly well-suited for a digital controller implementation [7], since it uses low rate computations and data storage, thus not requiring analog-to-digital sampling rates beyond the converter switching frequency, which is typically in the range of hundreds of kHz.

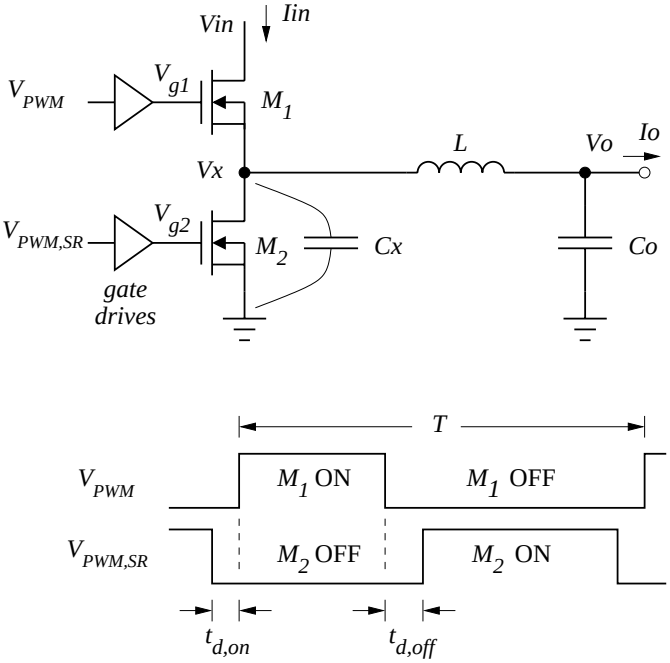


Fig. 1. Buck converter with synchronous rectification, and the corresponding MOSFET control signals.

II. Multi-Mode Buck Control

To ensure high efficiency over a wide load range, the buck converter can be operated in four different modes depending on the load current. These modes, together with the associated control switch and SR timing, are shown in Fig. 2, and are described below:

I. Fixed-frequency CCM with SR

At heavy loads, the converter operates in CCM with fixed switching period T. The control switch on-time is $T_{on} = MT$,

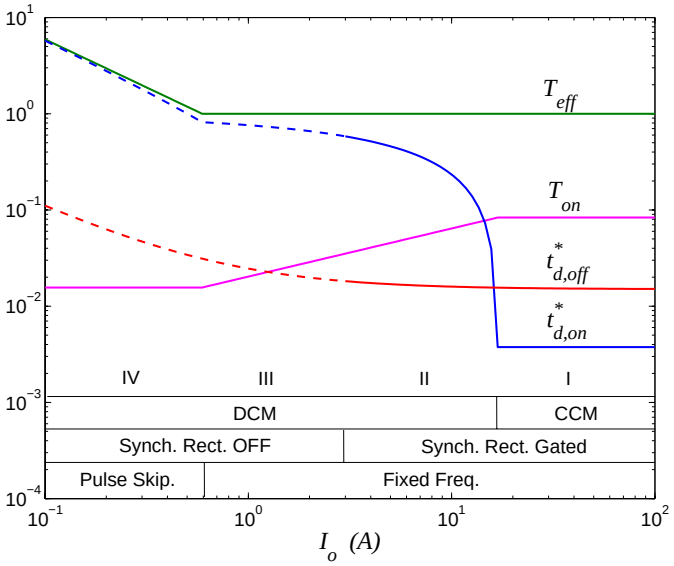


Fig. 2. Timing of control switch and synchronous rectifier of buck converter for different modes. All parameters are normalized by fixed-frequency switching period T, and both axes are logarithmic.

where $M = V_o/V_{in}$ is the conversion ratio, and V_{in} and V_o are the input and output voltages, respectively. The optimal turn-off deadtime $t^*_{d,off}$ depends on the intrinsic turn-off delay $t_{d,off0}$ of the control switch M_1, and the time it takes to discharge the switching node capacitance C_x,

$$t^*_{d,off} = \frac{V_{in}C_x}{I_o} + t_{d,off0}, \tag{1}$$

where I_o is the load current. Further, the optimal turn-on deadtime $t^*_{d,on}$ is a small constant $t_{d,on0}$, preventing conduction overlap between the control switch and the SR.

II. Fixed-frequency DCM with SR

At lighter loads, the converter enters DCM if the SR is gated so that it does not allow negative inductor currents. This happens for load currents

$$I_o < \frac{V_{in}TM(1-M)}{2L}, \tag{2}$$

where L is the total inductance (all inductors in parallel in a multi-phase converter). The duty ratio now depends on the load current,

$$D = \sqrt{\frac{2LI_oM}{V_{in}T(1-M)}}. \tag{3}$$

The optimal turn-off deadtime still follows (1). The optimal $t_{d,on}$, on the other hand, varies substantially as a function of the load current,

$$t^*_{d,on} = T - \sqrt{\frac{2LI_oT}{V_{in}M(1-M)}} + t_{d,on0}. \tag{4}$$

In DCM, this parameter corresponds to the time the inductor current is zero.

III. Fixed-frequency DCM without SR

Below some current level, the switching losses contributed by the SR gate drives exceed the conduction loss decrease contributed by the SR, thus it is beneficial to turn off the SR altogether.

IV. Variable-frequency Pulse Skipping without SR

Finally, at very light loads, the converter loss is dominated by gate drive losses which are proportional to the switching frequency. Thus, it is advantageous to allow variable frequency operation at very light loads. This can be implemented in a straightforward way with a digital controller, by limiting the minimum duty ratio to a value D_{min}. The duty ratio limit results in pulse-skipping behavior, effectively varying the switching frequency. The converter is in pulse skipping for

$$I_o < \frac{D^2_{min}V_{in}T(1-M)}{2LM}, \tag{5}$$

with the switching period following approximately

$$T_{eff} \approx \frac{V_{in}T^2_{on}(1-M)}{2LI_oM}. \tag{6}$$

The pulse width T_{on} is constant in steady state, and is equal to the sum of the proportional and derivative terms in the digital PID control law. The pulse is generated when the error signal crosses between the zero and minus-one error bins[1], resulting in a well defined pulse-skipping behavior, which is specific to digital controllers.

The mode transitions described above are straightforward to implement with a digital controller. The SR scheduling requires only coarse sampling of the output (or input) current at the converter switching rate, and ensures appropriate transition between CCM and DCM. The transition to pulse skipping is automatic, given that a minimum duty ratio is imposed. Importantly, the PID control law does not need to be modified for the different modes, resulting in a simple controller structure. Finally, since this approach determines the SR timing directly from the load current data, it allows for fast on-line adjustment of the SR gating for each switching period. This feature is very important in applications such as modern microprocessor supplies, where the load current can change with a high frequency and slew rate.

III. Loss-Minimizing Adaptation

The method proposed above calls for scheduling of the SR timing parameters as a function of the load current. The functions $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$ can be derived from theoretical equations, such as (4) and (1), and programmed into a look-up table. However, this approach does not take into account component tolerances and slow parameter variation with time and temperature. Alternatively, the optimal $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$ can be obtained from off-line power loss measurements, however, this approach cannot capture parameter variations either, and requires an off-line testing and burn-in setup. In this section we present an algorithm which resolves these issues by determining the optimal SR scheduling on-line, and adaptively adjusting the timing functions, tracking circuit parameter variations.

The objective is to adjust the SR timing parameters $t_{d,on}$ and $t_{d,off}$ so as to minimize the converter power loss P_{loss} for

[1]See [8] for definitions and a discussion of quantization phenomena in digitally controlled PWM converters.

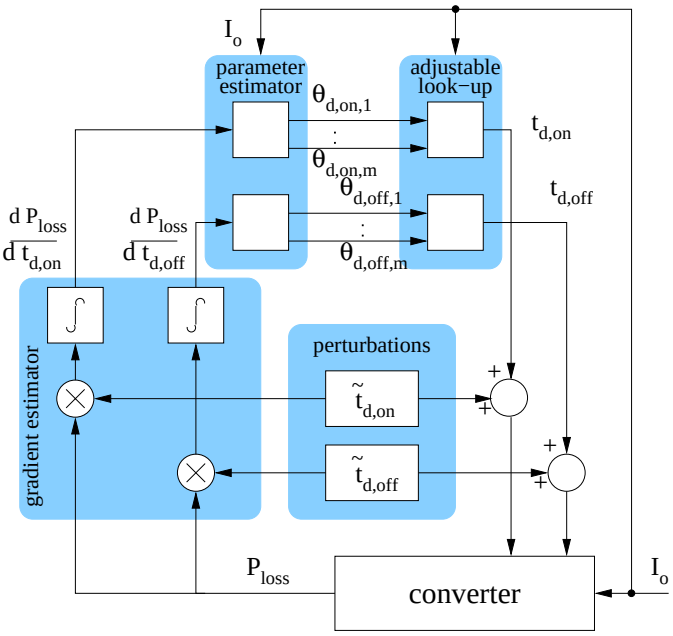


Fig. 3. Block diagram of the synchronous rectifier control using multi-parameter extremum seeking.

each load current value. The algorithm is identical for $t_{d,on}$ and $t_{d,off}$, and therefore, we will present it for a general variable t_d. We parametrize each of the deadtime functions

$$t_d = t_d(I_o, \mathbf{\Theta}) \tag{7}$$

with parameter vector $\mathbf{\Theta} = [\theta_1, \cdots, \theta_m]$. In this work we use a piecewise linear function to implement (7), where θ_l is the l-th vertex of the function (Fig. 4). The vertices are positioned at every $\Delta I_{o,lin}$ increment of I_o. The value of t_d is obtained by interpolation from the two nearest vertices,

$$t_d(I_o, \mathbf{\Theta}) = (1-\alpha)\theta_l + \alpha\theta_{l+1}. \tag{8}$$

The vertex index, l, is the integer part of $I_o/\Delta I_{o,lin}$,

$$l = \lfloor I_o/\Delta I_{o,lin} \rfloor, \tag{9}$$

and α is the fractional distance of I_o to the l-th vertex,

$$\alpha = I_o/\Delta I_{o,lin} - \lfloor I_o/\Delta I_{o,lin} \rfloor, \tag{10}$$

where $\lfloor x \rfloor$ is the floor function giving the greatest integer less than or equal to x. The increment size $\Delta I_{o,lin}$ can be constant or can depend on I_o to suit a particular shape of the fitted function. In the latter case the indexing in (9) and (10) should be adjusted appropriately. Other parameterization approaches can be used, such as realizing (7) with a smooth function, and adjusting its parameters (e.g., a polynomial with tunable coefficients).

To determine the optimal value of the parameter vector, a perturbation-based extremum seeking algorithm is used (see [4]–[6] and the references therein). The controller introduces small, zero-mean perturbations $\tilde{t}_d$ in t_d, resulting in modulation of the converter power loss.[2] The power loss gradient with respect to the SR gating edges is determined by integrating the product of the power loss and the perturbation signal. Based on this gradient, the parameter vector is adjusted in a direction which decreases the power loss. In this implementation, at each iteration we adjust the two vertices of (8) which bracket the load current,

$$\begin{aligned} \theta_l[k+1] &= \theta_l[k] + (1-\alpha[k])\, a\, P_{loss}[k]\, \tilde{t}_d[k], \\ \theta_{l+1}[k+1] &= \theta_{l+1}[k] + \alpha[k]\, a\, P_{loss}[k]\, \tilde{t}_d[k], \\ \theta_{l'}[k+1] &= \theta_{l'}[k], \qquad \text{for} \qquad l' \neq l, l+1, \end{aligned} \tag{11}$$

where a is a gain determining the speed of parameter adaptation. Note that the adjustment to the two vertices is weighted differently, via parameter α, according to the vertex distance from I_o. The two perturbation signals $\tilde{t}_{d,on}$ and $\tilde{t}_{d,off}$ are chosen to be zero-mean and mutually orthogonal to allow independent estimation of $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$, respectively. The perturbation signals can be sine or square waves at two different frequencies, for example. Importantly, this algorithm does not need to run fast, since it computes optimal curves for $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$, thus requiring only identification of the constant or slowly varying parameters describing these functions, and not the rapidly changing parameters $t_{d,on}$ and $t_{d,off}$ themselves.

In the adaptation problem discussed above there are four time scales: the converter dynamics, the load current dynamics, the perturbation frequencies, and the parameter estimator time constant. To ensure parameter covergence to a small neighborhood of their optimal values, the system has to be designed so that the parameter estimator is slower than the perturbation signals, which should be slow compared to the converter dynamics [6]. In some applications, such as microprocessor supplies, the load current can vary at speeds comparable to the converter dynamics. This variation tends to be rejected by the adaptive algorithm since it is not correlated with the perturbation signals. Finally, it may be useful to normalize the power loss by the load current for the gradient calculation, or to include a blanking scheme, to ensure satisfactory parameter convergence in the presence of large load transients.

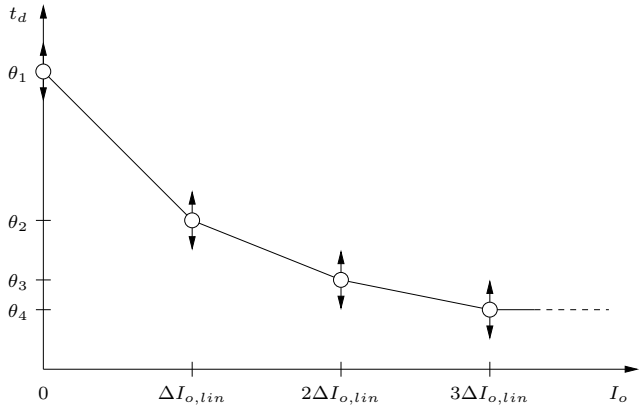
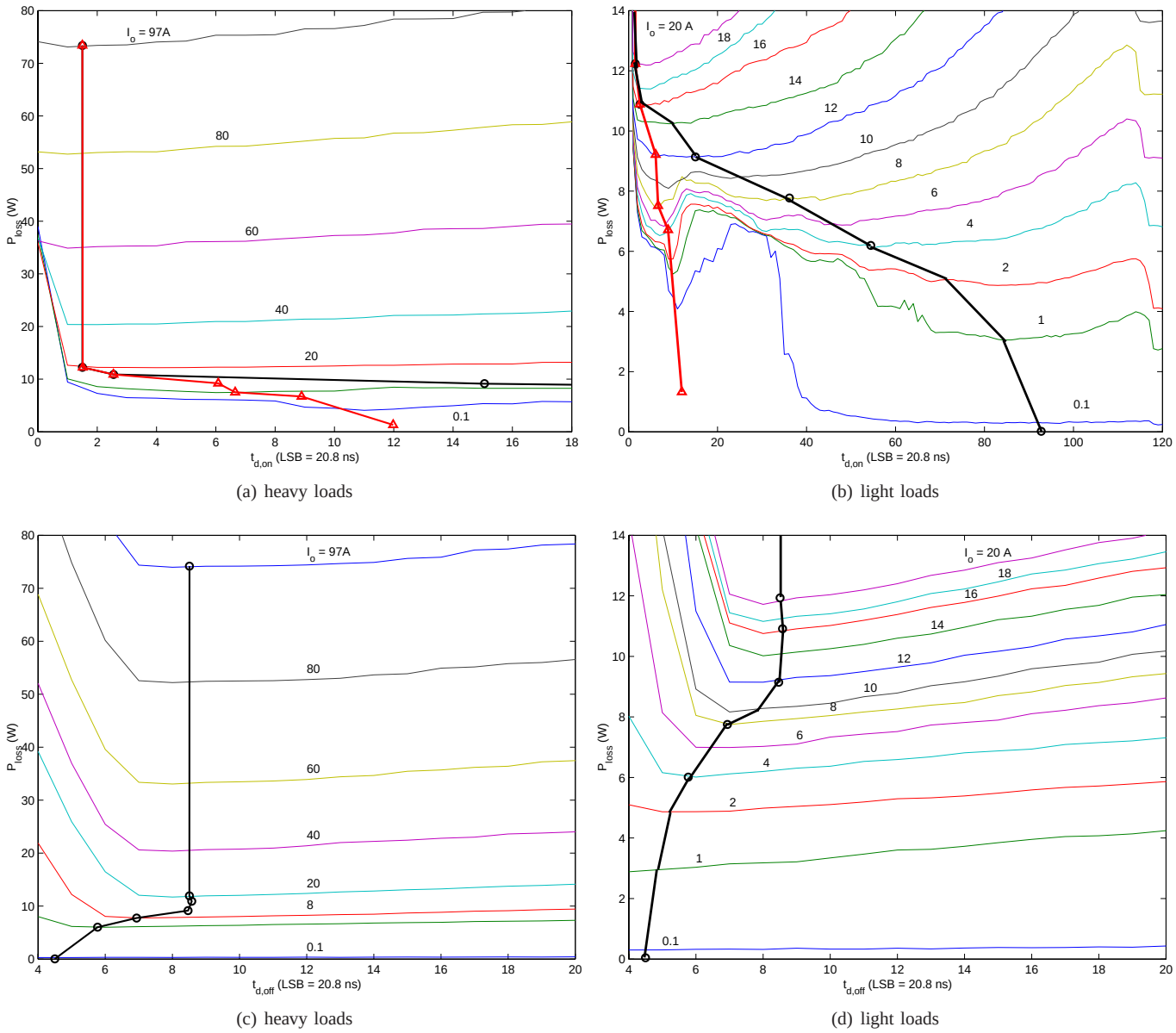


Fig. 4. Piecewise linear function modelling deadtime $t_d(I_o)$.

IV. Experimental Results

The algorithm described above was tested on a digitally-controlled 4-phase, 100 W, 12-to-1 V buck converter, switch-

[2] In power electronic systems the perturbation naturally introduced by the switching action can be used to optimize the system operation on-line [9], [10]. However, this approach cannot be used to adjust parameters which are not directly related to the switching action, such as the SR timing.



(a) heavy loads (b) light loads

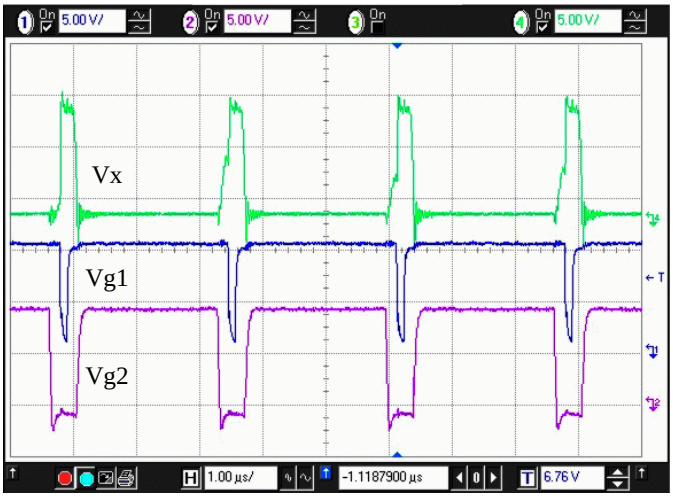
(c) heavy loads (d) light loads

Fig. 5. Power loss as a function of $t_{d,on}$ (a), (b), and $t_{d,off}$ (c), (d), parametrized by load current. The thicker lines depict the corresponding optimal $t_{d,on}$ and $t_{d,off}$ as a function of load current, as determined by the on-line extremum seeking algorithm. Note that the intersections of these lines with the power loss curves coincide with the power loss minima.

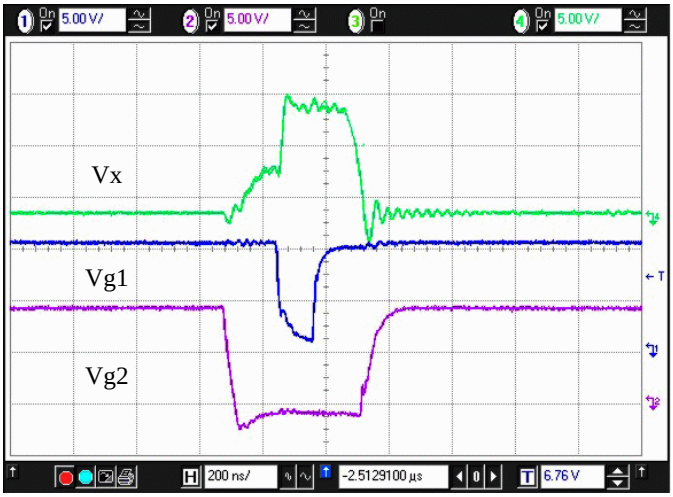
ing at 375 kHz per phase. The perturbation signals $\tilde{t}_{d,on}$ and $\tilde{t}_{d,off}$ were square waves at 20.9 and 41.8 Hz, respectively, with one hardware least significant bit (LSB) peak-to-peak amplitude (20.8 ns). The piecewise linear curves for $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$ had 7 vertices: 6 of them at 4 A steps between 0 and 20 A, and another vertex at 100 A. Further, the minimum control switch on-time was limited to 2 LSB's (41.6 ns), forcing the converter to enter pulse skipping mode for load currents below 2 A, resulting in low power dissipation at very low loads.

Fig. 5 shows the converter power loss, measured off-line, as a function of the SR timing and parameterized by load current. If the SR is kept off, the converter enters DCM for load currents below 17 A. As a result, at light loads the global power loss minimum shifts to large $t_{d,on}$ values [Fig. 5(b)], corresponding to the SR turning on when the inductor is discharging, and turning off when the inductor current becomes zero. Under these conditions another local minimum is observed for small $t_{d,on}$ values, denoted with $\triangle$'s in Figures 5(a,b), corresponding to the converter accomplishing soft-switching by letting negative inductor current charge up the switching node capacitance to V_{in}. Also note that the abrupt dips in power loss at the right end of Fig. 5(b) correspond to the SR being off all the time and thus not contributing switching losses. These indicate that for load currents below about 3 A, it is beneficial to completely turn off the SR to minimize power loss, which can be accomplished through a software limit.

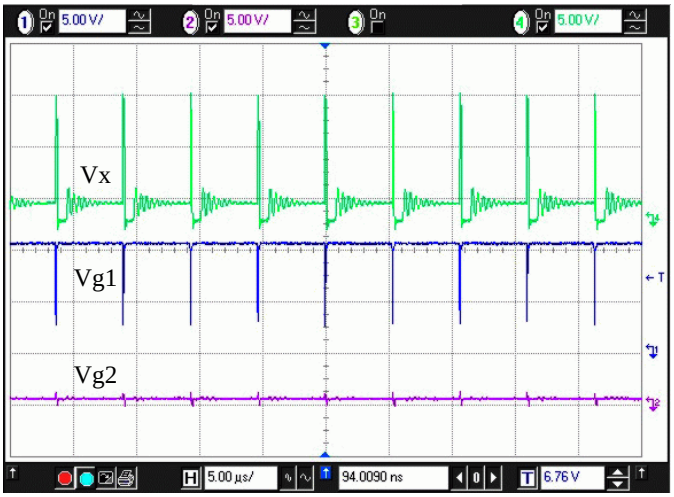
The thick lines in Fig. 5 depict the curves for the SR timing vs. load current resulting from on-line tests of the extremum seeking algorithm. Parameter $t_{d,on}$ is constant for heavy loads (a), but varies over a wide range for light loads (b), since



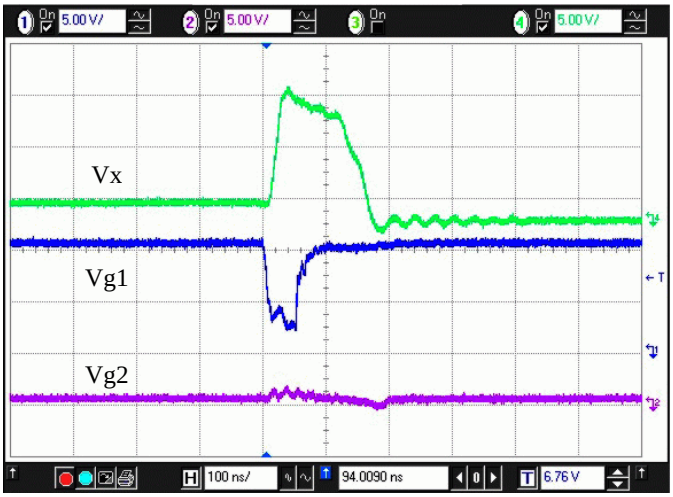
(a) DCM operation (I_o = 10 A, f_{sw} = 375 kHz)



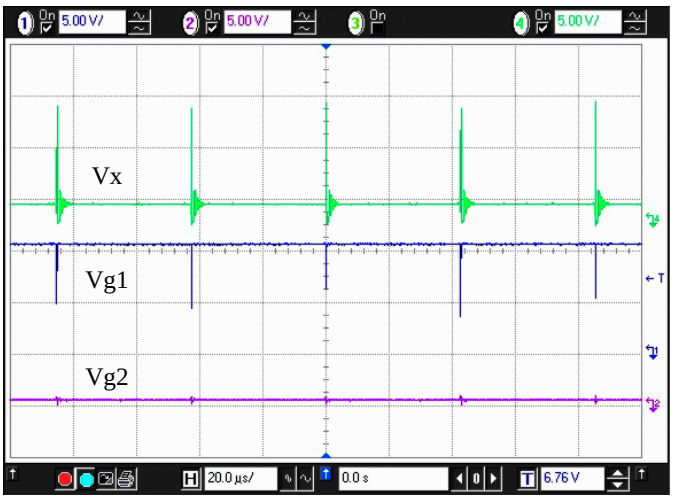
(b) Zoom-in of (a)



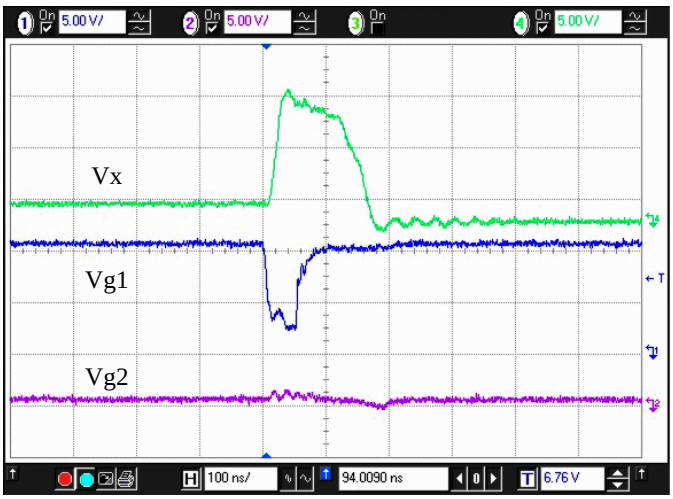
(c) Pulse skipping operation (I_o = 1 A, f_{sw} = 188 kHz)



(d) Zoom-in of (c)



(e) Pulse skipping operation (I_o = 0.1 A, f_{sw} = 23.5 kHz)



(f) Zoom-in of (e)

Fig. 6. Sample switching waveforms (V_{in} = 10 V, V_o = 1 V).

the optimal SR on-time is a strong function of load current in DCM. The right curve in (b), denoted with ○'s, corresponds to optimal DCM operation, as described above. If it is desirable to ensure that the algorithm will latch on this curve and not on the soft-switching mode, a software limit has to be imposed on $t_{d,on}$ for small loads.

Finally, Fig. 6 shows some sample converter waveforms, illustarting behavior at different load currents. Note that the

prototype power train uses p-channel MOSFET's as high-side control switches, hence the inverted polarity of V_{g1}. Figures 6(a,b) show DCM operation at 10 A with $t_{d,on} \approx 170$ ns (for comparison, in CCM, $t_{d,on} \approx 40$ ns). The switching frequency corresponds to the default of 375 kHz. Figures 6(c–f) illustrate pulse skipping at light loads. At both 1 A and 0.1 A, the commanded control switch on-time corresponds to the 2 LSB (41.6 ns) limit imposed by the controller. The actual pulse width is about 140 ns, due to the MOSFET turn-off delay. As expected, the switching frequency decreases at lighter loads. At 1 A it is 188 kHz, half the default, and at 0.1 A it is 23.5 kHz, one sixteenth of the default.

V. Conclusion

The proposed multi-mode control strategy allows for efficient operation of the buck converter over a wide load range. Thus, it is particularly well suited for portable electronic devices, such as laptop computers and cellular phones, which follow a trend of increasing power consumption, while preferably maintaining or extending battery life. The discussed control approach matches the advantages and constraints of a digital controller implementation: it uses data storage and computationally sophisticated adaptive algorithms, which do not require fast analog-to-digital conversion at rates beyond the switching frequency. Finally, the multi-parameter extremum seeking approach discussed in this paper, can be applied to other on-line optimization problems such as current balancing in interleaved or otherwise paralleled converter stages.

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