Quantization Resolution and Limit Cycling in Digitally Controlled PWM Converters

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***Abstract*—This paper discusses the presence of steady-state limit cycles in digitally controlled pulse-width modulation (PWM) converters, and suggests conditions on the control law and the quantization resolution for their elimination. It then introduces single-phase and multi-phase controlled digital dither as a means of increasing the effective resolution of digital PWM (DPWM) modules, allowing for the use of low resolution DPWM units in high regulation accuracy applications. Bounds on the number of bits of dither that can be used in a particular converter are derived. Finally, experimental results confirming the theoretical analysis are presented.**

***Index Terms*—Analog-digital conversion, digital control, dither, finite wordlength effects, power conversion, pulse-width modulation, quantization, stability, voltage regulation.**

I. Introduction

DIGITAL controllers for pulse-width modulation (PWM) converters enjoy growing popularity due to their low power, immunity to analog component variations, compatibility with digital systems, and faster design process, as discussed in [1] and the references therein. They have the potential to implement sophisticated control schemes and to accurately match duty cycles in interleaved converters. Their applications include microprocessor voltage regulation modules (VRMs), portable electronic devices, and audio amplifiers, among many others.

This paper discusses conditions for the elimination of limit cycles, steady state oscillations at frequencies lower than the switching frequency, in digitally controlled PWM converters, as well as techniques for increasing the effective resolution of digital PWM (DPWM) modules. Section II gives an overview of the structure of digital PWM controllers. Section III describes limit cycles and presents conditions for their elimination. Section IV introduces controlled digital dither as a technique that effectively increases the resolution of the DPWM module, allowing for the use of low resolution DPWM modules in applications requiring high regulation accuracy, such as VRMs. The use of low resolution DPWM modules in these applications, without incurring limit cycles, can result in substantial power and silicon area savings. Section V presents results from a prototype converter implementing the findings of this paper.

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II. Digital Controller Structure

A block diagram of a digitally controlled PWM buck converter is shown in Fig. 1. The controller consists of an analog-to-digital converter (ADC) which digitizes the regulated quantity (e.g., the output voltage V_{out}), a DPWM module, and a discrete-time control law. A discrete-time PID control law has the form

$$D_c(k+1) = -K_p D_e(k) - K_d[D_e(k) - D_e(k-1)] - K_i D_i(k) + D_{ref}(k) \quad (1)$$

where $D_c(k)$ is the duty cycle command at discrete time k, $D_e(k)$ is the error signal

$$D_e(k) = D_{out}(k) - D_{ref}(k), \quad (2)$$

and $D_i(k)$ is the state of an integrator

$$D_i(k+1) = D_i(k) + D_e(k). \quad (3)$$

Further, K_p is the proportional gain, K_d is the derivative gain, and K_i is the integral gain. Variable $D_{ref}(k)$ represents the reference voltage, and $D_{out}(k)$ is the digital representation of V_{out}. All variables are normalized to the input voltage, V_{in}. Variable D_{ref} is used as a feedforward term in (1). Note that D_{ref} by itself would give the correct duty cycle command for steady state operation with constant load, if there were no load-dependent voltage drop along the power train and no other nonidealities in the output stage [2]. Design of digital PID control law is discussed in [3]–[5].

III. Conditions for the Elimination of Limit Cycles

For the converter of Fig. 1, limit cycles refer to steady-state oscillations of V_{out} and other system variables at frequencies lower than the converter switching frequency f_{sw}. Limit cycles may result from the presence of signal amplitude quantizers like the ADC and DPWM modules in the feedback loop. Steady-state limit cycling may be undesirable if it leads to large, unpredicted output voltage variations. Furthermore, since the limit cycle amplitude and frequency are hard to predict, it is difficult to analyze and compensate for the resulting V_{out} noise and the electro-magnetic interference (EMI) produced by the converter.

Let us consider a system with ADC resolution of N_{adc} bits and DPWM resolution of N_{dpwm} bits. For a buck converter, this will correspond to voltage quantization of $\Delta V_{adc} = V_{in}/2^{N_{adc}}$ steps for the ADC, and $\Delta V_{dpwm} = V_{in}/2^{N_{dpwm}}$ for the

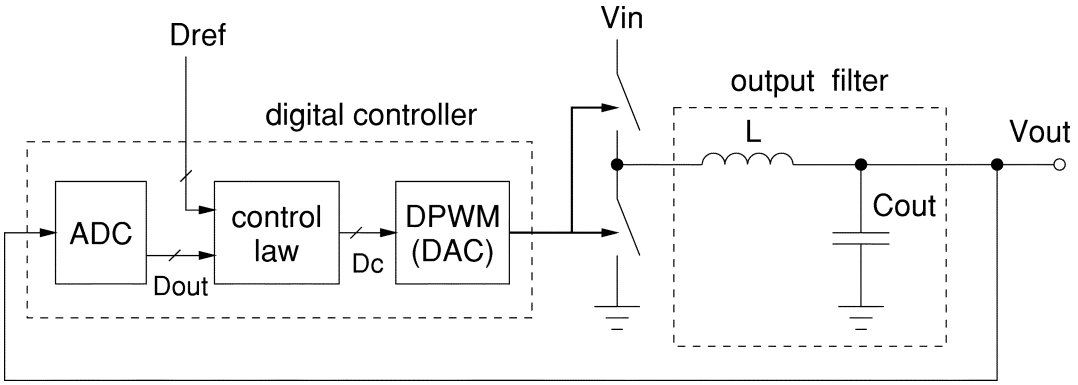

Fig. 1. Block diagram of a digitally controlled PWM buck converter.

DPWM. Fig. 2(a)[1] illustrates qualitatively the behavior of V_{out} in steady state when the DPWM resolution is less than the ADC resolution, and there is no DPWM level that maps into the ADC bin corresponding to the reference voltage V_{ref} (this ADC bin will be referred to as the *zero-error bin*). In steady state, the controller will be attempting to drive V_{out} to the zero-error bin, however due to the lack of a DPWM level there, it will alternate between the DPWM levels around the zero-error bin. This results in nonequilibrium behavior, such as steady-state limit cycling.

The first step toward eliminating limit cycles is to ensure that under all circumstances there is a DPWM level that maps into the zero-error bin. This can be guaranteed if the resolution of the DPWM module is finer than the resolution of the ADC. A one-bit difference in the resolutions, $N_{dpwm} = N_{adc}+1$, seems sufficient in most applications since it provides two DPWM levels per one ADC level

$$\textbf{No Limit Cycle Condition \#1}$$
$$\boldsymbol{resolution(DPWM) > resolution(ADC)}. \quad (4)$$

Yet, even if the above condition is met, limit cycling may still occur if the feedforward term is not perfect and the control law has no integral term ($K_i = 0$). In this case, the controller relies on nonzero error signal D_e to drive V_{out} toward the zero-error bin. However, once V_{out} is in the zero-error bin, the error signal becomes zero, and V_{out} droops back below the zero-error bin. This sequence repeats over and over again, resulting in steady-state limit cycling. This problem can be solved by the inclusion of an integral term in the control law. After a transient, the integrator will gradually converge to a value that drives V_{out} into the zero-error bin, where it will remain as long as $D_e = 0$, since a digital integrator is perfect [Fig. 2(b)]

$$\textbf{No Limit Cycle Condition \# 2}$$
$$\boldsymbol{0 < K_i \leq 1}. \quad (5)$$

An upper bound of unity is imposed on the integral gain, since the digital integrator is intended to fine-tune the output voltage, therefore it has to be able to adjust the duty cycle command by steps as small as a least significant bit (LSB).

[1]In all simulations the data is sampled at the switching frequency, therefore the switching ripple on V_{out} cannot be seen. For the discussions in this paper the switching ripple is not of interest and its omission makes the plots clearer.

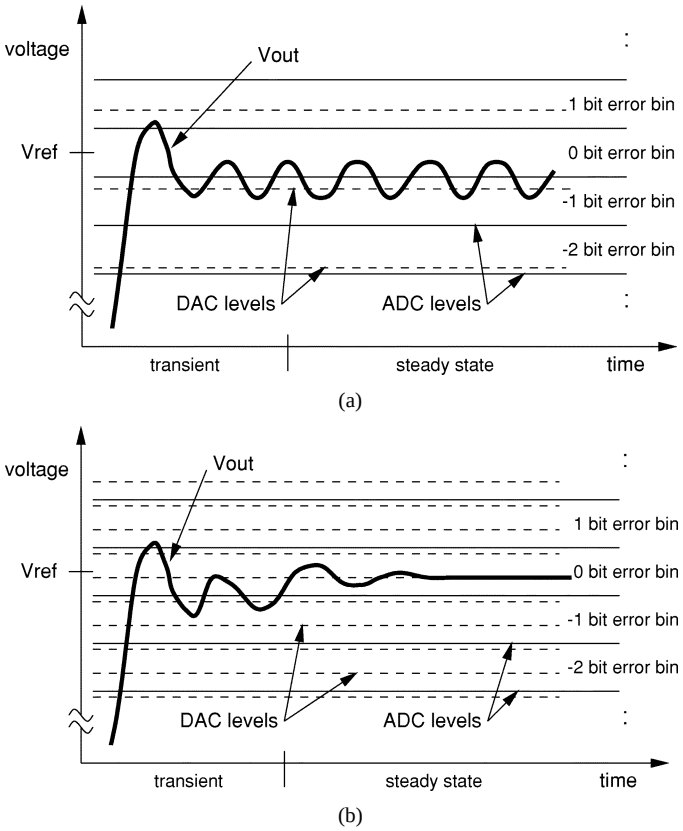

Fig. 2. Qualitative behavior of V_{out} with (a) DPWM resolution lower than the ADC resolution and (b) DPWM resolution two times the ADC resolution and with integral term included in control law.

Fig. 3(a) shows a simulation of the transient response of a digitally controlled PWM converter. The resolution of the DPWM module, $N_{dpwm} = 10$ bits, is higher than the resolution of the ADC, $N_{adc} = 9$ bits, however steady-state limit cycling is observed both before and after the load current step, since no integral term was used in the control law. On the other hand, in Fig. 3(b) an integral term is added to the control law, and the steady-state limit cycling is eliminated.

The two conditions suggested above are not sufficient for the elimination of steady-state limit cycles, since the nonlinearity of the quantizers in the feedback loop may still cause limit cycling for high loop gains. Non-linear system analysis tools, such as describing functions [5]–[7], can be used to determine the maximum allowable loop gain not inducing limit cycles. The

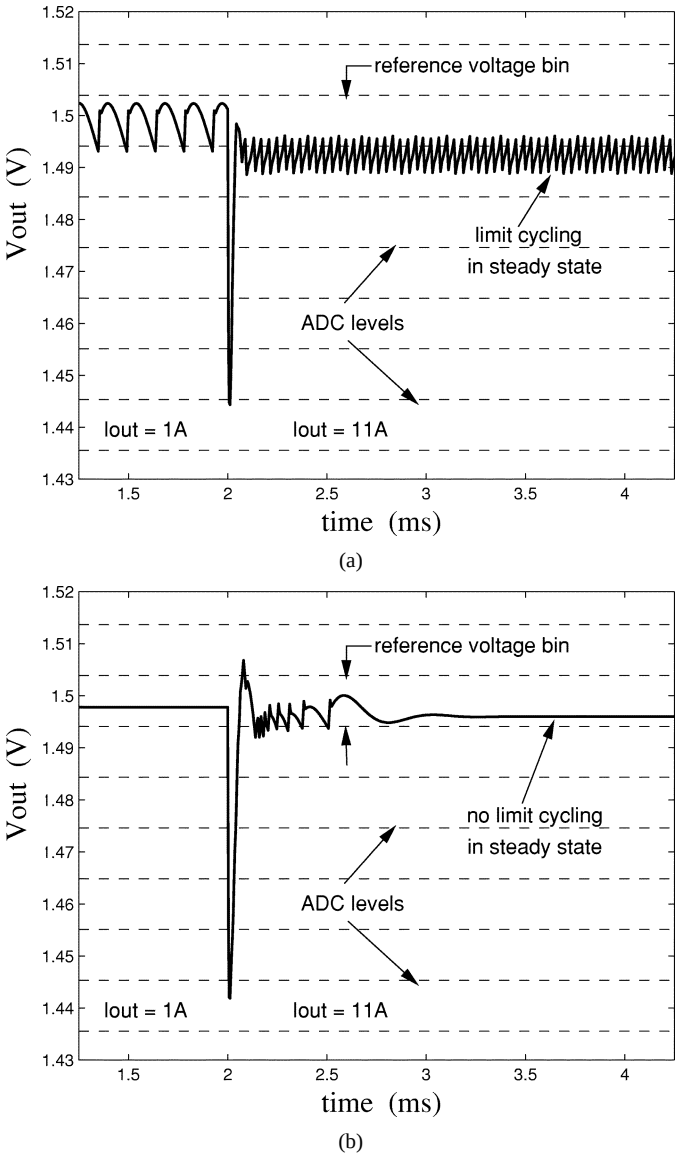

Fig. 3. Simulation of a DPWM converter output voltage under a load current transient with integral term: (a) not included and (b) included in control law. $V_{in} = 5$ V, $V_{ref} = 1.5$ V, $f_{sw} = 250$ kHz, $N_{adc} = 9$ b, and $N_{dpwm} = 10$ b.

feedback loop of the converter includes two quantizers—the ADC and the DPWM—however in the present analysis we will consider only the ADC nonlinearity, since it performs coarser quantization if the DPWM resolution is made higher than that of the ADC (as recommended above). The describing function of an ADC (a round-off quantizier) represents its effective gain as a function of the input signal ac amplitude and dc bias. When the control law contains an integral term, only limit cycles that have zero dc component can be stable, because the integrator drives the dc component of the error signal to the zero-error bin. Since in steady state the dc bias is driven to zero, and since the loop transmission, $L(j\omega)$, from the output of the ADC to its input has a low-pass characteristic, the sinusoidal-input describing function of a round-off quantizer can be used to analyze the stability of the system. The characteristic of a round-off quantizer is plotted in Fig. 4(a), where $V_{in,\,adc}$ is the ADC input voltage, ΔV_{adc} is the ADC quantization bin size corresponding to one LSB, and D_{out} is the quantized representation of $V_{in,\,adc}$. The corresponding describing function, $N(A)$, is plotted in Fig. 4(b), where A is the ac amplitude of $V_{in,\,adc}$. From the plot it can be seen that the describing function has a maximum value of about 1.3, corresponding to maximum effective ADC gain. The control law (1), and hence $L(j\omega)$, can then be designed to exclude limit cycles by ensuring that

$$\textbf{No Limit Cycle Condition \#3}$$
$$\boldsymbol{1 + N(A)L(j\omega) \neq 0} \qquad (6)$$
$$(Nyquist\ Criterion)$$

holds for all nonzero finite signal amplitudes A and frequencies ω. In practice, conventional loop design methods (e.g., Bode plots) can be used, keeping in mind that the effective ADC gain peaks somewhat above unity.

IV. Controlled Digital Dither

The precision with which a digital controller regulates V_{out} is determined by the resolution of the ADC. In particular, V_{out} can be regulated with a tolerance of one LSB of the ADC. Many present-day applications, such as microprocessor VRMs, demand regulation precision of about 10 mV [8], requiring ADCs and DPWM modules with very high resolution. For example, regulation resolution of 10 mV at $V_{in} = 12$ V corresponds to ADC resolution of $N_{adc} = \log_2(12\ \text{V}/10\ \text{mV}) \approx 10$ bits, implying DPWM resolution of at least $N_{dpwm} = 11$ bits to avoid steady-state limit-cycling. For a converter switching frequency of $f_{sw} = 1$ MHz, such resolution would require a $2^{11} f_{sw} = 2$ GHz fast clock in a counter-comparator implementation of the DPWM module, or $2^{11} = 2048$ stages in a ring oscillator implementation, resulting in high power dissipation or large area [7], [9], [1]. Thus, it is beneficial to look for ways to use low-resolution DPWM modules to achieve the desired high V_{out} resolution.

One method which can increase the effective resolution of a DPWM module is dithering. It amounts to adding high-frequency periodic or random signals to a certain quantized signal, which is later filtered to produce averaged dc levels with increased resolution. Analog dither has been used to increase the effective resolution of a DPWM module [10]. However, analog dither is difficult to generate and control, it is sensitive to analog component variations, and it can be mixed only with analog signals in the converter, and not with signals inside a digital controller. On the other hand, digital dither generated inside the controller is simpler to implement and control, is insensitive to analog component variations, and can offer more flexibility. Therefore, the use of digital dither to improve the resolution of DPWM modules is discussed in the present section.

A. Single-Phase Dither

The idea behind digital dither is to vary the duty cycle by an LSB over a few switching periods, so that the *average* duty cycle has a value *between* two adjacent quantized duty cycle levels. The averaging action is implemented by the output LC filter. The dither concept is illustrated in Fig. 5. Let D_{c1} and D_{c2} correspond to two adjacent quantized duty cycle levels put out by the DPWM module, $D_{c2} = D_{c1} + LSB$. If the duty cycle is made to alternate between D_{c1} and D_{c2} every next

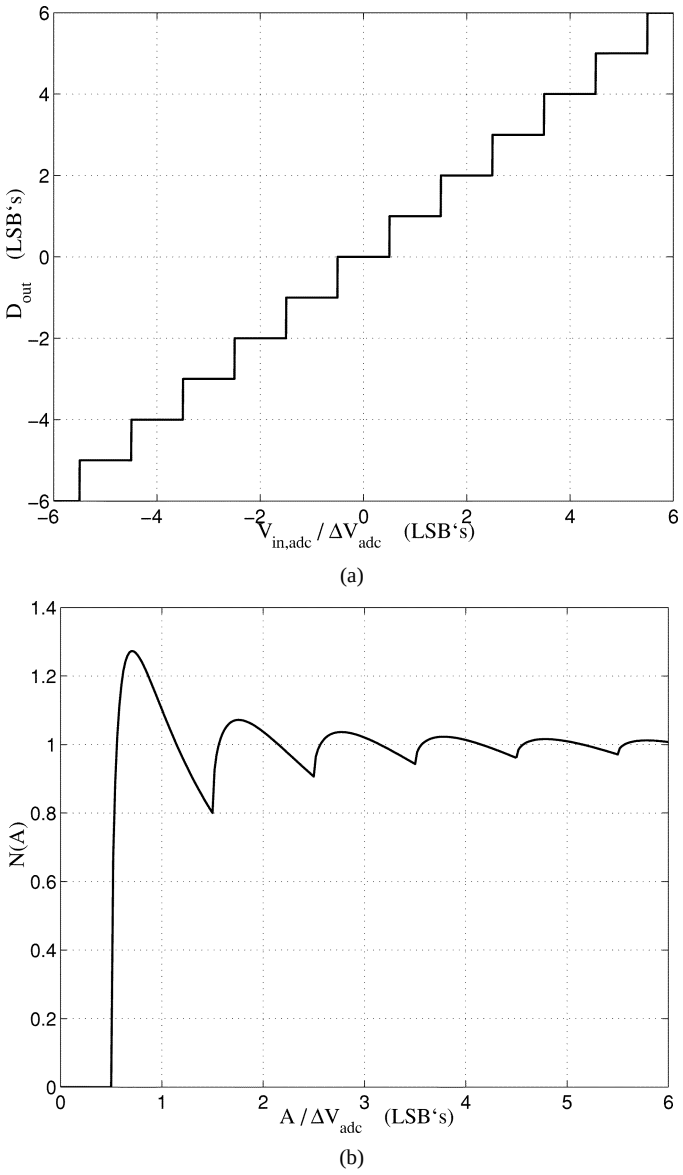

Fig. 4. Characteristic of: (a) a round-off quantizer and (b) the corresponding describing function for sinusoidal signals with zero dc bias.

switching period, the average duty cycle over time will equal $(D_{c1} + D_{c2})/2 = D_{c1} + (1/2)LSB$. Thus, an intermediate $(1/2)LSB$ sub-bit level can be implemented by averaging over two switching periods, resulting in an increase of the effective DPWM resolution of 1 b. Using the same reasoning, $(1/4)LSB$ and $(3/4)LSB$ levels can be implemented by averaging over four switching periods (Fig. 6), which increases the effective DPWM resolution by 2 b. Finally, it can be seen that by using dither patterns spanning 2^M switching periods, the effective DPWM resolution can be increased by M b

$$N_{dpwm,\,eff} = N_{dpwm} + M \tag{7}$$

where N_{dpwm} is the hardware DPWM resolution, and $N_{dpwm,\,eff}$ is the effective DPWM resolution.

B. Dither Patterns

Of course, the effective increase in DPWM resolution by dithering does not come for free. The dithering of the duty

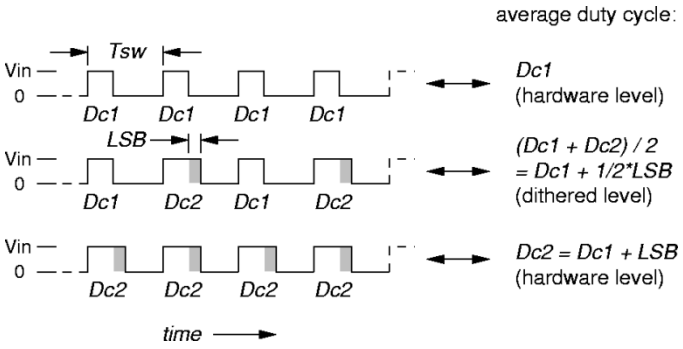

Fig. 5. Use of switching waveform dither to realize a $(1/2)LSB$ DPWM level (1-b dither).

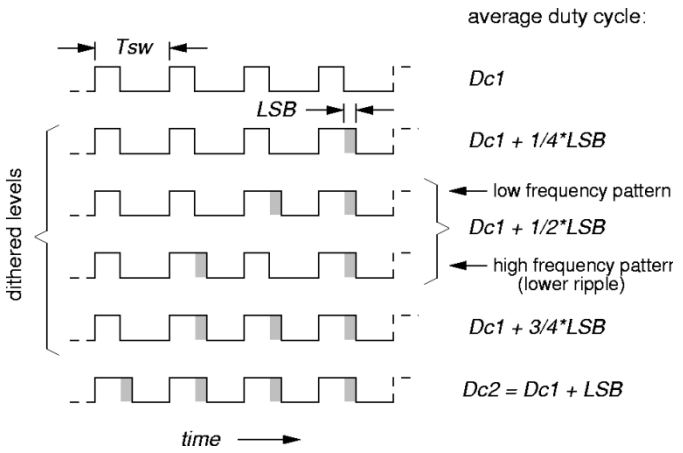

Fig. 6. Switching waveform dither patterns realizing $(1/4)LSB$, $(1/2)LSB$, and $(3/4)LSB$ DPWM levels (2-b dither).

cycle creates an additional ac ripple at the output of the LC filter, which is superimposed on the ripple from the converter switching action. It is desirable to keep the amplitude of the dither ripple low, in order to avoid poor output regulation, EMI, and limit cycles (which may result from the interaction between the dither ripple and the ADC). Thus it is beneficial to select dither patterns that minimize the dither ripple.

For a dither sequence with a particular length (2^M switching cycles for M-bit dither) there may be a few different dither patterns that average to the same dc level. For example, in Fig. 6 the $(1/2)LSB$ level can be implemented with two different sequences: $\{D_{c1}, D_{c1}, D_{c2}, D_{c2}\}$ or $\{D_{c1}, D_{c2}, D_{c1}, D_{c2}\}$. The latter pattern has higher fundamental frequency, and thus produces less output voltage ripple, due to the low-pass characteristic of the output LC filter.

Two sets of 3-b dither sequences are shown in Table I, with "1" standing for the addition of an LSB to the duty cycle. Table I(a) corresponds to a simple rectangular waveform dither discussed in [11]. The generation of these patterns is very systematic and thus easy to implement. On the other hand, the dither sequences in Table I(b) were chosen with the aim of minimizing their low frequency spectral content. Thus, when filtered, they produce the lowest ripple for a given average duty cycle. Notice that, while for the rectangular-waveform dither the sequences producing *lowest* ripple are $\{0, 0, 0, 0, 0, 0, 0, 1\}$ and its complement, for the minimum-ripple dither the ripple produced by any sequence does not exceed the ripple produced

by $\{0, 0, 0, 0, 0, 0, 0, 1\}$ and its complement. Therefore, the minimum-ripple sequences have a clear advantage over the rectangular-waveform sequences, with respect to dither ripple size.

Yet another dither generation approach is to use $\Sigma\Delta$ modulation, however it does not guarantee minimum-ripple patterns, and further the dither spectral content is hard to predict. $\Sigma\Delta$ modulation in power electronics applications is discussed, for example, in [12] and [13].

C. Dither Generation Scheme

Fig. 7 shows a dither generation scheme that can produce patterns of *any* shape, and can therefore implement minimum-ripple dither such as the one in Table I(b). A look-up table stores 2^M dither sequences, each 2^M b long, corresponding to the sub-bit levels implemented with M-bit dither. The M LSBs of the duty cycle command D_c select the dither sequence corresponding to the appropriate sub-bit level, while the M-bit counter sweeps through this dither sequence. The dither pattern is then added to the N MSBs of D_c to produce the duty cycle command D_c' which is sent to the hardware DPWM module.

D. Dither Ripple Size

In Section IV-A it was shown that the longer the dither patterns used, the larger the effective DPWM resolution. However, longer dither patterns can cause higher output ripple, since they contain lower frequency components, and the LC filter has less attenuation at lower frequencies. This consideration puts a practical limit on the number of bits of dither that can be added to increase the resolution of the DPWM module.

For the rectangular-waveform dither in Table I(a) some simple mathematical analysis (see the Appendix) can give an estimate of the maximum peak-to-peak ripple added to the output voltage as a result of the dither

$$v_{p-p,\,dith} \le \left(\frac{f_c}{f_{sw}}\right)^2 2^{2M}\,\frac{4}{\pi}\,\frac{V_{in}}{2^{N_{dpwm}}} \tag{8}$$

for $f_c < f_{dith} < f_z$, and

$$v_{p-p,\,dith} \le \frac{f_c^2}{f_z f_{sw}}\,2^M\,\frac{4}{\pi}\,\frac{V_{in}}{2^{N_{dpwm}}} \tag{9}$$

for $f_c < f_z < f_{dith}$, where f_{dith} is the fundamental frequency of the dither

$$f_{dith} = f_{sw}/2^M \tag{10}$$

f_c is the LC filter cutoff frequency, and f_z is the ESR zero frequency associated with the output capacitor.

Once the amplitude of the dither is known, we can develop a condition on how many bits of dither, M, can be used in a certain system, without inducing limit cycles (see the Appendix),

$$M < \frac{1}{3}\log_2\left[\frac{\pi}{4}\left(\frac{f_{sw}}{f_c}\right)^2\left(2^{\Delta N}-1\right)\right] \tag{11}$$

for $f_c < f_{dith} < f_z$, and

$$M < \frac{1}{2}\log_2\left[\frac{\pi}{4}\,\frac{f_z f_{sw}}{f_c^2} = \left(2^{\Delta N}-1\right)\right] \tag{12}$$

TABLE I
3-B DITHER SEQUENCES

Sequence Average	*Dither Sequence*								*Ripple*
0	0	0	0	0	0	0	0	0	*none*
1/8	0	0	0	0	0	0	0	1	*lowest*
2/8	0	0	0	0	0	0	1	1	
3/8	0	0	0	0	0	1	1	1	
4/8	0	0	0	0	1	1	1	1	***highest***
5/8	0	0	0	1	1	1	1	1	
6/8	0	0	1	1	1	1	1	1	
7/8	0	1	1	1	1	1	1	1	*lowest*

(a)

Sequence Average	*Dither Sequence*								*Ripple*
0	0	0	0	0	0	0	0	0	*none*
1/8	0	0	0	0	0	0	0	1	***highest***
2/8	0	0	0	1	0	0	0	1	
3/8	0	0	1	0	0	1	0	1	
4/8	0	1	0	1	0	1	0	1	*lowest*
5/8	0	1	0	1	1	0	1	1	
6/8	0	1	1	1	0	1	1	1	
7/8	0	1	1	1	1	1	1	1	***highest***

(b)

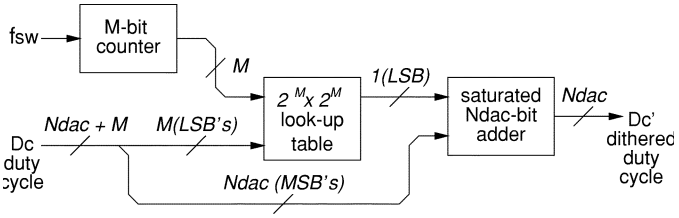

Fig. 7. Structure for adding arbitrary dither patterns to the duty cycle.

for $f_c < f_z < f_{dith}$, where

$$\Delta N = N_{dpwm,\,eff} - N_{adc} = (N_{dpwm} + M) - N_{adc} \tag{13}$$

is the difference between the effective resolutions of the DPWM and the ADC (in bits). For example, in Section III it was suggested that making the resolution of the DPWM one bit higher then that of the ADC adequately satisfies the condition to eliminate steady-state limit cycling, hence $\Delta N = 1$. The above equations can be used by starting with a guess for M, obtaining the corresponding dither frequency from (10), and then using (11) or (12), respectively, to obtain a bound on M. If the result is not consistent with the initial guess for M, the procedure should be repeated with a reduced value of M. On the other hand, if the inequalities are satisfied, the value of M can be increased, and the procedure can be repeated.

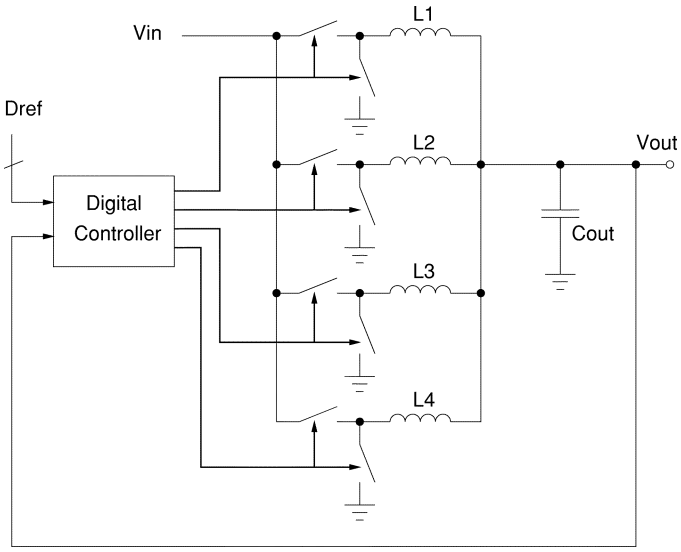

Fig. 8. Block diagram of a four-phase buck converter.

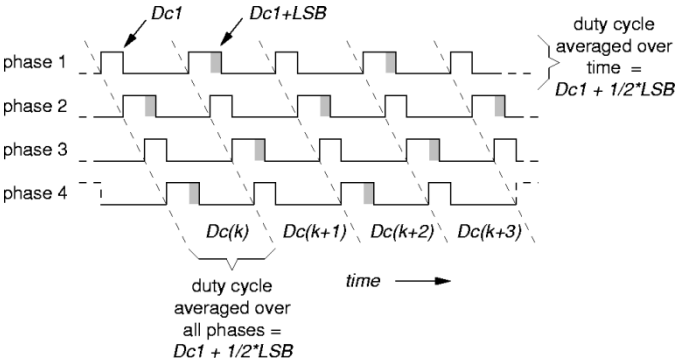

Fig. 9. Four-phase switching waveform dither patterns implementing a $(1/2)LSB$ DPWM level.

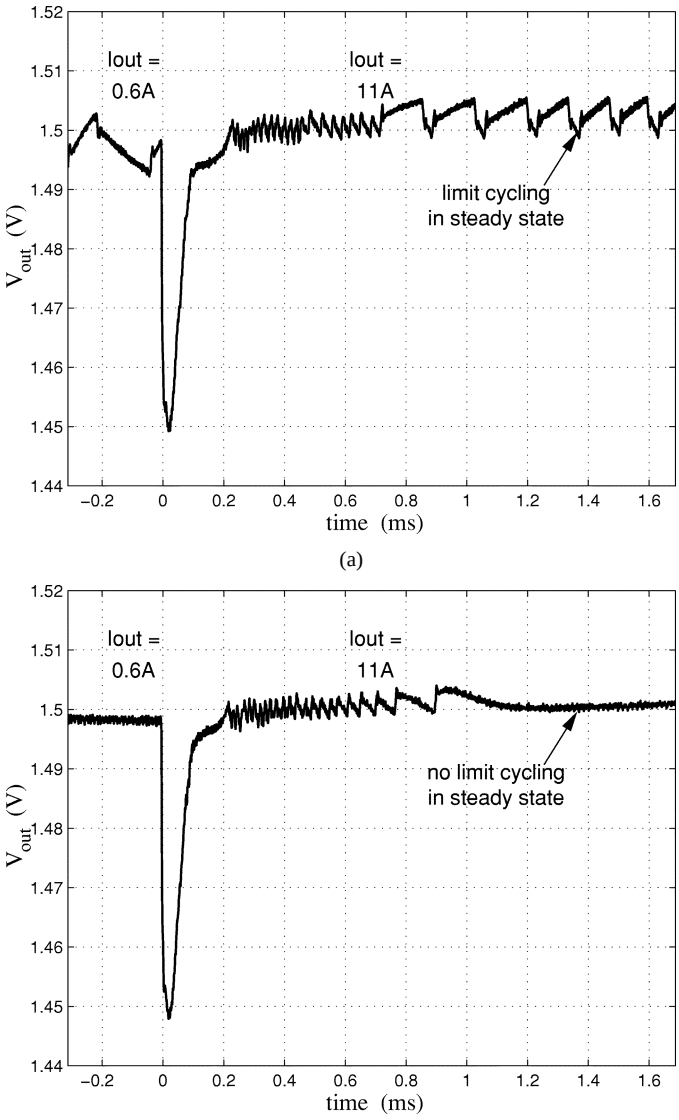

Fig. 10. Experimental four-phase buck converter transient response under a load current step with: (a) $N_{dpwm} = 7$ b and (b) $N_{dpwm,\,eff} = 7$ b + 3-b dither = 10 b. $N_{adc} = 9$ b, $V_{in} = 5$ V, $V_{ref} = 1.5$ V, $f_{sw} = 250$ kHz.

In Section IV-B it was shown that there are dither patterns, such as the minimum-ripple dither in Table I, that produce lower ripple compared to the rectangular-waveform dither on which the above analysis is based. If such dither patterns are used, (8) and (9) give an overestimate, while (11) and (12) yield an underestimate. Nevertheless, these equations are still a useful tool for conservative design, since ripple amplitude analysis of the minimum-ripple dither is far more involved.

E. Multi-Phase Dither

The concept of controlled dither can be extended to multi-phase (interleaved) VRMs. In a multi-phase converter, multiple single-phase power trains are connected to a common output capacitor and switched with the same duty cycle, but out of phase, which decreases the ripple in the output voltage and input current. For example, the block diagram of a four-phase buck converter is shown in Fig. 8. In this case, the four power train legs are switched $360°/4 = 90°$ out of phase.

The controlled dither technique developed for single phase converters can be applied directly to the multi-phase case. For example, to achieve a $D_{c1} + (1/2)LSB$ level, duty cycle D_{c1} is applied to *all* phases for one switching period, followed by $D_{c2} = D_{c1} + LSB$ applied to all phases, and so on. However, in a multi-phase converter we can exploit the additional degrees of freedom associated with the independent switching of the different phases to further reduce the dither ripple, and thus allow more bits of dither, and respectively less bits of hardware resolution of the DPWM module.

Consider again the case of a $D_{c1} + (1/2)LSB$ level. This level can be implemented by commanding, in the same switching period, D_{c1} to two of the phases and D_{c2} to the other two, so that the average duty cycle over all phases is $D_{c1} + (1/2)LSB$ for that period. The next switching period the duty cycle commands are toggled, so that the average over all phases is still $D_{c1} + (1/2)LSB$, however the *average over time* for each phase is $D_{c1} + (1/2)LSB$ as well (Fig. 9). The equal averaging over time for each phase is necessary to avoid dc current mismatch among the phases. This approach can be extended for other sub-bit levels, like $D_{c1} + (1/4)LSB$, noting that for a multiphase converter with N_ϕ phases, $\log_2 N_\phi$ bits of dither can be implemented by averaging over the phases.

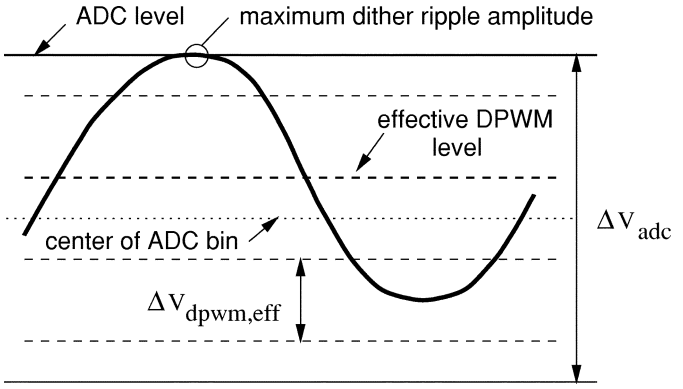

Fig. 11. Maximum dither ripple amplitude constraint. Illustrated case is for $N_{dpwm,\,eff} = N_{adc} + 2$.

Multiphase dither can increase the dither frequency seen at the output node about N_ϕ times, thus reducing the resulting ripple, and allowing approximately $\log_2 N_\phi$ more bits of DPWM resolution to be implemented with dither.

V. Experimental Results

The digital dither technique was tested on a prototype four-phase buck converter with results confirming the theoretical expectations. In the prototype, the ADC had 9-b resolution and the DPWM had 7 b of hardware resolution. The control law included an integral term, thus (5) was satisfied. Condition (6) was satisfied as well, by design of the proportional gain. The transient response of the converter due to a load current step is shown in Fig. 10(a). The system exhibits steady-state limit cycling since condition (4) is not met. Subsequently 3-b single-phase digital dither was introduced, using the minimum ripple sequences from Table I(b), thus increasing the effective resolution of the DPWM module to $7+3=10$ bits. The step response of the modified system is shown in Fig. 10(b). The effective resolution of the DPWM is now higher than that of the ADC, and all three *no-limit-cycle* conditions (4)–(6) are satisfied. Consequently, limit cycles are prevented. It should be noted that in this case the steady state ripple is only due to the multiphase switching and the dither, and it does not exceed a few millivolts. This example illustrates the validity of the *no-limit-cycle* conditions, as well as the effectiveness of the controlled dither concept.

VI. Conclusion

This paper discussed the presence of steady-state limit cycles in digitally controlled PWM converters, and suggested conditions on the control law, and the ADC and DPWM resolutions for their elimination. It then introduced single-phase and multi-phase controlled digital dither as a means of increasing the effective resolution of DPWM modules, allowing for the use of low resolution DPWM units in high regulation accuracy applications. Bounds on the number of bits of dither that can be used in a particular converter were derived.

Appendix
Dither Ripple Calculations

Since the dither constitutes switching between two adjacent quantized duty cycle levels, it can be modeled as a square wave with peak-to-peak amplitude of one hardware LSB of the DPWM module equal to $V_{in}/2^{N_{dpwm}}$. For M-bit rectangular-waveform dither [Table I(a)], the dither waveform with the largest low frequency component is a square wave with 50% duty ratio at frequency

$$f_{dith} = f_{sw}/2^M. \tag{14}$$

This waveform can be used to study the worst case dither ripple. Since the dither is smoothed by the converter output LC filter, it is sufficient to consider only its fundamental frequency component, which is a sine wave with frequency f_{dith} and peak-to-peak amplitude

$$A_{p\text{–}p,\,dith} = \frac{4}{\pi}\,\frac{V_{in}}{2^{N_{dpwm}}}. \tag{15}$$

The peak-to-peak output voltage ripple can then be bounded approximately as

$$v_{p\text{–}p,\,dith} \le H(f_{dith}) A_{p\text{–}p,\,dith} \tag{16}$$

where $H(f_{dith})$ is the attenuation of the output LC filter at frequency f_{dith}.

The LC filter has a cutoff frequency at $f_c = 1/2\pi\sqrt{LC_{out}}$ after which it rolls off at -40 dB/dec. A real capacitor has finite effective series resistance (R_{ERS}) which causes a zero in the filter characteristic at frequency $f_z = 1/2\pi R_{ERS} C_{out}$, changing the rolloff to -20 dB/dec. Thus

$$H(f) \approx \left(\frac{f_c}{f}\right)^2 \qquad \text{for } f_c < f < f_z, \tag{17}$$

and

$$H(f) \approx \left(\frac{f_c}{f_z}\right)^2 \frac{f_z}{f} = \frac{f_c^2}{f_z f} \qquad \text{for } f_c < f_z < f. \tag{18}$$

Substituting back in (16), we obtain upper bounds for the peak-to-peak output voltage ripple due to dither

$$v_{p\text{–}p,\,dith} \le \left(\frac{f_c}{f_{sw}}\right)^2 2^{2M}\,\frac{4}{\pi}\,\frac{V_{in}}{2^{N_{dpwm}}} \tag{19}$$

for $f_c < f_{dith} < f_z$, and

$$v_{p\text{–}p,\,dith} \le \frac{f_c^2}{f_z f_{sw}}\,2^M\,\frac{4}{\pi}\,\frac{V_{in}}{2^{N_{dpwm}}} \tag{20}$$

for $f_c < f_z < f_{dith}$.

Once the amplitude of the dither is known, a condition on how many bits of dither, M, can be used in a certain system can be developed. To ensure that the dither does not cause steady-state limit cycling, there should always be an effective DPWM level that completely fits into one ADC quantization bin, taking into account the dither ripple. With M-b dither, the effective DPWM quantization bin size is

$$\Delta V_{dpwm,\,eff} = V_{in}/2^{N_{dpwm,\,eff}} = V_{in}/2^{N_{dpwm}+M}. \tag{21}$$

Geometric considerations show that the case which allows for the smallest dither ripple amplitude is when the effective DPWM levels are located at one-half effective DPWM bin size from the center of the ADC bin (Fig. 11). Then the tolerable peak-to-peak dither ripple amplitude is bounded by

$$v_{p-p,\,dith} < \Delta V_{adc} - \Delta V_{dpwm,\,eff}. \tag{22}$$

Assuming that the ADC has resolution ΔN b coarser than the effective resolution of the DPWM module

$$N_{adc} = N_{dpwm,\,eff} - \Delta N = N_{dpwm} + M - \Delta N \tag{23}$$

the ADC bin size is

$$\Delta V_{adc} = V_{in}/2^{N_{adc}} = V_{in}/2^{N_{dpwm}+M-\Delta N}. \tag{24}$$

Substituting (21) and (24) in (22), we obtain

$$v_{p-p,\,dith} < V_{in}\left(2^{\Delta N}-1\right)/\,2^{N_{dpwm}+M}. \tag{25}$$

Combining (25) with (19) and (20) we obtain an upper bound on M

$$M < \frac{1}{3}\log_2\left[\frac{\pi}{4}\left(\frac{f_{sw}}{f_c}\right)^2\left(2^{\Delta N}-1\right)\right] \tag{26}$$

for $f_c < f_{dith} < f_z$, and

$$M < \frac{1}{2}\log_2\left[\frac{\pi}{4}\,\frac{f_z f_{sw}}{f_c^2}\left(2^{\Delta N}-1\right)\right] \tag{27}$$

for $f_c < f_z < f_{dith}$.

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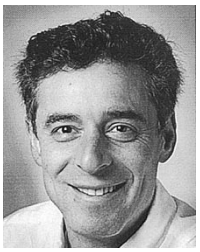

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