Low Conversion Ratio VRM Design

Angel V. Peterchev Seth R. Sanders
Department of Electrical Engineering and Computer Science
University of California, Berkeley

Abstract— **This paper discusses the design considerations for low conversion ratio voltage regulation modules (VRM's) for the next generation of microprocessors, focusing on the handling of large, high-slew-rate current transients. A converter topology which deploys an inductive clamp to handle the unloading transients, while operating at a modest switching frequency, low current ripple, and low power dissipation, is discussed. The clamp response is analyzed, and simulation results for a 1 MHz, 100 A, 12-to-1V VRM are presented.**

I. Introduction

THE projected specifications for next generation microprocessor VRM's [1] are summarized in Table I. The very low conversion ratio ($< 1/12$), the high load current and current slew rate, and the tight output regulation tolerance present a challenge to VRM design calling for new design solutions. Various modifications to the basic multi-phase buck converter have been proposed to address these demanding specifications, mostly using coupled-inductor topologies [2], [3], [4], [5]. The present paper introduces a converter topology which deploys an inductive output clamp to handle the unloading transients. Section II summarizes the theoretical analysis of the VRM current step response. Section III discusses considerations in VRM design. Section IV describes the inductive clamp topology, gives simulated results of its performance, and analyzes its power dissipation. Finally, the Appendix presents an analysis of the response requirements for a general output clamp.

II. VRM Transient Response

An output voltage transient of a buck VRM (Fig. 1) due to an increase in the load current I_o by ΔI_o is illustrated in Fig.2. The load current step will first cause an output voltage drop of magnitude $\Delta V_{o,R} = \Delta I_o R_{ESR}$ due to the effective series resistance (R_{ESR}) of the output capacitor[1]. Then, since the controller has non-zero response delay, V_o will continue to drop due to discharge of the output capacitor C_o. Let T_d be the delay of the controller response, *i.e.* the time between the instant a step in the load current has occurred and the resulting update of the duty cycle by the controller. Then the V_o drop due to the capacitive discharge will be $\Delta V_{o,C} = \Delta I_o T_d / C_o$. After time T_d, the controller responds to the load step by increasing the duty cycle, resulting in inductor current (I_L) increase at a rate of $dI_L/dt = V_L/L$, where, assuming saturated controller response, $V_L = V_{in} - V_o$. Consequently, V_o exhibits second-order behavior and eventually starts to increase. Reference [7] gives a condition on the total converter inductance L (all phase inductors in parallel) ensuring that V_o starts increasing immediately after I_L begins to ramp up,

$$L_{crit} = \tau_o V_L / \Delta I_o \tag{1}$$

where $\tau_o = R_{ESR} C_o$ is the time constant of the output capacitor, which is approximately constant for a particular capacitor technology.

The unloading current transient (a decrease of I_o by ΔI_o) is exactly analogous to the loading transient discussed above, with $V_L = -V_o$.

More discussions of VRM transient response can be found in [7], [8], [9], [10], [11].

[1] Here, for clarity, we are omitting the initial V_o drop due to the series inductance of the output capacitor. Recent research [6] has developed an advanced capacitor model for power applications and has indicated that the capacitor series inductance can be greatly reduced with proper capacitor packaging and power train layout.

TABLE I
NEXT GENERATION MICROPROCESSOR VRM SPECIFICATIONS *

V_{in}	input voltage	> 12 V
V_{ref}	reference voltage	< 1 V
$\Delta V_{o,max}$	regulation tolerance	< 50 mV
$I_{o,max}$	load current	> 100 A
dI_o/dt	current slew rate	> 350 A/μs
T_d	regulator response time	< 200 ns

(*) Source: reference [1]

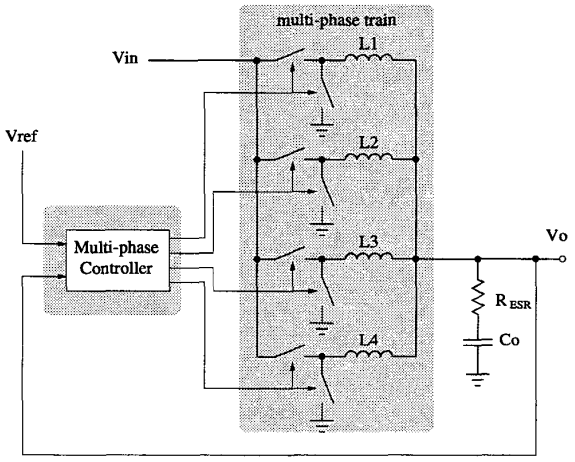

Fig. 1. Four-phase VRM.

0-7803-7262-X/02/$10.00 © 2002 IEEE.

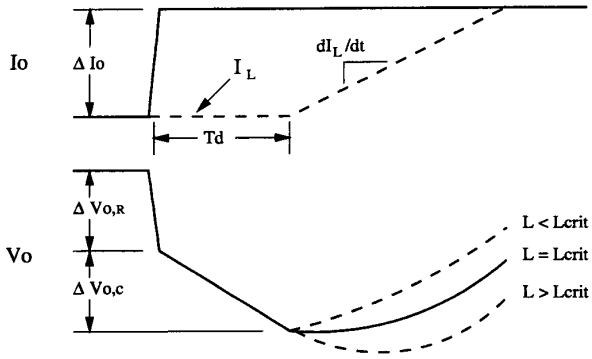

Fig. 2. Transient response of a buck VRM due to load current step.

TABLE II

CONSTRAINTS RESULTING FROM THE SPECIFICATIONS IN TABLE I

assuming ceramic output capacitors with $\tau_o = 0.8\mu s$

$L_{crit,load}$	critical induct. for loading step	88 nH
$L_{crit,unload}$	critical induct. for unloading step	8 nH
R_{ref}	closed-loop output impedance	$< 0.5\ m\Omega$

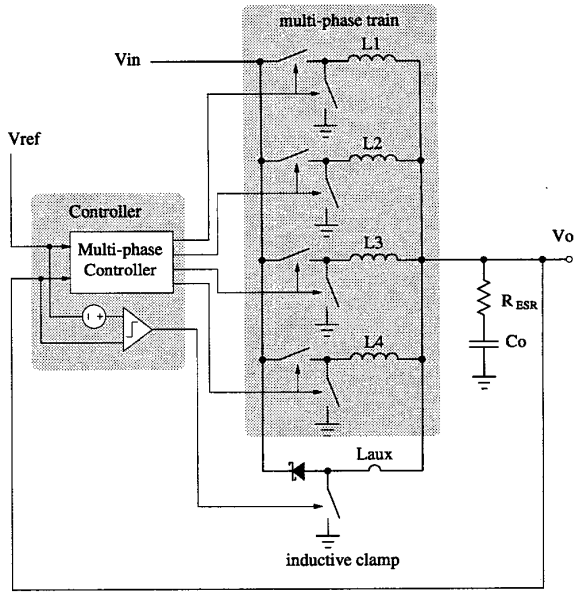

Fig. 3. Four-phase VRM with inductive clamp to ground.

III. VRM DESIGN

From the above analysis it can be seen that provided $L < L_{crit}$, output impedance control [8] can be used to position the output voltage V_o at $V_{ref} - R_{ref} I_o$, where V_{ref} is the reference voltage, and R_{ref} is the targeted closed-loop output impedance of the converter [7],

$$R_{ref} = R_{ESR}\,(1 + T_d/\tau_o)\,. \tag{2}$$

The desired R_{ref} can be calculated from the parameters in Table I,

$$R_{ref} < \Delta V_{o,max}/\Delta I_{o,max} \tag{3}$$

where $\Delta V_{o,max}$ is the output regulation tolerance, and $\Delta I_{o,max}$ is the maximum load current step (for this calculation we can assume $\Delta I_{o,max} \approx I_{o,max}$).

Returning to (1), for a loading current step, the critical inductance is

$$L_{crit,load} = \tau_o(1 - D)V_{in}/\Delta I_o, \tag{4}$$

while for an unloading current step it is

$$L_{crit,unload} = \tau_o D V_{in}/\Delta I_o. \tag{5}$$

Clearly for low conversion ratios, *i.e.* low values of D, $L_{crit,unload}$ is much smaller than $L_{crit,load}$. For example, with $D = 1/12$ there is an order of magnitude difference (see Table II). By definition L_{crit} is an upper bound for the converter inductance value which allows V_o to start increasing immediately after I_L begins to ramp up. If the converter presents the same inductance for both loading and unloading transients, the converter inductance is constrained by the smaller of $L_{crit,load}$ and $L_{crit,unload}$. Thus for low conversion ratios L is constrained by $L_{crit,unload}$ resulting in a very low value of L. The relation for the current ripple in each phase of the converter

$$\Delta I_{Lp-p} = V_{in}(1 - D)D/f_{sw}L_i, \quad \text{for } L_i = L_{1-4} \tag{6}$$

indicates that a low value of L would imply either a high current ripple, resulting in increased conduction losses, or the need to operate at high switching frequency (f_{sw}), resulting in high switching losses [1]. For example, a four-phase buck converter designed to meet the specifications in Table I with $L_i = 4L_{crit,unload}$, will have inductor current ripple of 29 A at 1 MHz. Thus, if the phase inductors are chosen based on $L_{crit,unload}$, switching frequencies in the 3–5 MHz range would be required to attain high efficiency.

IV. VRM TOPOLOGY

A topology which can handle fast current transients at low conversion ratios and modest steady-state switching frequencies, while maintaining low inductor current ripple, is presented in Fig. 3. It consists of a 4-phase buck converter complemented with an additional low value inductor L_{aux} which can be switched to ground during large unloading transients. The inductor values are selected so that,

$$L_i/4 < L_{crit,load} \tag{7}$$

and

$$L_{aux} \parallel L_i/4 < L_{crit,unload}. \tag{8}$$

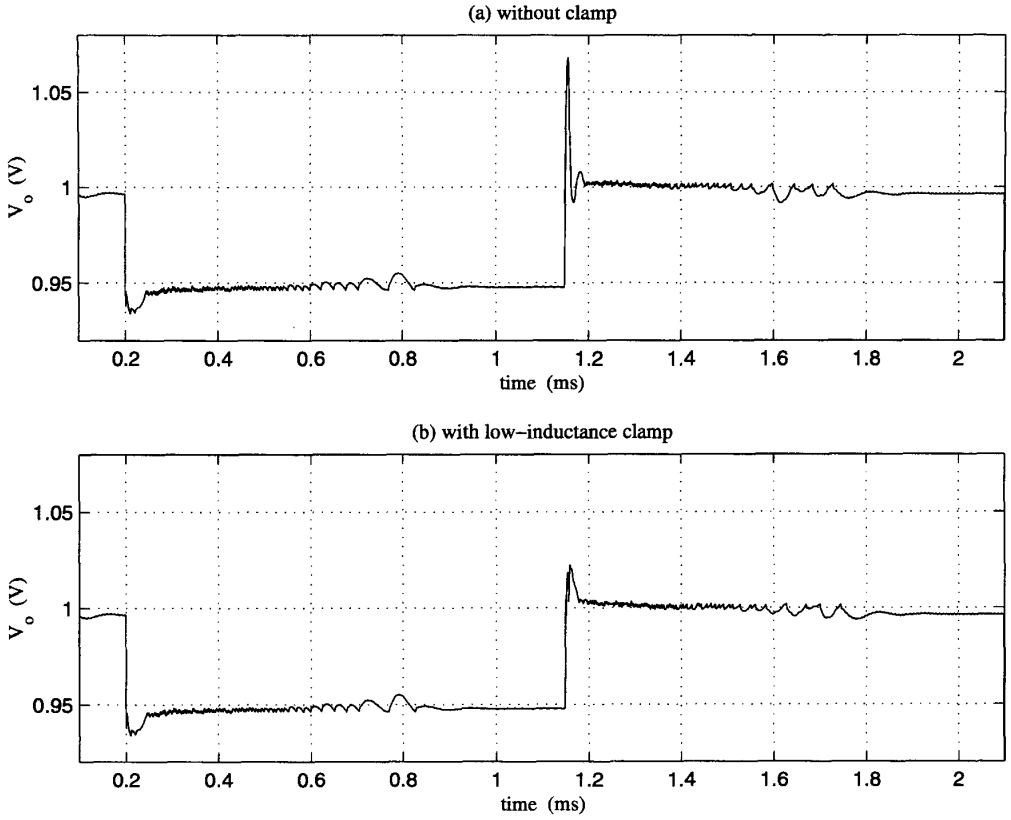

Fig. 4. Simulation of 4-phase buck converter transient response under a load current step $\Delta I_o = 100$A. $V_{in} = 12$V, $V_{ref} = 1$V, $f_{sw} = 1$MHz.

Thus, for large unloading transients the converter inductance is lower than its steady state value.

It was calculated in Table II that for the specified VRM requirements, $L_{crit,unload} = 8$ nH is on the order of lead and PCB trace inductances. Since $L_{crit,unload}$ has a very low value, some authors have proposed using a resistive output clamp implemented with a single MOSFET [12].

Parameters for a VRM design based on the considerations and topology discussed above are presented in Table III. The parameter values indicate that the use of the inductive clamp topology allows for a design operating at a modest f_{sw} = 1MHz, while having a low phase current ripple of ΔI_{Lp-p} = 3.2A, and using ceramic output capacitors.

A. VRM Simulation

Fig. 4 shows simulation results for the prototype in Table III under a 100 A transient. The converter is controlled by a digital controller [7], [13], with quantization resolution of 11.7 mV (10 bits over 12 V). The controlled quantity (V_o') is a combination of V_o and the total inductor current, scaled to yield an output impedance of about $R_{ref} = 0.44\ m\Omega$. If V_o' is close to V_{ref} then conventional PID PWM control is used. If V_o' is more than two quantization bins *above* V_{ref}, all phase inductors and the clamp inductor (L_{aux}) are switched to ground to prevent large overshoot of V_o. If, on the other hand, V_o' is more than four quantization bins *below* V_{ref}, all phase inductors are switched to V_{in} to avoid a large V_o undershoot. Quantity V_o' is sampled at $f_{s,cl} = 4$ MHz to ensure fast control action. This control strategy achieves fast saturated response of the converter during large load transients.

As Fig. 4 indicates, if clamping is not used the unloading transient produces a large overshoot, despite the saturated response of the phase inductors, since $L \gg L_{crit}$ (hereafter L_{crit} implies $L_{crit,unload}$). When the proposed low-inductance clamp is added, the unloading overshoot is substantially reduced, becoming comparable in size to the loading undershoot. The simulation thus confirms the theoretical expectations for the impact of the critical inductance value on the output voltage regulation.

TABLE III

PROTOTYPE VRM PARAMETERS

V_{ref}	reference voltage	1 V
V_{in}	input voltage	12 V
I_o	max load current	100 A
N_ϕ	number of phases	4
f_{sw}	switching frequency	1 MHz
$f_{s,cl}$	clamp sampling frequency	4 MHz
T_d	controller delay	200 ns
L_i	phase inductors	290 nH
L_{aux}	clamp inductor	8 nH
C_o	output capacitance	3.2 mF (ceramic)
R_{ESR}	output capacitor ESR	0.3 $m\Omega$
R_{ref}	closed-loop output impedance	0.44 $m\Omega$
N_{adc}	effective ADC resolution	10 bit
N_{dpwm}	effective DPWM resolution	7 bit (hardware) + 4 bit (dither)

B. Clamp Power Dissipation

The purpose of the clamp in the proposed VRM topology is to absorb energy from the four phase inductors during fast unloading transients, and therefore a theoretical understanding of its behavior and power dissipation is necessary. In order to ensure proper output impedance regulation during unloading transients, the energy absorbed by the clamp is approximately (see Appendix)

$$E_{cl} \approx (L/2 - L_{crit})\Delta I_o^2, \quad \text{for } L \gg L_{crit}. \tag{9}$$

assuming saturated response of the main inductors. The inductive clamp is essentially a boost converter transferring energy from V_o to V_{in}. Thus, ideally, it can recover all the energy absorbed during an unloading transient by returning it to V_{in}. In practice this clamping boost converter has efficiency η_{cl}, thus there is a power loss associated with the clamping,

$$P_{cl} = (1 - \eta_{cl})E_{cl} f_{load} \tag{10}$$

where f_{load} is the frequency of the load transients associated with E_{cl}. For the design in Table III, assuming a fully dissipative clamp ($\eta_{cl} = 0$) and full-scale current transients at a frequency of f_{load} = 5kHz, we obtain

$$P_{cl} \approx 1.4\,W \tag{11}$$

which is 1.4 % of the full load power of 100W.

V. Conclusion and Future Work

This paper discussed considerations for the design of low conversion ratio VRM's. The importance of the critical inductance value for tight regulation of the output voltage was emphasized. This analysis led to the introduction of a low-inductance clamp topology capable of handling large load transients with tight output regulation at moderate switching frequency, and low current ripple and power dissipation. A simulation illustrating the clamp effect on the output voltage was presented. Finally, an experimental converter incorporating the proposed topology is currently under development.

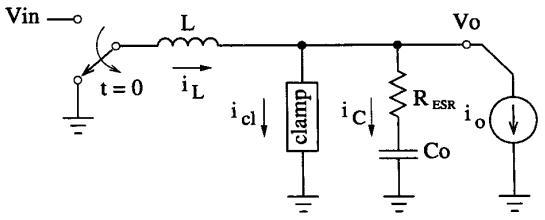

Fig. 5. Model of buck converter with clamp for transient analysis.

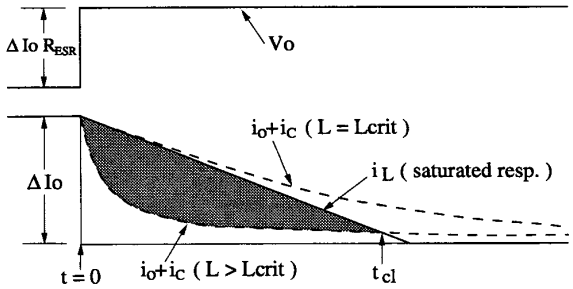

Fig. 6. Response of the converter in Fig. 5 after an unloading current step of magnitude ΔI_o at time $t = 0$.

Appendix

Clamp Response Analysis

A simple model of a buck converter with a clamp is shown in Fig. 5. For a multi-phase topology, inductor L corresponds to all the phase inductors in parallel. Fig. 6 shows the behavior of the converter after an unloading current step of magnitude ΔI_o at time $t = 0$. We assume that the converter is controlled to have output impedance equal to the capacitor ESR, thus the transient produces a V_o step of $\Delta I_o R_{ESR}$. If the inductor has saturated response, its current after the load step is given by

$$i_L = I_o - V_o t/L, \tag{12}$$

where I_o is the output current before the load step. Saturated unloading response of the inductor corresponds to the fastest rate at which its current can decrease. Meanwhile, the current flowing into the output capacitor is

$$i_C = \Delta I_o e^{-t/\tau_o}, \tag{13}$$

where $\tau_o = R_{ESR}C_o$, and the load current is

$$i_o = I_o - \Delta I_o. \tag{14}$$

As illustrated in Fig. 6, if $L \leq L_{crit}$, the current sunk from the output node ($i_o + i_C$) is always more than the inductor current corresponding to a saturated response. In this case the inductor current i_L can be pulsed by the control circuitry so that it follows $i_o + i_C$, and thus V_o can indeed follow the step depicted in the figure. However, if $L > L_{crit}$, even with saturated response the inductor supplies more current to the output

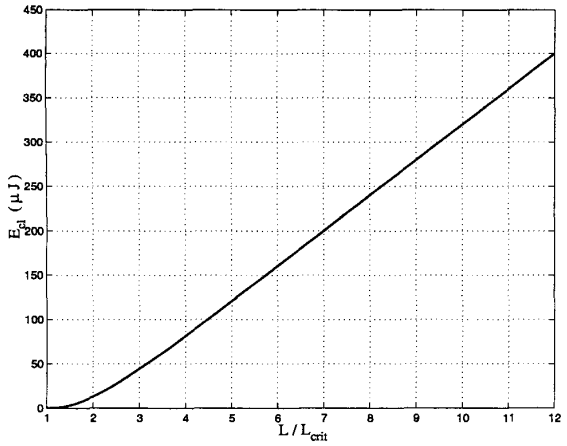

Fig. 7. Energy that has to be absorbed by the clamp during a full unloading step.

node than the load and the capacitor can sink, thus there is an "excess" of energy which will result in a V_o overshoot as indicated in Fig. 4(a). The role of the output clamp is to absorb this excess energy during the transient, and either dissipate it, or recycle it, for example by delivering it back to the converter input. The current that the clamp has to sink is thus

$$\begin{aligned} i_{cl} =& i_L - (i_o + i_C) \\ =& \Delta I_o(1 - e^{-t/\tau_o}) - V_o t/L, \quad \text{for } t \in (0, t_{cl}) \end{aligned} \tag{15}$$

where t_{cl} is the non-zero solution of

$$i_{cl}(t) = 0. \tag{16}$$

The energy that has to be absorbed by the clamp is then

$$\begin{aligned} E_{cl} &= \int_0^{t_{cl}} V_o i_{cl}(t) dt \\ &= V_o \left[\Delta I_o t_{cl} - \Delta I_o \tau_o (1 - e^{-t_{cl}/\tau_o}) - \frac{V_o}{2L} t_{cl}^2 \right], \end{aligned} \tag{17}$$

which is proportional to the shaded area in Fig. 6. Since the solution to (16) is transcendental, we cannot obtain an analytic expression for t_{cl}. We have therefore solved (17) numerically and plotted the result in Fig. 7 for a range of L/L_{crit}. It should be noted that for $L \gg L_{crit}$ we have $t_{cl} \gg \tau_o$, thus

$$t_{cl} \approx \Delta I_o L / V_o \tag{18}$$

leading to a simple approximate expression for the clamp energy

$$\begin{aligned} E_{cl} &\approx L \Delta I_o^2/2 - V_o \Delta I_o \tau_o, \quad \text{for } L \gg L_{crit} \\ &= (L/2 - L_{crit}) \Delta I_o^2. \end{aligned} \tag{19}$$

Finally, note that the above analysis of the energy that a clamp has to absorb is general, and thus holds for *any* kind of clamp (resistive, inductive, *etc.*).

References

[1] B. Rose, "Voltage regulator technology requirements", in *4th Annual Intel Technology Symposium*, Seattle, USA, Sept. 2000.

[2] P.-L. Wong, P. Xu, P. Yang, and F. C. Lee, "Performance improvements of interleaving VRMs with coupling inductors", *IEEE Trans. on Power Electron.*, vol. 16, no. 4, pp. 499–507, July 2001.

[3] J. Li, C. R. Sullivan, and A. Schultz, "Coupled-inductor optimization for fast-response low-voltage DC-DC converters", in *Proc. IEEE Applied Power Electron. Conf.*, 2002, vol. 2, pp. 817–23.

[4] P. Xu, J. Wei, K. Yao, Y. Meng, and F. C. Lee, "Investigation of candidate topologies for 12V VRM", in *Proc. IEEE Applied Power Electron. Conf.*, 2002, vol. 2, pp. 686–92.

[5] K. Yao, F. C. Lee, Y. Meng, and J. Wei, "Tapped-inductor buck converters with a lossless clamp circuit", in *Proc. IEEE Applied Power Electron. Conf.*, 2002, vol. 2, pp. 693–8.

[6] C. R. Sullivan and A. M. Kern, "Capacitors with fast current switching require distributed models", in *Proc. IEEE Power Electron. Spec. Conf.*, 2001, vol. 3, pp. 1497–503.

[7] J. Xiao, A. V. Peterchev, and S. R. Sanders, "Architecture and IC implementation of a digital VRM controller", in *Proc. IEEE Power Electron. Spec. Conf.*, 2001, vol. 1, pp. 38–47.

[8] R. Redl, B. P. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter", in *Proc. IEEE Applied Power Electron. Conf.*, 1999, vol. 1, pp. 170–6.

[9] P.-L. Wong, F. C. Lee, X. Zhou, and J. Chen, "Voltage regulation modules (VRM) transient modeling and analysis", in *Proc. IEEE Industry Appl. Conf.*, 1999, vol. 3, pp. 1669–76.

[10] P.-L. Wong, F. C. Lee, P. Xu, and K. Yao, "Critical inductance in voltage regulation modules", in *Proc. IEEE Applied Power Electron. Conf.*, 2002, vol. 1, pp. 203–9.

[11] P.-L. Wong and F. C. Lee, "Switching action delays in voltage regulation modules", in *Proc. IEEE Applied Power Electron. Conf.*, 2002, vol. 2, pp. 675–8.

[12] A. Consoli, F. Gennaro, G. Giannetto, and A. Testa, "A new VRM topology for next generation microprocessors", in *Proc. IEEE Power Electron. Spec. Conf.*, 2001, vol. 1, pp. 339–44.

[13] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters", in *Proc. IEEE Power Electron. Spec. Conf.*, 2001, vol. 2, pp. 465–71.