An Electrostatic Microresonant Power Conversion Device *

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Abstract

An electrostatically driven microstructure suitable for use in a monolithic resonant DC-DC converter is presented. The device can be manufactured using existing integrated circuit processing techniques, permitting integration with switching devices in Silicon. The mechanical resonant structure is used in place of an LC tank and in place of a transformer, avoiding the complexity of manufacturing integrated magnetic clements. A monolithic resonant converter using this technology offering high power density is proposed. The device can potentially be driven in a zero-voltage-switched (ZVS) mode, scaling well to higher operating frequencies.

1 Introduction

A large proportion of present power electronics research focuses on miniaturization of power converters. The goal is to maximize efficiency and power density. Power densities of approximately $50W/cm^3$ have been reported in the literature for discrete switch-mode supplies [1]. Efforts at miniaturizing power converters often are hampered by the difficulty of integrating magnetic components with other circuit elements using existing processing technology.

One interesting approach proposed by Smit et al. [2] and Stielau et al. [3] integrates an inductor with a capacitor using microstrip theory. This method permits the manufacture of integrated LC structures suitable for power conversion applications. Apparently, these devices are not compatible with existing planar integrated circuit technology. The paper of Yachi et al. [4] outlines a planar microtransformer manufactured by dry process techniques using Cu, Ta, and CoZrRe as the magnetic material. This process apparently permits integration of the microtransformer with power semiconductor devices. The microtransformer is used as a component in a discrete 36 mW output forward converter operating at 32Mhz. A problem with this design is the large series resistance of the device, apparently caused by contact resistance between the two separate metallization steps needed to define the coil. Another approach for constructing integrated power supplies has been based on the methodology of switched capacitor circuits [5, 6, 7]. The limitations of this are in the lack of isolation and in the inherent switching losses.

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The approach in our work is to replace the LC tank in a resonant converter with a micromechanical device, thereby avoiding the fabrication of magnetic components. Isolation and energy transfer between primary and secondary ports is achieved with an insulating mechanical coupling. Our device is manufactured by planar techniques using readily available Silicon processing equipment. This permits integration of the device with semiconductor devices to yield a monolithic power supply.

2 Principles of Operation

The device, shown schematically in Figure 1a), consists in principle of two mechanically coupled variable capacitors mounted on springs as shown in Figure 1b). The dark areas are immobile, while the shaded region represents the mechanical coupling between the capacitors. In our design, a fixed beam acts to provide the restoring spring force, the driving force is provided by an applied voltage between the primary mobile plate and the bottom electrode (C1 in Figure 1), and the mechanical coupling is provided by a strip of silicon nitride. The device is biased with a DC voltage through a high impedance and is excited near resonance by an active bridge circuit as shown in Figure 2. A coupling capacitor is needed to block the DC bias voltage. The DC bias could be supplied across a substrate capacitor by a solid-state voltage multiplier circuit. The secondary side is a mirror image of the primary, but with the active switch devices replaced by diodes, and the source replaced by a load.

Energy is transferred from the primary to the secondary by the mechanical coupling within the structure. A basic approach is to run the device near the resonant frequency, providing the greatest mechanical oscillations. The total power handling capacity of the device can be approximated by

$$\frac{P_m}{A} = f_o \frac{\Delta C}{A}(1/2)[(V_b + V_s/2)^2 - (V_b - V_s/2)^2] = f_o \frac{\Delta C}{A} V_b V_s \quad (1)$$

in watts per unit area. Here, f_o is the operating frequency of the device (selected near the resonant frequency), and $\frac{\Delta C}{A}$ is the capacitance change per unit area of wafer surface. A justification for the estimate (1) is as follows. If the maximum voltage $V_b + V_s/2$ is applied while the plates are moving toward each other, the energy absorbed on the primary side is $(1/2)\Delta C(V_b+V_s/2)^2$. Then, if the minimum voltage $V_b - V_s/2$ is applied while the plates are moving apart, the energy re-

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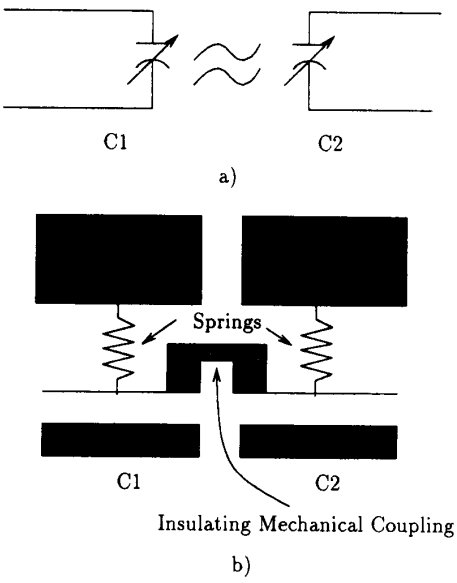

Figure 1: Illustration of Mechanical Capacitive Structure

turned is $(1/2)\Delta C(V_b - V_s/2)^2$. The estimate (1) of the power density includes factors for the frequency f_o and the total area A.

Based on preliminary results, we can estimate power densities for structures designed to operate at various frequencies. We conservatively set $V_b = 100V$, $V_s = 10V$, and estimate $\Delta C = \frac{1}{5}C_0$ where C_0 is the capacitance of the structure with no DC bias for a 1 μm gap. The power densities of the devices are then estimated as shown in the following table.

Operating Frequency	1Mhz	10Mhz	30Mhz	50Mhz
Power Density (W/cm^2)	2	20	60	100

The proposed converter should scale well to higher frequencies, since it permits zero-voltage-switching (ZVS) similar to that described in [8, 9] when operating above resonance. Naturally, the high frequency hysteresis and eddy current losses associated with magnetic components are avoided. By sequencing the gate drives for the active bridge as indicated in Figure 3, zero-voltage-switching can be effected. In particular, the top transistor Q1 is switched off while the plates of the capacitor are still moving toward each other, and hence the current i into the capacitor is positive. If the amplitude of the mechanical oscillation is large enough, the voltage on the capacitor (and associated parasitic capacitance) is pulled down until the bottom diode D2 turns on. Then, the bottom transistor Q2 can be turned on at zero voltage. Transistor Q2

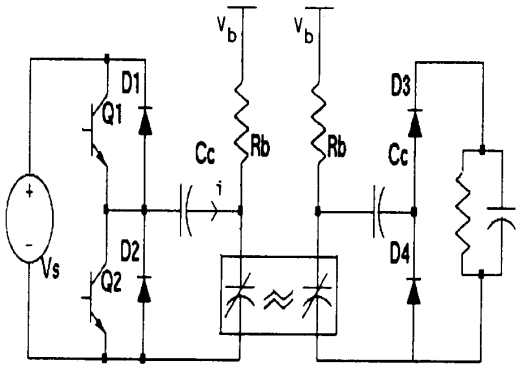

Figure 2: Example of Power Converter Employing Resonant Device.

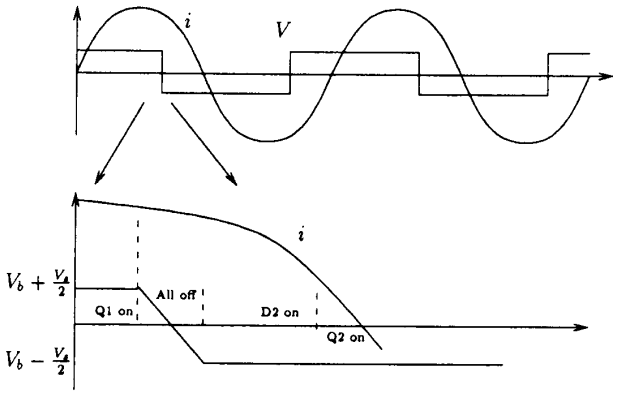

Figure 3: Typical Zero Voltage Switching Waveforms

is held on until the motion of the plates reverses. The lossless turn-off of Q2 and turn-on of Q1 occurs in a symmetric fashion. The secondary can also exhibit zero-voltage-switching as in a series resonant DC-DC converter.

The nominal voltage transfer ratio from primary to secondary can be set by the DC bias on either side of the structure and the relative areas of the coupled resonant capacitors. Power flow can be controlled by frequency variation as in a series resonant converter, or more simply by controlling the DC bias voltage.

A completed device made from polysilicon with silicon nitride mechanical coupling is shown in Figure 5. A section of the corresponding layout description is shown in Figure 4. Alternating plates correspond to capacitors C1 and C2 in Figure 1a). Motion is in the vertical direction, with one electrode of the capacitor defined by the top polysilicon layer,

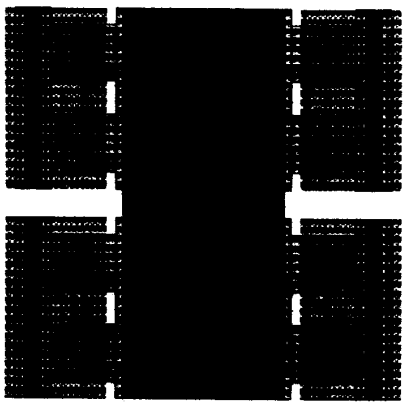

Figure 4: Layout of Fabricated Device. Top section is primary, bottom is secondary. Approximate dimensions of each plate (dark area) are 50μm (w)x30μm (l).

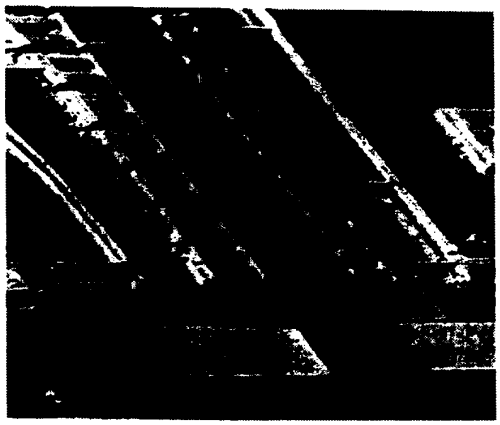

Figure 5: Scanning Electon Micrograph of Device with both Primary and Secondary Ports. Height of the polysilicon plate is approximately 2.4μum. The vertical space between polysilicon and substrate is approximately 1μm. Primary and secondary port bus lines run along the left and right side of the device respectively.

and another by the lower polysilicon layer. The lines running alongside the devices electrically interconnect the individual mechanical devices. Note that the strategy in building a high power converter is to parallel many of these devices. The structure in Figure 5 consists of a parallel connection of these devices in one dimension, and Figure 6 shows a scheme for connecting large numbers of these devices in two dimensions.

Device Modeling With thick plates, the device with only a primary can be modeled as a parallel connection of fixed-fixed beams, yielding the following governing equations

$$\begin{aligned} \dot{q} &= C\dot{V} + \tfrac{\partial C}{\partial x}\dot{x}V \\ m\ddot{x} &= -kx - b\dot{x} + F_{mech} \\ F_{mech} &= \tfrac{1}{2}\tfrac{\partial C}{\partial x}V^2 \end{aligned} \tag{2}$$

where x is the position of the plate with $x = 0$ corresponding to the static position with no bias, $C(x) = \epsilon_0 \frac{A}{s-x}$ is the instantaneous capacitance, s is the static separation of the plates with no DC bias, m is the mass, k is the spring constant, b is the damping, q is the charge on the plates, and V is the voltage. From elementary beam theory the spring constant is found to be

$$k = \frac{16Ewh^3}{l^3}$$

where h, w, and l are the height, width, and total length of the support beam respectively, and E is the Young's modulus of polysilicon. By solving equations (2) for an equilibrium, we find the static deflection as a function of the applied DC bias. Note that there is a critical pull-in voltage above which the attractive force overcomes the restoring spring force, thereby pulling the plates together. This is given by

$$V_{pi} = \sqrt{\frac{8ks^3}{27\epsilon a_p}} \tag{3}$$

where a_p is the area of the plate. Figure 7 plots the normalized deflection of the plate ($\frac{x_0}{s}$) versus the normalized voltage ($\frac{V_0}{V_{pi}}$), as determined from (2) to be

$$\frac{V_0}{V_{pi}} = (1 - \frac{x_0}{s})\sqrt{\frac{27x_0}{4s}}. \tag{4}$$

It is instructive to linearize the nonlinear mechanical equation in (2) around the equilibrium point x_0 corresponding to a bias voltage V_0, giving

$$\begin{aligned} m\ddot{\delta x} + b\dot{\delta x} + K_e\delta x &= \tfrac{\partial F_{mech}}{\partial V}\Big|_{x_0}\delta V \\ K_e &= k - \tfrac{\partial F_{mech}}{\partial x}\Big|_{x_0} \end{aligned} \tag{5}$$

From (5), it is evident that an increase in DC bias will result in a decrease in the effective spring constant [10], thereby resulting in a decrease of the resonant frequency. Figure 8 summarizes the relationship between normalized resonant frequency, normalized deflection and normalized DC voltage.

3 Process

Devices have been fabricated using CMOS-level clean furnaces and etch procedures. The process is similar in principle to that described in [11] where the etch of a sacrificial phosphosilicate glass (PSG) layer releases polysilicon structures.

In the first step, a 5000A layer of in-situ doped polysilicon is deposited and patterned on a passivated substrate. Next,

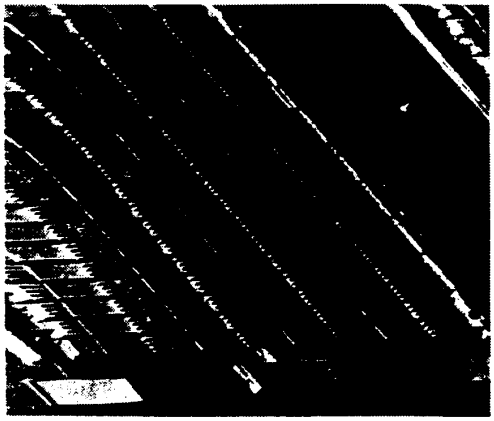

Figure 6: 2-Dimesional Interconnection of Devices with both Primary and Secondary Ports

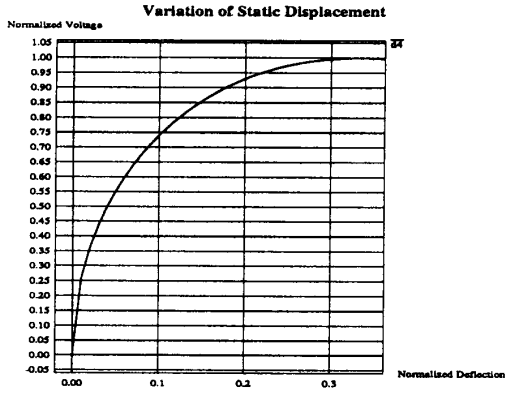

Figure 7: Plot of normalized steady-state voltage vs normalized deflection

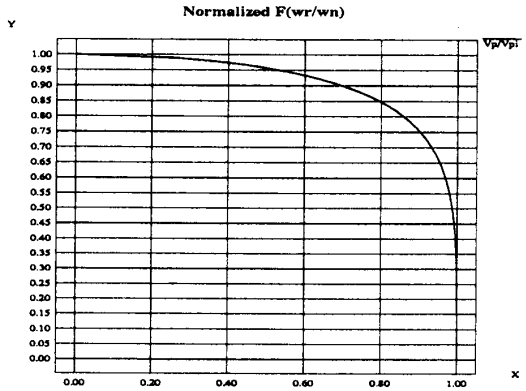

Figure 8: Plot of normalized frequency vs. normalized voltage

a 2.5 μm PSG layer is deposited and patterned (Figure 9a). This layer offsets the supports from the substrate relative to the plate, thereby minimizing parasitic capacitance.

Next a blanket 3000A insulating layer of low stress silicon nitride followed by 1μm of PSG is deposited. The PSG is then patterned to define the fixed points for the springs (Figure 9b). The nitride ensures that in the event that the two plates contact a short circuit current will not destroy the device.

Then, the 2.4μm structural layer of undoped polysilicon is deposited, followed by a doping PSG layer. The resulting PSG/poly/PSG sandwich is then annealed at 950 C in a nitrogen ambient for one and a half hours. In addition to doping the polysilicon, this step decreases the stress gradients in the polysilicon. The top oxide is removed in 5:1 buffered hydrofluoric acid (BHF), and the polysilicon is patterned twice; firstly to define the general shape of the upper layer, and secondly to define the thin sections of the upper polysilicon (Figure 9c).

Finally, the bottom layer of nitride is exposed by removing some of the sacrificial oxide in a timed 5:1 BHF etch. This is then patterned to expose contacts to the bottom layer of poly, and then the remainder of the sacrificial oxide is removed in a timed 49% HF etch.

For test devices with a secondary port another 4000A layer of nitride is deposited and patterned to couple adjacent sections of mobile polysilicon.

4 Results and Discussion

Structures designed to have a resonant frequency of approximately 1MHz have been fabricated using the process outlined above. The area of each test device is approximately 0.5 mm^2. For a device with only a primary side resonant capacitor, sharp resonant behavior is attained in vacuum. Figure 10 shows measured device current and voltage excitation. With no DC bias, the behavior is that of a capacitor of approximately 15pF. With a 50V DC bias, a significant component of current due to the mechanical resonance is exhibited. With only a 4V excitation, the resonant current is on the order of 1mA. With these numbers, a power handling capability of 8mW/mm^2 or 0.8W/cm^2 is attained. With a larger voltage excitation, greater power handling capacity could be measured. To exhibit the high-Q resonant behavior of the device, Figure 11 shows a measured small-signal admittance plot.

In Section 2 we derived an expression for V_{pi}, an upper bound on the DC bias voltage. It is necessary to ensure that other mechanisms do not damage the devices. In particular it is necessary to investigate the breakdown characteristics of PSG, nitride and air with respect to the small dimensions in the device.

Typical spacing between the plates of the device is on the order of micrometers, with approximately 5 μm between pri-

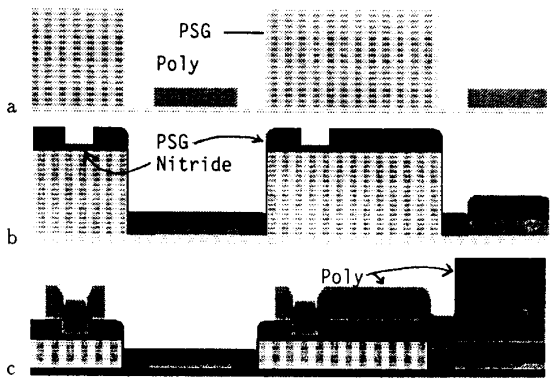

Figure 9: Cross-section view of device a) after bottom poly and oxide deposition, b) nitride and PSG defining interelectrode spacing, c) after final poly layer deposition- thicker section of poly is emphasized in black. Note that vertical scale is greatly exaggerated in these drawings.

mary and secondary ports. These distances are well below the Paschen curve minimum point at atmospheric pressure. A further decrease in pressure will only increase the breakdown field. Hence, breakdown of air is not expected to be a problem.

Published data on breakdown of stoichiometric nitride thin films gives a critical breakdown field of $5-10MV/cm$ [12] depending on deposition conditions. As our nitride film is non-stoichiometric we conducted breakdown tests with a 60Hz voltage source on a 2000A nitride film. The critical field was found to be 8MV/cm, well in agreement with the data. It should be noted that the nitride did not leak appreciable current for fields below 80% of the breakdown.

Published breakdown fields for oxide are typically in the range of $3-10MV/cm$ [12], however similar figures for PSG are less readily availabe. We conducted similar breakdown tests on PSG layers of thickness $\approx 2\mu$m. We found our PSG to break down at approximately 1MV/cm, somewhat lower than that reported in the literature for oxide, presumably because of the doping of our PSG. The result is that the primary to secondary breakdown voltage for the device of Figures 4 and 5 was measured at approximately 300V. The breakdown occurred in the passivation oxide. Future devices will use nitride passivation, and hence should exhibit much larger breakdown voltages.

5 Conclusion

We have presented a power conversion device compatible with standard silicon processing techniques which does not require magnetic components. The device has good isolation and scales well to higher frequencies, showing promise as a building block for a monolithic power supply.

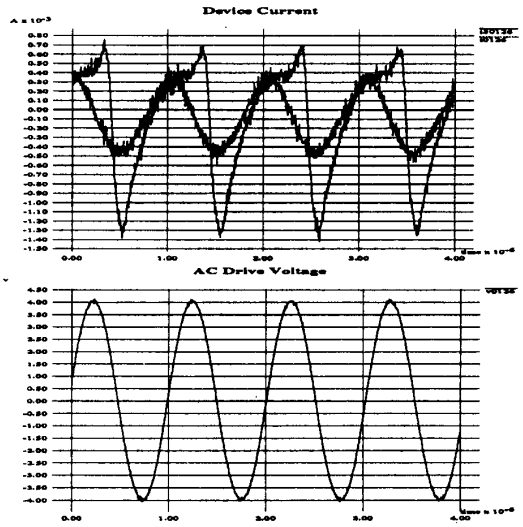

Figure 10: Measured Device current (in mA) and AC Voltage (in V) for Resonant (50V Bias) and Nonresonant (0V Bias) Excitation in vacuum. The units of Time are μS. The sinusoidal current waveform corresponds to nonresonant excitation.

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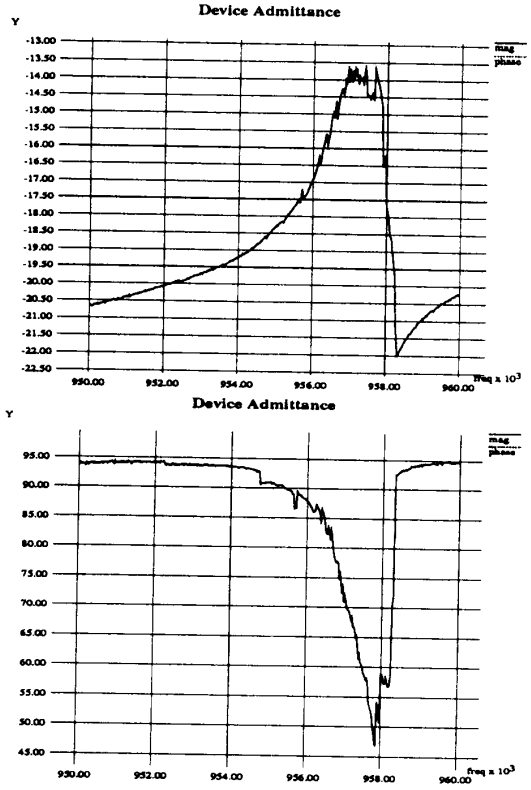

Figure 11: Graph of Device Admittance with 50V DC bias in vacuum. Top graph is magnitude, bottom is phase.

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