An Ultra-Low-Power Power Management IC for Energy-Scavenged Wireless Sensor Nodes

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***Abstract*– A power interface IC is designed and demonstrated to convert and manage power for a wireless tire pressure sensor node. The IC includes two switched-capacitor DC-DC converters to supply power to the various components of the sensor at their appropriate voltages. The design of the two integrated converters is discussed, including the optimization of capacitors and power transistors. The losses due to parasitic capacitances are analyzed. Two gate drive techniques are used to drive the gates of the floating triple-well transistors. A synchronous rectifier efficiently harvests energy from an electromagnetic shaker and control circuitry regulates the output voltage while minimizing power consumption. The two converters achieve efficiencies of approximately 84% while the synchronous rectifier achieves an efficiency of 88%.**

I. Introduction

Wireless Sensor Nodes (WSNs) are using less power and are becoming smaller as this technology matures. Scavenged-power sensor nodes are now a reality with modern processor, sensor and radio technology [1], [2]. The efficiency of the scavenger-battery-load power interface path, especially at low power, is critical to the performance of such a sensor node. A custom IC is designed in this work to perform scavenger-to-battery and battery-to-load power conversion, while meeting power and size constraints of the system.

II. Application Description

This paper describes a power interface integrated circuit for a wireless tire pressure sensor (TPS), running from energy scavenged from a magnetic shaker [1], [3]. Photos of the node and scavenger are shown in fig. 1, with dimensions indicated. The sensor node is a modular stack of 1 cm^2 printed circuit boards connected by elastomer connectors. Each board contains a single functional block of the system. The energy consumers, or loads, include a TI MSP430 microcontroller, an Infineon pressure and acceleration sensor, and a custom PicoRadio radio transmitter [4]. The microcontroller and sensor run at a minimum 2.1 V supply and the radio requires a precise 0.65 V supply. A small NiMH coin cell with a nominal capacity of 18 mAh is used as an energy buffer, although the use of a supercapacitor is also feasible. The electromagnetic shaker utilizes the rotation of the tire to generate energy to power the sensor.

WSNs often run at very low duty cycles to minimize power consumption. In the TPS application, tire pressure is measured once every six seconds. Power consumption for a single 14ms measurement/transmission period is shown in fig. 2. Each 14ms measurement/transmission cycle uses approximately 29 μJ, yielding peak powers of several mW. Node standby power is less than 1 μW resulting in a time-averaged power consumption of approximately 6 μW.

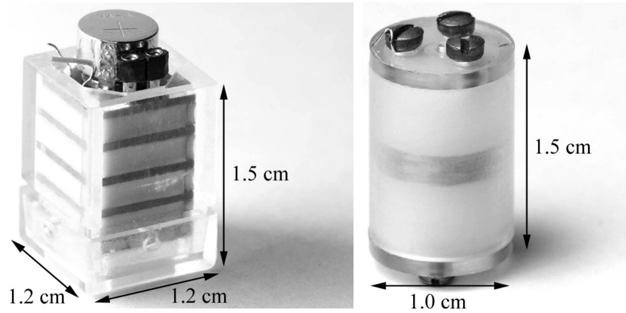

Fig. 1. Photos and dimensions of the PicoCube (left) and the shaker (right)

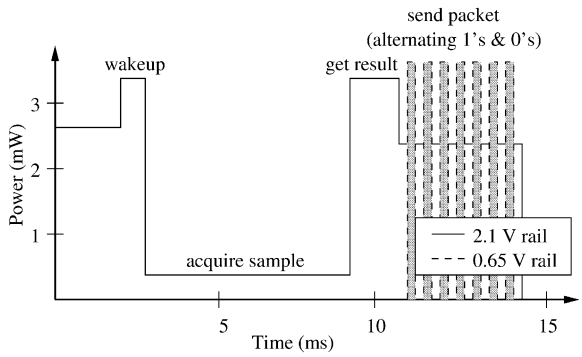

Fig. 2. Measurement and transmission power

The performance of a self-powered WSN is often defined by the sample rate or the number of samples per second the node can acquire and transmit. For a given fixed energy per packet, and a fixed average power supply (defined by the capabilities of the battery or energy scavenger), the sample rate is highly dependent on the efficiency of the power interface circuits. Since WSNs spend the vast majority of time in standby mode, power efficiency at microwatt levels is critical but often lacking in current solutions. This power interface IC aims to improve this efficiency.

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III. Converter Architecture

The architecture of the power interface IC is given in fig. 3. The synchronous rectifier interfaces the electromagnetic shaker (scavenger), which puts out a pulsed waveform, to the battery. Details about its use and implementation are in section VI. Two switched-capacitor power converters convert the battery voltage, nominally 1.2 V, to 2.1 V for the microcontroller and sensors and to 0.7 V to power the radio. The design of the power stages of these converters is detailed in section IV, while the gate drive techniques used are described in section V.

An ultra-low-power linear regulator is used as a post-regulator to more-precisely set the radio supply voltage to 0.65 V and to smooth the ripple from the switched-capacitor converter. This linear regulator is designed with an integrated switch to disable the regulator's output. When the output is disabled, the regulator's bias current is decreased substantially to reduce quiescent power. The enable transistor is located between the output capacitor and the load such that the output capacitor remains charged while the output is disabled. Thus, the energy stored in the capacitor is preserved and the turn-on transient response is shortened. Finally, a hysteretic feedback controller is used to regulate output voltage and switching frequency, and is described in section VII.

A number of analog blocks provide support to the power electronics by providing references and control signals. A self-biased current source (reference) supplies bias current to the chip via a current mirror. It is biased at 18 nA independent of V_{DD} and mildly dependent on temperature. An ultra-low-power sampled bandgap reference provides a reference voltage to both the converter feedback circuitry and the linear regulators. The design of this voltage reference is further described in section VIII.

The converter IC was implemented using a 0.13 μm CMOS process provided by STMicroelectronics. The nominal 1.2V working voltage matches the battery voltage perfectly, and the process provides 2.5 V transistors and high-density capacitors, the latter used in the switched-capacitor converters.

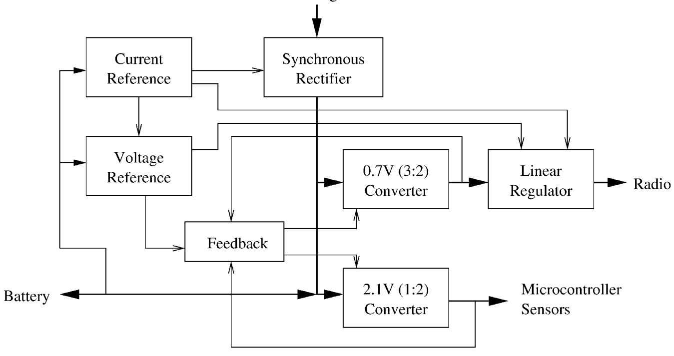

Fig. 3. Block diagram of the converter IC

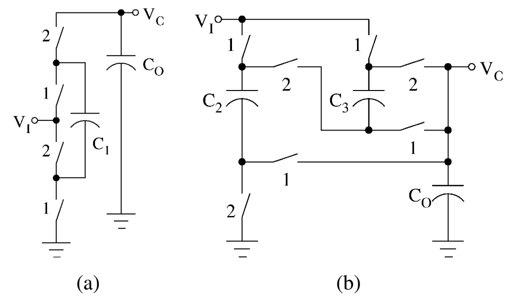

Fig. 4. Switch-level diagram of a) 1:2 converter, b) 3:2 converter

IV. Design of the Power Stages

Two independent switched-capacitor (SC) converters perform the power conversion between the battery and the loads. A 1:2 ratio converter, shown in fig. 4a, provides a doubled voltage for the microcontroller and sensors. The minimum supply voltage for these components is 2.1 V. A 3:2 ratio converter, shown in fig. 4b, provides a lower voltage (nominally 0.65V) to supply the radio.

The topologies are chosen to utilize the native transistors of the 0.13 μm CMOS process, even to generate the 2.1 V rail. The benefits and drawbacks of a number of SC converter topologies are described in reference [5]. All power switches are implemented using NMOS transistors to minimize die area and gating and parasitic losses. Section V addresses the level shifters and other circuitry required to drive these transistors.

The transistors, capacitors and converter switching frequency of each converter are adjusted to optimize efficiency while meeting constraints on output voltage and power. In previous work [5], [6], a method to optimize transistor and capacitor sizes in SC converters was developed. Those techniques are applied here to formulate a global optimization method. SC converters provide an ideal dc voltage conversion ratio under no load conditions. Voltage drop at the output can be associated with non-zero load current through the output-referred impedance of the converter [7]. Two factors determine this output impedance, as outlined below. An additional two parasitic-related factors contribute to the loss of an SC converter. Thus, converter loss is comprised of the following factors:

1) *SSL output impedance:* For periodic steady-state operation, the slow-switching-limit (SSL) output impedance incorporates the voltage drop at the output required to transfer the necessary charge from input to output during each period. The resistance of the power switches and interconnect are neglected for this calculation [5]. The SSL power loss represents the loss due to this series resistance, and is inversely proportional to capacitance and switching frequency.
2) *FSL output impedance:* At high switching frequencies, the switch and interconnect resistances dominate the converter output impedance. This limit is known as the fast-switching-limit (FSL) impedance. In this limit, capacitors are assumed to be large and their voltages con-

stant. The fast-switching-limit (FSL) output impedance is the weighted combination of the switch on-state resistances, and is independent of switching frequency. The FSL impedance is derived in [5].

3) *Capacitor bottom-plate loss:* This loss is due to charging and discharging the parasitic capacitance between the bottom plate of the flying capacitors and the substrate once per period. This loss is proportional to capacitor size and switching frequency.
4) *Switch parasitic loss:* This loss is due to the parasitic capacitances of the power switches, specifically the gate, drain and body-substrate capacitances. These capacitances are charged and discharged once per switching period. This loss is proportional to transistor size and switching frequency.

All four losses contribute additively to decrease efficiency, while the first two losses contribute to the equivalent output impedance of the converter. The converter is optimized to maximize efficiency while keeping the output impedance sufficiently low such that the required output voltage is maintained at maximum output current. A margin of error for process tolerances needs to be included as well.

To optimize the SC converters, the total capacitor area was constrained to a prescribed area, and the relative capacitor sizes within each converter adjusted by the optimization in [5]. Next, the capacitor area was divided between the two converters such that both would run at the same switching frequency (to allow for a single clock), while minimizing net loss. The two remaining variables are the switch area (for each converter) and the switching frequency. A numerical optimization was performed by evaluating efficiency and output impedance over a range of switching frequencies and switch areas.

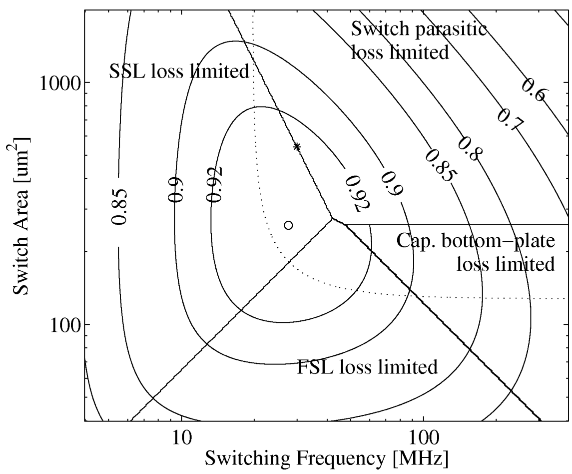

Fig. 5. Optimization contours of the 1:2 converter

Fig. 5 is a contour plot of the converter efficiency swept over switching frequency and switch area for the 1:2 converter. An analogous plot for the 3:2 converter was also constructed to size the 3:2 converter, but is not shown here. Contour efficiencies are indicated. The optimal design lies in a wide plateau above 92% efficiency. The dotted line indicates the limit of output impedance for which an output voltage of 2.1V and 0.7V can be obtained, respectively, for a 1.1V input voltage at maximum output power. The satisfactory design space lies above this dotted line. Finally, the solid straight lines separate the space into four regions, indicating where each of the four loss mechanisms are dominant.

The two converters were designed with a slightly higher switching frequency and switch area than optimal to ensure the output impedance was sufficiently low across the process corners. A nominal switching frequency of 30 MHz was chosen, along with switch areas of 550 and 950 μm^2 for the 1:2 and 3:2 converters, respectively. The anticipated full-load open-loop efficiencies of these two converters are 92% and 86% for the 1:2 and 3:2 converters, respectively.

V. Gate Drive

Since both converters use only native 0.13 μm NMOS devices, driving the gates is not trivial. Two gate-drive structures have been developed for the two SC converters.

A. 1:2 Converter Gate Drive

The 1:2 converter exhibits a regular structure that can be extended for higher ratio conversions. This ladder topology can be driven with cascode level-shifters. The cascode level shifters [8] are made with triple-well 0.13 μm devices and can translate a signal up an arbitrary number of levels. This implementation is shown in fig. 6 for an intermediate stage in a ladder converter.

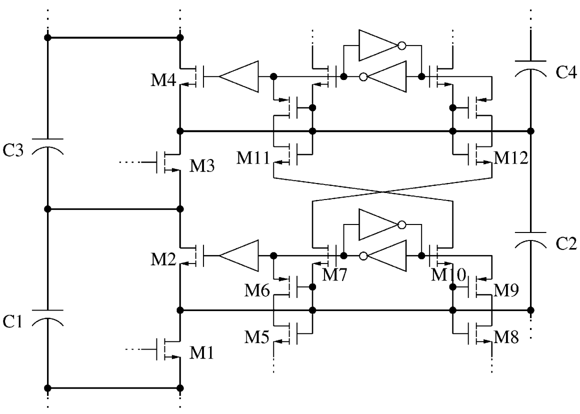

Fig. 6. Cascode level-shift gate drive for the 1:2 ladder converter

Each level shifter and its gate driver are powered from the local power capacitor connected to the relevant switch's source. For instance, capacitor C2 in fig. 6 powers the circuitry to drive M2. Two cross-coupled inverters form a latch, regenerating the signals. Two pull-down signals toggle the latch to either the *on* or *off* position. Two NMOS transistors (M7 and M10) then reproduce these signals to drive the level-shifter above it.

Since all transistors in the level-shifter are 1.2V triple-well devices, shielding devices are needed to prevent device breakdown. Cascode pairs (e.g. M5, M6 and M8, M9) are used to shield both the NMOS pull-down transistor and the gates of the NMOS transistors. Transistor sizing and optimization is critical to ensure operation over rail-voltage variation.

B. 3:2 Converter Gate Drive

An alternate gate drive structure is used for the 3:2 converter. Since the sources of all the transistors in this converter (in fig. 4b) never exceed the V_{DD} rail, a more-direct drive can be used. This charge-pump gate drive, shown in fig. 7, uses a flying capacitor charged to the 1.2V supply to directly drive the gate of a transistor with a non-grounded source. In the 3:2 converter, six of the seven transistors are driven this way. The remaining transistor is driven with an inverter-chain buffer.

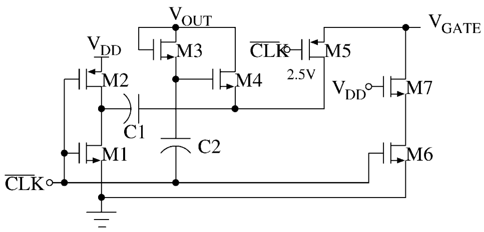

Fig. 7. Capacitor-boost gate drive for the 3:2 converter

The operation of this gate drive circuit will be examined with respect to the drive signal *CLK*. When *CLK* is low, the transistor gate is discharged to ground via transistors M6 and M7. Also, the flying cap C1 is charged to V_{OUT} via M4 and M1.

When *CLK* is high, C1 charges the gate of the power transistor to $V_{DD} + V_{OUT}$ through M2 and M5. In addition, assist cap C2 is charged to V_{OUT} via diode-connected M3. C2 eliminates the diode drop of M4 while charging C1 when *CLK* is low.

C1 is sized such that it dominates the gate capacitance of the power transistor, enabling the gate to be charged to $V_{DD} + V_{OUT}$. While in the on-state, these power transistors' sources are at V_{OUT}, so their gates are driven correctly. This gate driver, along with the cascode level-shifter for the 1:2 converter, ensure efficient converter operation using only the native 0.13 μm NMOS devices.

VI. Synchronous Rectifier

The tire pressure sensor is powered using an electromagnetic shaker. A small permanent magnet moves inside a cylinder wrapped with a single multi-turn winding, shown in fig. 8a. The shaker axis is oriented tangential to the circumference of the wheel. The varying gravitational in the frame of the rotating wheel causes the magnet to fall back and forth in the cylinder. The local centrifugal force is normal to the direction of magnet travel, creating a rotation-speed-dependent friction force. Each time the magnet falls from one side to another, a pulse of voltage is created. To charge a battery or capacitor, these pulses must be rectified.

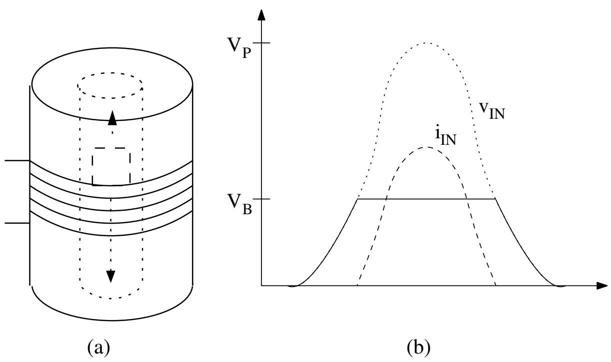

Fig. 8. Shaker (a) design and (b) example input waveform

Simple diode-based rectifiers are convenient but the forward voltage drop severely impacts efficiency at low system voltages. A synchronous rectifier (see fig. 9) uses active devices and feedback to perform the rectification function without significant voltage drop and power loss. The synchronous rectifier approaches efficiencies close to an ideal diode rectifier. By changing the number of turns in the single shaker winding, the source can be matched for the battery or load voltage.

Analysis of a diode rectifier is necessary to compute the optimum number of turns, and thus the optimum peak input voltage. The synchronous rectifier is modeled as an ideal-diode rectifier, as its forward voltage drops turn out to be negligible. Fig. 8b shows a typical waveform for a shaker transition. The amount of power obtained in a transition is the integrated input current multiplied by the battery voltage. Assuming a sinusoidal input pulse and a resistive source impedance R_S, the normalized input energy (per pulse) is given by:

$$E_{IN} = \int_{-\mathrm{acos}(V_B/V_P)}^{\mathrm{acos}(V_B/V_P)} \frac{V_B}{R_S}(V_P \cos(\theta) - V_B)d\theta \qquad (1)$$

$$= \frac{2V_B}{\pi R_S}\left(\sqrt{V_P^2 - V_B^2} - V_B \mathrm{acos}\frac{V_B}{V_S}\right) \qquad (2)$$

The ideal ratio between V_P and V_B can be found by maximizing E_{IN} with respect to V_B. When the optimization is performed, we determine that 93% of the resistively-matched-load energy is recovered when the peak of the input pulse is approximately 2.5 times the battery voltage. At microwatt power levels, it is not advantageous to pursue the remaining 7% by creating an elaborate impedance-matching circuit.

Fig. 9 summarizes the circuits used for the synchronous rectifier. The lower two transistors of the bridge are gated complementarily from a hysteretic comparator. Hysteresis prevents the system from oscillating or using excess power at zero input voltage. As the magnet is usually not moving (as vehicles are usually parked), energy conservation at zero-input is critical. The upper transistors of the bridge run independently and are controlled by comparators continuously sampling the voltage across each of the switches. The delay of the rectifier depends

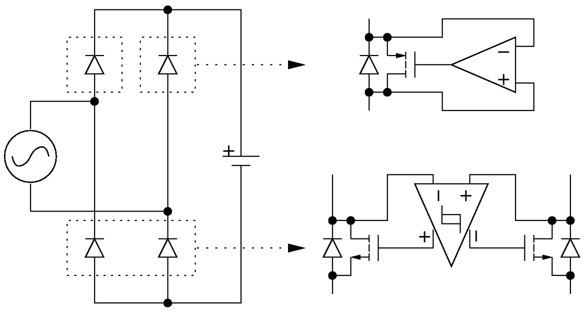

Fig. 9. Synchronous rectifier circuit

on the bias current and the drain-source voltage difference on the switch. By making the switch large, conduction loss is minimized, but transition time is lengthened. An on-state drop of 20-50 mV and bias current of 10 nA were targeted to achieve a compromise between conduction loss, bias current and delay time.

VII. Converter Control

For systems with large peak power to average power ratios, switching frequency control is essential to maintain high efficiencies across operating conditions. Gating and parasitic loss at the maximum switching frequency is approximately 200 μW, which would dominate standby power. Regulation is performed on the output voltage of each converter using a hysteretic controller. By keeping the output voltage regulated at the lowest voltage tolerated by the load, load current consumption can be minimized. Hysteretic (thermostat-like) feedback has advantages of being simple to implement and inherently stable for all loads. In addition, hysteretic feedback exhibits near-instant response to large steps in load current, typical in a wireless sensor node.

However, hysteretic feedback inherently introduces ripple in the output voltage, which can be filtered by a low-dropout-voltage regulator (LDO) for ripple-intolerant loads. In our application, the radio is sensitive to ripple and variation of its supply, so an LDO is used for post-regulation, dropping an additional 50 mW and reducing ripple by approximately 20 dB.

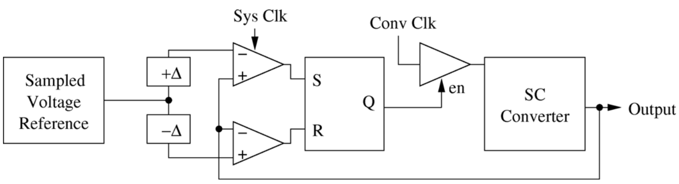

Fig. 10. Diagram of control logic

Fig. 10 shows the control system. Two clocked comparators [9] compare each converter's output to a pair of reference thresholds every 20 μs. If the output is above the upper threshold, the converter's clock is disabled until the output falls below the lower threshold. The hysteresis zone between the two thresholds causes the ripple on the output. The sampled bandgap reference is discussed in section VIII.

VIII. Analog References

To bias the analog circuitry on the IC, an ultra-low-power current reference was used. The topology of the reference was chosen to minimize the bias current for a given size resistor. Fig. 11 shows the structure of the current reference. The circuit is designed for deep sub-threshold operation, yielding an exponential relation between the drain current and the gate-source voltage. The reference current is set by the resistor R and the voltage drop across it, defined by the difference in gate-source voltage between M1 and M2. The value of this resistor is nominally 500 kΩ. At room temperature, the current reference produces a current of 18 nA, independent of supply voltage. The current reference occupies 0.004 mm^2 of die area.

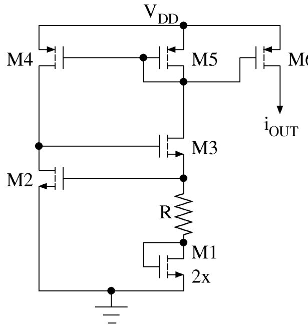

Fig. 11. Sub-threshold current source

A reference voltage is required to perform output voltage regulation. This function is performed by a compact bandgap voltage reference. Even with subthreshold conduction, microamps of current are necessary to allow for sufficiently low process variation. To reduce the average power consumed by this bandgap reference, it was operated at a very low duty cycle and sampled. Since the supply voltage is below the bandgap voltage of silicon (1.2 V), a non-traditional reference structure is used.

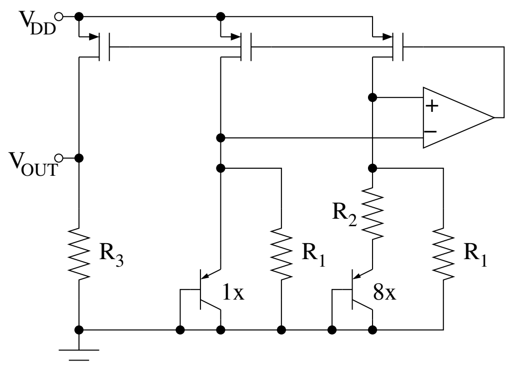

Fig. 12. Low-supply bandgap reference

The bandgap core (in figure 12) is based on the sub-1V operational circuit presented in [10]. It operates below the bandgap voltage by adding currents, proportional and complementary to absolute temperature (PTAT and CTAT, respectively), instead of voltages. The startup and stabilization of the bandgap circuit was optimized for speed to minimize the duty cycle.

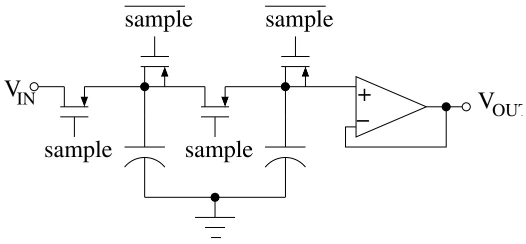

Fig. 13. Low-leakage sample and hold circuit

The sample and hold circuit was specifically designed to reduce leakage and charge injection to keep a constant output voltage with a long period between samples. Figure 13 shows the two-stage sample and hold circuit. Opposing matched PMOS transistors counter the charge injection from turning off the sampling transistors. Thick-oxide transistors were used for the input of the follower to reduce gate tunneling current, which becomes significant for the small sampling capacitors and the long hold times used. As the sampling transistors dominate the leakage rate, a two-stage circuit was used. The first sampling capacitor discharges linearly to the input (which is at a low potential when the bandgap reference is off). The second capacitor, discharges based on the difference between the two capacitor voltages, forming a quadratic voltage profile. This sample and hold topology is more space-efficient than a single-stage circuit using a larger capacitor for a given sample rate.

IX. Experimental Results

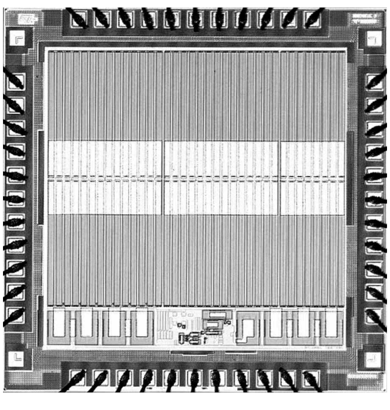

Fig. 14. Photomicrograph of power interface IC

The IC was fabricated using the STMicroelectronics 0.13 μm CMOS process. The die, shown in fig. 14, is approximately 2 mm on a side, significantly smaller than discrete, off-the-shelf system implementations. The die area is dominated by the flying capacitors and the pad ring. The analog circuitry and power transistors occupy the 420 $\mu m\times$ 200 μm region at the bottom-center of the IC. In this IC, the leakage current was approximately 6.5 μA, a combination of analog quiescent current, ESD structure and pad ring leakage, and component leakage.

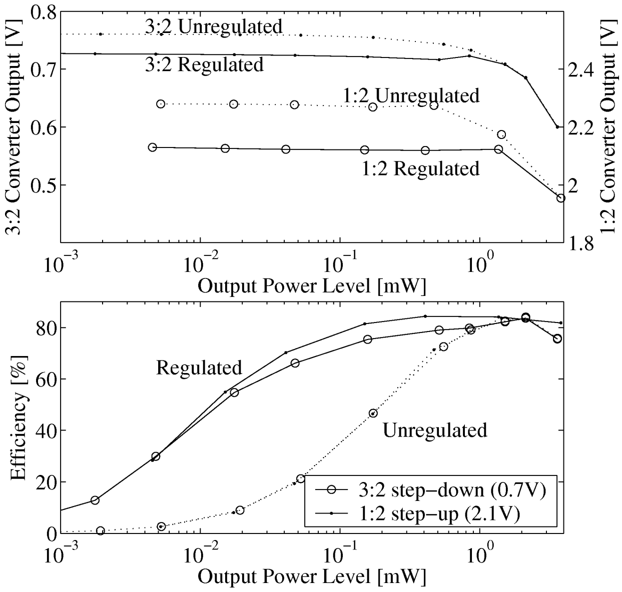

Fig. 15. SC Converter output voltage and efficiency, $V_{in} = 1.15V$

Both switched-capacitor converters were tested over a range of loads. The output voltage and efficiency of both converters with and without regulation are shown in fig. 15. The efficiency data include the quiescent current of the chip, so nominal converter-only efficiencies would be higher. The results show that the regulation function works to achieve a constant output voltage and to dramatically improve efficiency at low power levels. When an overload condition causes the output to drop below the regulation level, the output voltage and efficiency are not affected by the feedback, as the converter is continuously operating at maximum switching frequency. The 3:2 converter and 1:2 converter achieve peak efficiencies of 83.7% and 84.3%, respectively. Efficiency for both regulated converters remains above 60% for output power levels in a wide range between 20 μW and 4 mW.

The performance of the synchronous rectifier is evaluated using a sinusoidal voltage source, with a 2.0 $k\Omega$ series resistance, approximately matching the impedance of the scavenger. The rectifier was compared to three idealized interface models: an exact impedance match (2.0 $k\Omega$ load resistor), an ideal diode rectifier into a fixed voltage source, and a diode bridge rectifier with a forward voltage of 0.2 volts per diode. The third interface represents a Schottky-based diode bridge rectifier, typical of an off-the-shelf implementation.

The efficiency and output power of the synchronous rectifier, and the idealized sources, are plotted in fig. 16. A battery voltage of 1.2 V was used. Nearly identical results were obtained at 100 Hz and 1 kHz input frequency. This

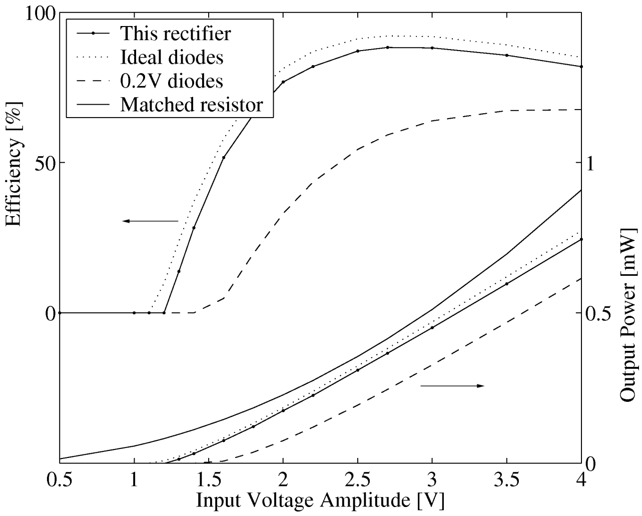

Fig. 16. Power output and efficiency of synchronous rectifier, $V_B = 1.2V$, $R_S = 2.0k\Omega$

frequency range includes this scavenger and the majority of available vibrational scavengers[2]. The peak efficiency of 88%, relative to the matched-impedance case, is obtained at an input amplitude of 2.7 V. At 10 kHz input, the peak efficiency drops by 10%, due to delay-associated losses. Compared with the ideal diode rectifier (the practical maximum efficiency), the rectifier obtains an efficiency of 95.8%. Of this loss, 35% can be attributed to chip-wide quiescent current and 65% to rectifier conduction loss and switching delay. The synchronous rectifier has been shown to be significantly more efficient than a diode-based rectifier, and to approach ideal behavior.

Conclusion

A power interface IC was designed and fabricated to convert power for a wireless tire pressure sensor node. Power conversion was performed using on-chip switched-capacitor converters with size-optimized devices and specially-designed gate drivers. A synchronous rectifier was used to efficiently harvest energy from an electromagnetic shaker. Control circuitry regulated the output voltage while minimizing power consumption.

Acknowledgments

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