An Ultra-Low-Power Power Management IC for Wireless Sensor Nodes

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***Abstract*– A power interface IC is designed and demonstrated to convert and manage power for a wireless tire pressure sensor node. Power conversion is performed using on-chip switched-capacitor converters with size-optimized devices and level-shifting gate drivers. A synchronous rectifier efficiently harvests energy from an electromagnetic shaker and control circuitry regulates the output voltage while minimizing power consumption. The converters achieve efficiencies approaching 80%.**

I. Introduction

Wireless Sensor Nodes (WSNs) are using less power and are becoming smaller as this technology matures. Scavenged-power sensor nodes are now a reality with modern processor, sensor and radio technology [1]. The efficiency of the scavenger-battery-load power interface path, especially at low power, is critical to the performance of such a sensor node. A custom IC is designed in this work to perform scavenger-to-battery and battery-to-load power conversion, while meeting power and size constraints of the system.

II. Application Description

This paper describes a power interface integrated circuit for a wireless tire pressure sensor (TPS), running from energy scavenged from a magnetic shaker [1]. The energy consumers, or loads, include a TI MSP430 microcontroller, an Infineon pressure and acceleration sensor, and a custom PicoRadio radio transmitter [2]. The microcontroller and sensor run at a minimum 2.1 V supply and the radio requires a precise 0.65 V supply. A small NiMH coin cell with a nominal capacity of 18 mAh is used as an energy buffer. The electromagnetic shaker utilizes the rotation of the tire to generate energy to power the sensor.

WSNs often run at very low duty cycles to minimize power consumption. In the TPS application, tire pressure is measured once every six seconds. Power consumption for a single 14ms measurement/transmission period is shown in fig. 1. Each 14ms measurement/transmission cycle uses approximately 29 μJ, yielding a time-averaged power consumption of 6 μW. Peak powers of several mW are required.

The performance of a self-powered WSN is often defined by the sample rate or the number of samples per second the node can acquire and transmit. For a given fixed energy per packet, and a fixed average power supply (defined by the capabilities of the battery or energy scavenger), the sample rate is highly dependent on the efficiency of the power interface circuits. Since WSNs spend the vast majority of time in standby mode, power efficiency at microwatt levels is critical but often lacking in current solutions. This power interface IC aims to improve this efficiency.

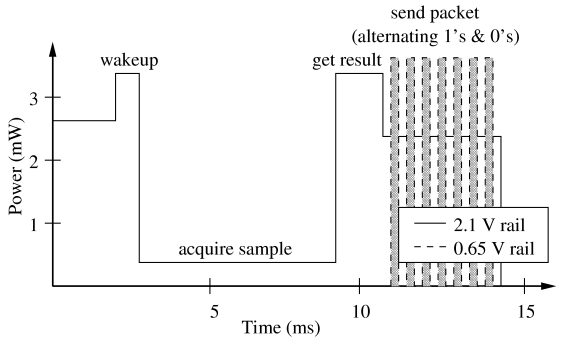

Fig. 1. Measurement and transmission power

III. Converter Architecture

The architecture of the power interface IC is given in fig. 2. The synchronous rectifier interfaces the electromagnetic shaker (scavenger), which puts out a pulsed waveform, to the battery. Details about its use and implementation are in section VI. Two switched-capacitor power converters convert the battery voltage, nominally 1.2 V, to 2.1 V for the microcontroller and sensors and to 0.7 V to power the radio. The design of the power stages of these converters is detailed in section IV, while the gate drive techniques used are described in section V. A linear regulator is used as a post-regulator to more-precisely set the radio voltage to 0.65 V and to smooth the ripple from the switched-capacitor converter. The design of the linear regulator is not novel, so it will not be described in depth.

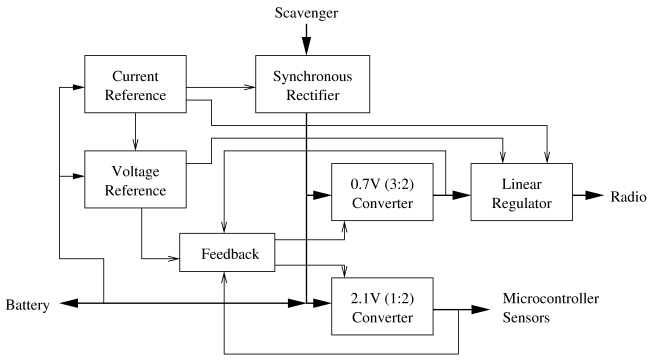

Fig. 2. Block diagram of the converter IC

Finally, a hysteretic feedback controller is used to regulate output voltage and switching frequency, and is described in section VII.

A number of analog blocks provide support to the power electronics by providing references and control signals. A self-biased current source (reference) supplies bias current to the chip via a current mirror. It is biased at 18 nA independent of V_{DD} and mildly dependent on temperature. An ultra-low-power sampled bandgap reference provides a reference voltage to both the converter feedback circuitry and the linear regulators. The design of this voltage reference is further described in section VII.

The converter IC was implemented using a 0.13 μm CMOS process provided by ST Microelectronics. The nominal 1.2V working voltage matches the battery voltage perfectly, and the process provides 2.5 V transistors and high-density capacitors, the latter used in the switched-capacitor converters.

IV. Design of the Power Stages

Two independent switched-capacitor (SC) converters perform the power conversion between the battery and the loads. A 1:2 ratio converter, shown in fig. 3a, provides a doubled voltage for the microcontroller and sensors. The minimum supply voltage for these components is 2.1 V. A 3:2 ratio converter, shown in fig. 3b, provides a lower voltage to supply the radio, nominally at 0.65 V.

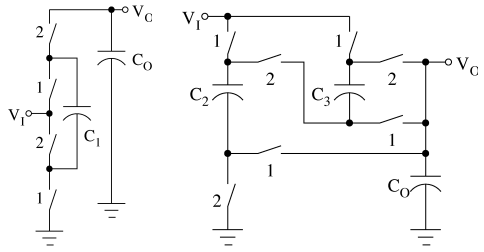

Fig. 3. Switch-level diagram of a) 1:2 converter, b) 3:2 converter

The topologies are chosen to utilize the native transistors of the 0.13 μm CMOS process, even to generate 2.1 V. The benefits and drawbacks of a number of SC converter topologies are described in reference [4]. All power switches are implemented using NMOS transistors to minimize die area and gating and parasitic losses. Section V addresses the level shifters and other circuitry required to drive these transistors.

The transistors and capacitors in each SC converter must be sized correctly to provide the required performance. Devices which are too large waste silicon area and require excess power to overcome the parasitic losses. In previous work [4], [5], an optimization method for SC converters was developed, and will be applied here. The power losses due to finite capacitance and switch conductance in a SC converter can be lumped into a single output impedance representing a converter's topology and component values [4], [6]. From the system specifications, the desired output impedance for each converter can be determined. For this design, the converters should be able to achieve the desired output voltage for battery voltages down to 1.1 V.

The desired output impedance can be calculated from the worst-case load condition and the acceptable drop. For the 1:2 converter, the target output impedance was determined to be about 60 Ω for a 100 mV drop at the output. Likewise, the output impedance target for the 3:2 converter is about 8 Ω.

A converter's output impedance is a function of its switching frequency f_{sw}. At low f_{sw}, the output impedance is capacitor-limited (in the *slow switching limit (SSL)*), and is inversely proportional to frequency. At high f_{sw}, the output impedance levels off and becomes switch-limited (this is the *fast switching limit (FSL)*) [4]. By considering the output impedance at both limits, the converter's switching frequency and component sizes can be optimized.

Capacitor size is limited by die area. By dividing this area between the three power capacitors (C_1, C_2 and C_3) such that the switching frequency for both converters is the same, the values of the capacitors and the switching frequency can be determined. Capacitors C_1, C_2 and C_3 were determined to have values of 750 pF, 1.2nF and 1.2nF, respectively. The switching frequency to obtain the target output impedance for both converters is about 23 MHz.

The power transistors are then sized such that they do not limit the output impedance at the maximum switching frequency. The power transistors occupy a much smaller area than the capacitors, but still must be made small to minimize gate drive loss and associated dynamic loss. After performing the optimization [4], the four switches in the 1:2 converter are each designed to have an on-state resistance of 3.8 Ω while the seven switches in the 3:2 converter are each designed to have an on-state resistance of 2.6 Ω. The corresponding transistor widths can be found by finding the conductance per width of a minimum channel length transistor driven at the appropriate voltage.

V. Gate Drive

Since both converters use only native 0.13 μm NMOS devices, driving the gates is not trivial. The 1:2 converter exhibits a regular structure that could be extended for higher ratio conversions. This topology is known as the ladder topology, and can be driven with cascode level-shifters. This level shifter [7] is made with triple-well 0.13 μm devices and can translate a signal up an arbitrary number of levels. This implementation is shown in fig. 4 for an intermediate stage in a ladder converter.

Each stage is powered from the local power capacitor connected to the relevant switch's source. Capacitor C2 in fig. 4 powers the circuitry to drive M2. The two inverters, and the gate buffer are supplied by this capacitor. The two inverters, sized with a weak PMOS, create a latch to regenerate the signal at each rung of the ladder. There are two connections to the lower stage, each is either floating or pulled low. Cascode-connected transistors M6 and M9 protect the gates of the other transistors in the stage from being subjected to voltage lower than the local ground. Likewise, transistors M11 and M12 protect the drains of M7 and M10 from breakdown. The

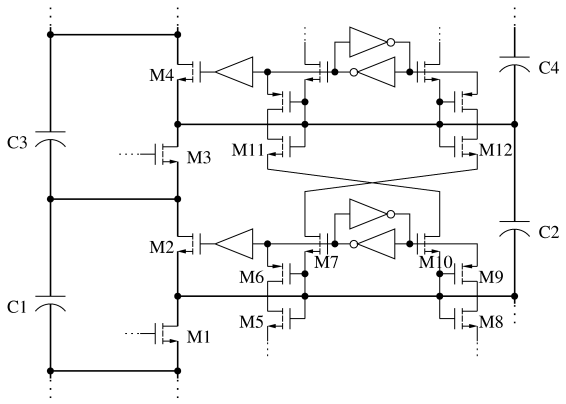

Fig. 4. Cascode level-shift gate drive for the 1:2 ladder converter

cascode PMOS transistors M6 and M9 must be sized large to allow the latch to toggle. A pull-down on an input line can flip the latch, turning the gate drive on or off. The signal is then translated to the next rung of the ladder.

An alternate gate drive structure is used for the 3:2 converter. Since the sources of all the transistors in this converter never exceed the V_{DD} rail, a more-direct drive can be used. This gate drive circuit is shown in figure 5. Capacitor C1, around 2 pF, is used in a charge pump scheme to create a voltage greater than the V_{DD} rail. Capacitor C2, charged through diode-connected M3, drives M4 to charge C1 when the input is high (gate off). When the input is low (gate on), M2 and M5 turn on, charging the gate to $V_{DD} + V_{OUT}$. When the input is on (gate off), M6 discharges the gate to ground through cascode transistor M7. This gate drive structure provides more robust performance compared to the cascode level-shift gate drive, but cannot be applied to a multi-stage ladder structure.

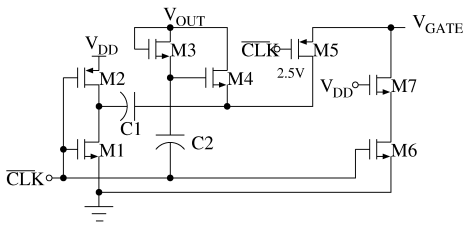

Fig. 5. Capacitor-boost gate drive for the 3:2 converter

VI. Synchronous Rectifier

The tire pressure sensor is powered using an electromagnetic shaker. A small permanent magnet moves inside a cylinder wrapped with a single winding. The shaker axis is oriented tangential to the circumference of the wheel. The varying gravitational in the frame of the rotating wheel causes the magnet to fall back and forth in the cylinder, creating pulses of voltage. To charge a battery or capacitor, these pulses must be rectified.

Simple diode-based rectifiers are convenient but the forward voltage drop severely impacts efficiency at low system voltages. A synchronous rectifier uses active devices and feedback to perform the rectification function without significant voltage drop and power loss. Fig. 6 sketches the circuitry used for the synchronous rectifier.

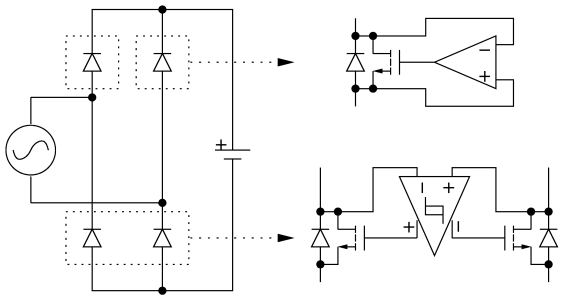

Fig. 6. Synchronous rectifier circuit

The lower two transistors of the bridge are gated complementarily from a hysteretic comparator. Hysteresis prevents the system from oscillating or using excess power at zero input voltage. The upper transistors of the bridge run independently and are controlled by comparators looking at the voltage across the switch. The delay of the rectifier depends on the bias current and the voltage difference on the switch. By making the switch large, conduction loss is minimized, but transition time is lengthened. An on-state drop of 50-100 mV and bias current of 10 nA were targeted to achieve a compromise between conduction loss, bias current and delay time. To achieve the maximum rectified power, the number of turns on the shaker was varied to achieve an approximate impedance match.

VII. Converter Control

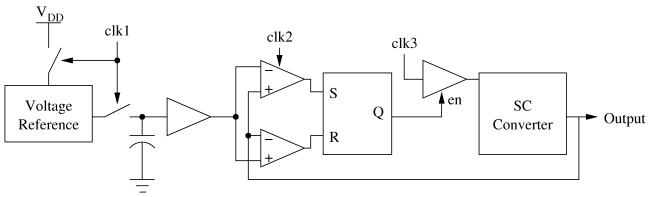

Fig. 7. Diagram of control logic

Fig. 7 shows the control system. A hysteretic control method is used to regulate the output of each of the two converters. The method is simple and provides the same reduction in gating power as more sophisticated methods. By not clocking the converter continuously at low loads, gate and dynamic losses can be greatly reduced. However, moderate ripple at the converters' output is introduced. This ripple does not affect the operation of the microcontroller or sensors on the 2.1 V rail. The 0.65 V radio requires a constant rail, which is created by a linear post-regulator from the 3:2 converter's output. Two clocked comparators [8] compare each converter's output to a pair of reference thresholds. If the output is above the upper threshold, the converter's clock is disabled until the output falls below the lower threshold. The hysteresis zone between the two thresholds causes the ripple on the output.

A low-supply-voltage bandgap reference [9] is used to create a reference voltage from a supply below 1.2 V. To reduce power, the output from the reference is sampled with a low-leakage sample-and-hold circuit every 20 ms, and the reference is turned off between samples. Thus, the average power consumption of the reference is merely 40 nW, compared to the reference active power of 20 μW. This power savings is essential to meet the application's power target.

VIII. Experimental Results

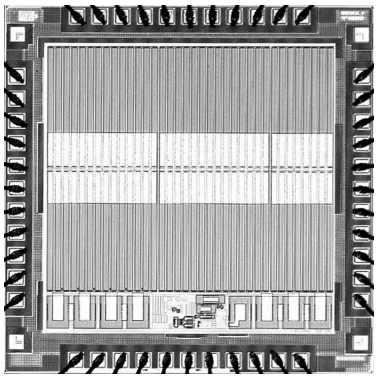

Fig. 8. Photomicrograph of power interface IC

The IC was fabricated using an ST 0.13 μm CMOS process. The die, shown in fig. 8, is approximately 2 mm on a side, significantly smaller than off-the-shelf implementations. In this IC, the leakage current was approximately 40 μA, attributable to the pad ring and on-chip decoupling capacitor leakage. A revision is in progress to reduce or eliminate the unnecessary leakage current.

Both switched-capacitor converters were tested over a range of loads. The output voltage and efficiency of both converters with and without regulation are shown in table I. The efficiency data do not include the leakage current as this current cannot be associated with the individual power converters. The efficiency numbers are worst-case results as there are additional internal loads which cannot be separated from the external load. The results show that the regulation function works to achieve a constant output voltage and improved efficiency at low power levels. When the output drops below the regulation level, the output voltage and efficiency are not affected by the feedback. Variation in the internal clocking rate and excessive layout ESR are responsible for the reduced maximum power level of the converter. Both factors will be addressed in the next revision of the IC.

TABLE I

Performance of switched-capacitor converters, $V_{in} = 1.2V$

Approx. output power	5 μW	45 μW	450 μW	1.4 mW
1:2 Converter				
Unregulated voltage:	2.376 V	2.367 V	2.294 V	2.093 V
Unregulated efficiency:	2.3%	17%	64%	75%
Regulated voltage:	2.317 V	2.316 V	2.294 V	2.094 V
Regulated efficiency:	8.1%	36%	64%	75%
3:2 Converter				
Unregulated voltage:	780 mV	775 mV	724 mV	608 mV
Unregulated efficiency:	2.3%	19%	62%	65%
Regulated voltage:	683 mV	680 mV	671.6 mV	608 mV
Regulated efficiency:	14%	49%	66%	65%

TABLE II

Performance of rectifiers (V_B = 1.1V, R_S = 2.1K, V_S = 2.8 V)

	Output Power	% of Matched Load
Matched ($R_L = R_S$)	467 μW	100%
Ideal diode bridge	429 μW	91.2%
$V_F = 0.5V$ diode bridge	120 μW	25.7%
Synchronous rectifier at 100 Hz	*360 μW*	*77.1%*
Synchronous rectifier at 1 kHz	*280 μW*	*60.0%*

The performance of the synchronous rectifier is compared to three idealized interface models for a Thevenin sinusoidal source, shown in table II. Two experimental results were measured: one at a frequency of 1 kHz and one at 100 Hz. The measured performance comes close to the ideal bridge rectifier but the limited response speed and switching power cause the performance to drop at higher input frequencies. For slow pulsed inputs, the synchronous rectifier circuit is significantly more efficient than a diode rectifier with a finite forward voltage.

Conclusion

A power interface IC was designed and fabricated to convert power for a wireless tire pressure sensor node. Power conversion was performed using on-chip switched-capacitor converters with size-optimized devices and specially-designed gate drivers. A synchronous rectifier was used to efficiently harvest energy from an electromagnetic shaker. Control circuitry regulated the output voltage while minimizing power consumption.

Acknowledgments

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