

# An Integrated Controller for a High Frequency Buck Converter

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**Abstract**— This paper reports on the design, fabrication, and test of a controller IC for a buck converter, designed to operate with synchronous rectification in a constant off-time, variable frequency mode. This mode is advantageous to support soft-switching over a wide input voltage range. Operation up to 5MHz allows potential use with a micro-fabricated inductor. Considerable attention is paid to the control of deadtimes. Specifically, the adaptive deadtime control scheme proposed in our earlier work was successfully implemented and tested.

## I. INTRODUCTION

This paper reports on the design and test of an IC controller for a high frequency integrated buck converter. The target application is for a wide range input (8V - 40V) and a 5V output. The high switching frequency allows the use of a microfabricated inductor which is currently under research and development [1, 2]. At the proposed switching frequency ( $\sim 5\text{MHz}$ ), switching loss of a conventional hard-switched converter is high. Techniques such as zero voltage switching (ZVS) and adaptive deadtime control scheme are therefore necessary. These techniques are described in Section II, along with a loss analysis of the buck converter. Implementation issues of the circuit are discussed in Section III. Test results of an IC controller are reported in Section IV.

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## II. CIRCUIT DESCRIPTION

### A. Buck Converter with Synchronous Rectification and Soft Switching

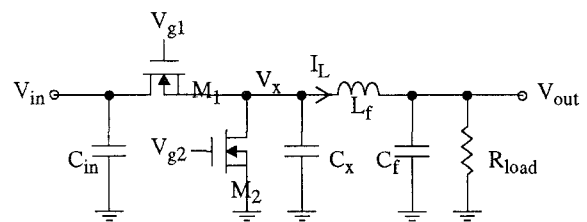


Fig. 1. Buck converter with synchronous rectification

Fig. 1 shows the buck circuit with synchronous rectification. The soft switching operation, which is described in [3, 4, 5] and by many other authors, can be explained with reference to the idealized periodic steady state waveforms in Fig. 2.

Assume  $M_1$  is on. As  $L_f$  has a constant positive voltage ( $V_{in} - V_{out}$ ), the inductor current ( $I_L$ ) increases linearly with time. When  $M_1$  is turned off, the positive inductor current discharges the parasitic capacitance at the inverter node ( $C_x$ ). The high-to-low transition at the inverter node will be lossless if  $M_2$  is gated on when its drain-source voltage is zero, i.e.  $V_x = 0$ .

When  $M_2$  is on,  $I_L$  decreases linearly because a constant negative voltage ( $-V_{out}$ ) is now applied across  $L_f$ . If the current ripple ( $\Delta I_L$ ) is large enough [5], the current re-

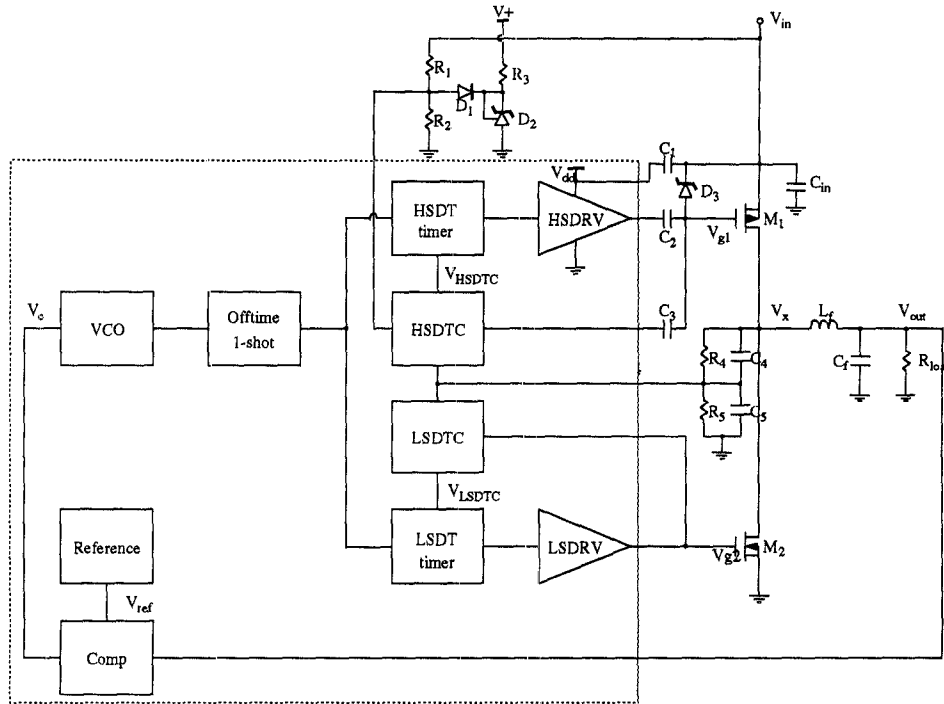


Fig. 3. Block diagram of the integrated buck controller and the buck converter (Blocks in the box are implemented on-chip).

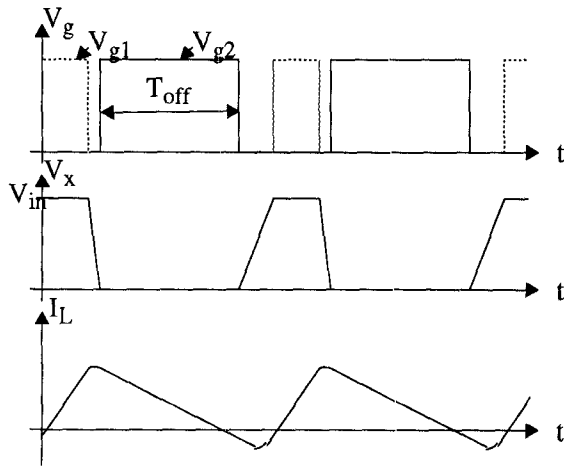


Fig. 2. Ideal periodic waveforms of the soft-switched buck converter

verses, and  $C_x$  will be charged by the negative inductor current once  $M_2$  turns off. A lossless low-to-high transition at the inverter node is achieved by turning on  $M_1$  when  $V_x = V_{in}$ .

By switching the transistors at zero drain-source potential (ZVS), the capacitive switching loss of the inverter node, which can dominate in a high frequency converter,

is essentially eliminated.

### B. System Block Diagram

In order to achieve ZVS, it is necessary to have sufficient reverse inductor current under all input voltage and load conditions. One simple scheme to meet this requirement is to have a constant inductor current ripple,  $\Delta I_L$ , that is large enough. Note that  $\Delta I_L \approx V_{out} T_{off}$ , where  $T_{off}$  (Fig. 1) is the time interval during which the low-side device is on. The above scheme therefore implies a constant off-time control. In terms of  $T_{off}$ , the duty cycle of the buck converter is given by:

$$D = \frac{T_{on}}{T} = 1 - T_{off} f_s, \quad (1)$$

where  $T_{on}$  is the time interval during which the high-side device is on,  $T$  is the period, and  $f_s$  is the operating frequency. Eq.(1) shows that with a fixed off-time, the switching frequency may be varied to modulate the duty cycle.

Fig. 3 shows a block-level system implementation of the *variable frequency, fixed off-time* control scheme. A

voltage-controlled oscillator (VCO), generates a variable frequency signal proportional to its control voltage,  $V_c$ . The block, COMP, completes the main feedback loop. It compares the output voltage,  $V_{out}$  against a reference,  $V_{ref}$ , and provides compensation to generate the signal  $V_c$  fed to the VCO, to achieve output voltage regulation.

The output waveform of VCO is shaped by a one-shot (offtime 1-shot) to get the required fixed off-time. The signal is further modified by the deadtime timers (HSDT and LSDT timers) independently to add in appropriate deadtime intervals. The two timers are controlled by their respective deadtime controllers, HSDTC and LSDTC, the principle of which is describe in Section IIC. The high-side and low-side devices are then driven by the two drivers, HSDRV and LSDRV.

Note that a power P-channel MOSFET ( $M_1$ ) is used for the high-side switch so that the controller (the dashed box) can be fabricated in a standard CMOS process. The capacitor,  $C_2$ , level-shifts the gate signal whereas capacitor  $C_1$  facilitates a fast turn-off of  $M_1$  by providing a low-impedance return path.

### C. Adaptive Deadtime Control Loop

As pointed out earlier, if a power transistor is turned on before its drain-source potential reaches zero, a capacitive switching loss at the inverter node results. On the other hand, if the power transistor is turned on late, the parasitic body diode may turn on and introduce additional losses through body diode conduction and reverse recovery. Therefore, to achieve maximum efficiency, the deadtime between the conduction of the two transistors should ideally equal the corresponding transition time at the inverter node.

Since the transition time varies greatly with input voltage and load, there is a need to adjust the deadtime in an on-line manner. One scheme that provides such functionality, called adaptive deadtime control, is described in [3, 6].

A block diagram of the adaptive deadtime control loop for the low-side power transistor is shown in Fig. 4. The

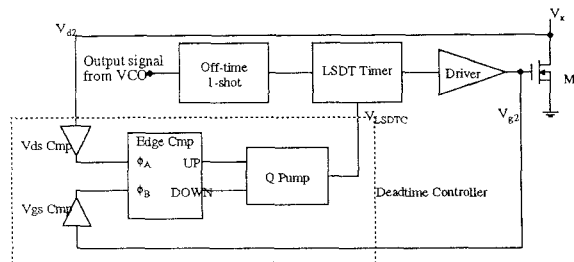


Fig. 4. Block diagram of the low-side adaptive deadtime control loop

$V_{ds}$ -comparator senses the zero crossing of  $V_{ds}$  and produces a low-to-high transition in its output. Similarly, the  $V_{gs}$ -comparator pulls up its output once it detects that the gate voltage of the power transistor exceeds the threshold voltage. If the low-to-high output transition of the  $V_{ds}$  comparator occurs earlier than that of the  $V_{gs}$  comparator, a positive pulse is asserted at the  $UP$  output of the edge comparator. Conversely, if the positive edge of the  $V_{ds}$  comparator lags that of the  $V_{gs}$  comparator, the edge comparator produces a positive pulse at the  $DOWN$  output. The pulse width of the respective  $UP$  or  $DOWN$  signal equals the time interval between the positive edges of the two comparator outputs. The pulse is integrated by a charge pump, which causes either an increase or decrease of the control voltage ( $V_{LSDTC}$ ). Finally,  $V_{LSDTC}$  controls the delay produced by the low-side deadtime one-shot. A higher  $V_{LSDTC}$  decreases the delay and thus the deadtime.

When the circuit is in periodic steady state, as shown in Fig. 5, the deadtime is constant, implying a constant delay produced by the low-side deadtime one-shot and a constant  $V_{LSDTC}$ . The constant  $V_{LSDTC}$  in turn requires no pulse at either the  $UP$  or  $DOWN$  outputs of the edge comparators. In other words, the low-to-high transition of both the  $V_{ds}$  and  $V_{gs}$  comparators must happen at the same time. Therefore, the low-side power transistor is gated on exactly when  $V_{ds}$  crosses zero.

Fig. 6 shows the ideal waveforms of the adaptive deadtime control loop when the transistor turns on early due to, for example, a change in load current. The  $V_{gs}$  comparator output leads the  $V_{ds}$  comparator output, and

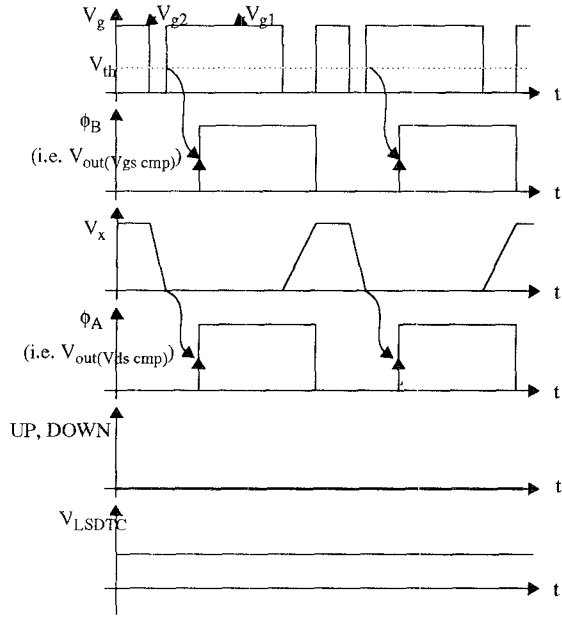


Fig. 5. Ideal periodic steady state waveforms of the adaptive deadtime control loop

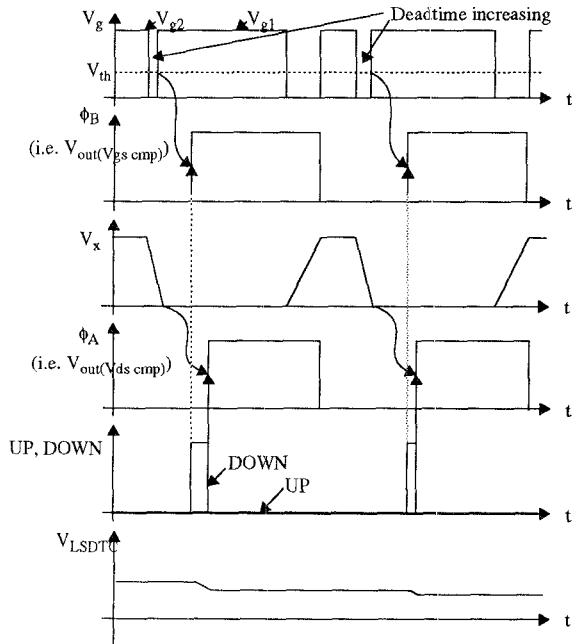


Fig. 6. Ideal waveforms of the adaptive deadtime control loop with early turn-on

hence a positive pulse is asserted at the *DOWN* output of the edge comparator. By the action of the charge pump,  $V_{LSDTc}$  is decreased. The reduced  $V_{LSDTc}$  then increases the deadtime such that the time lag between the

turn-on of the power transistor and the zero crossing of its drain-source voltage is reduced. The above process repeats for many cycles, successively reducing the time lag, until asymptotically the transistor is turned on exactly when its drain-source potential equals zero.

A similar control scheme is utilized for the high side deadtime control.

#### D. Passive Loop Compensation

Consider the buck converter as shown in Fig. 1, the transfer function of a small perturbation in duty cycle,  $d$ , to the small signal output,  $v_{out}$  is given by

$$\frac{v_{out}}{d}(s) = V_{in} \cdot \frac{\frac{1}{LC}}{s^2 + s \frac{1}{R_{load}C} + \frac{1}{LC}}. \quad (2)$$

If the parasitic resistances  $R_l$  and  $R_c$ , associated with  $L_f$  and  $C_f$ , respectively, are taken into consideration, the expression becomes

$$\begin{aligned} \frac{v_{out}}{d}(s) &= V_{in} \cdot \frac{(\frac{R_{load} \parallel R_c}{L_f})(s + \frac{1}{R_c C_f})}{s^2 + bs + c} \\ b &= \left[ \frac{1}{(R_{load} + R_c)C_f} + \frac{R_c R_l + R_l R_{load} + R_c R_{load}}{L_f (R_{load} + R_c)} \right] \\ c &= \frac{R_{load} + R_l}{L_f C_f (R_l + R_c)} \end{aligned} \quad (3)$$

The overall forward small-signal transfer function,  $v_{out}/v_c$ , (see Fig. 3) is thus

$$\frac{v_{out}}{v_c}(s) = \frac{d}{v_c}(s) \frac{v_{out}}{d}(s) = -A_{VCO} \frac{v_{out}}{d}(s), \quad (4)$$

assuming the output frequency of the voltage-controlled oscillator varies linearly with its controlled voltage,  $v_c$ , with a slope of  $-A_{VCO}$ . Note that the ESR resistance of the output capacitor,  $R_c$ , introduces some phase lead. To obtain a good phase margin, however, it is often necessary to provide additional phase lead at the crossover frequency.

One conventional PID compensation is shown in Fig. 7(a). The amount of positive phase shift available at high frequency depends on the ratio  $R_4/R_3$ . The drawback of such a scheme, however, is the requirement of a

high gain-bandwidth op-amp. An alternative approach is shown in Fig. 7(b). In this passive loop compensation scheme, the integral control is still provided by the op-amp. However, at high frequency, the  $R_5$ - $C_2$  path dominates, and provides the required phase margin depending on the ratio of resistors  $R_5/R_4$ . The necessity of a high gain-bandwidth op-amp is thus eliminated. Note that substantial loop gain is achieved with the VCO modulation scheme.

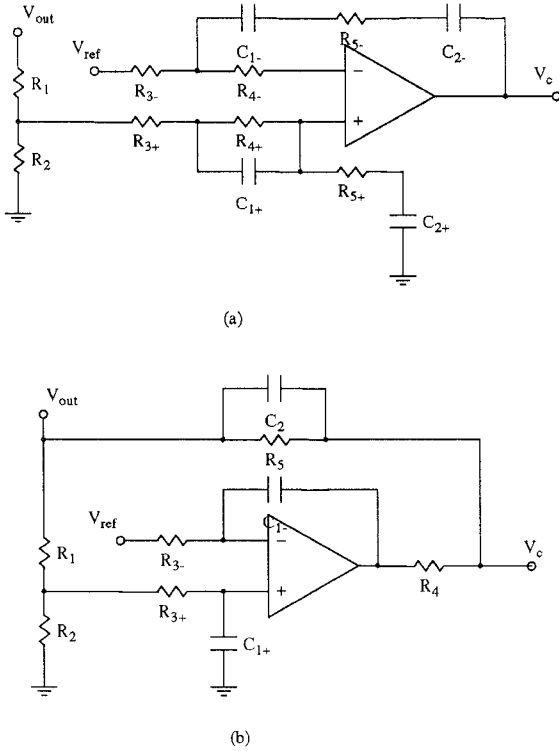


Fig. 7. Loop compensation schemes: (a) conventional PID controller; (b) passive compensation

### E. Loss Analysis of the Buck Converter

The power train has the following major components of power losses: conduction loss (in power MOSFETs and passive components), gate-drive loss, inductive switching loss, and capacitive switching loss.

Conduction loss is mainly due to the  $R_{ds(on)}$  of the power transistors, and parasitic resistances, for example,  $R_l$  of the main inductor and  $R_c$  of the output capacitor.

Assuming the inductor current is roughly triangular with an average value  $I_{load}$  and a ripple  $\Delta I_l$ , the total conduction loss is given by:

$$P_{loss}(cond.) = \left( I_{load}^2 + \frac{\Delta I_l^2}{12} \right) [DR_{ds(on),PMOS} + (1-D)R_{ds(on),NMOS}] + I_{load}^2 R_{l,dc} + \frac{\Delta I_l^2}{12} (R_{l,ac} + R_c), \quad (5)$$

where  $R_{l,dc}$  and  $R_{l,ac}$  are respectively the dc and ac values of  $R_l$ .

Gate-drive loss at a switching frequency  $f_s$  is described by:

$$P_{loss}(gate) = E_g f_s + P_{loss}(driver), \quad (6)$$

where  $E_g$  is the gate energy transferred per cycle while  $P_{loss}(driver)$  includes dissipation in gate drive circuitry.  $P_{loss}(driver)$  may also be proportional to the switching frequency.

Inductive switching loss is caused by loss of stored energy in stray inductance  $L_s$  in the loop formed by the input decoupling capacitor and the power transistors. The following equation describes the loss:

$$P_{loss}(ind. sw.) = \frac{1}{2} L_s I_{l1}^2 + \frac{1}{2} L_s I_{l2}^2, \quad (7)$$

where  $I_{l1}$  is the inductor current in the loop when transistor  $M_1$  turns off, and  $I_{l2}$  is a similar current when  $M_2$  turns off.

Ideally, with ZVS of the power transistor, there is no capacitive switching loss at the inverter node. However, at high input voltage and switching frequency, a large inductor ripple current is required to ensure ZVS [5]. A trade-off between the conduction loss and the capacitive switching loss thus exists at a specific switching frequency. Typically there is no capacitive switching loss associated with the high-to-low transition. However, at full load, the low-to-high transition may exhibit some capacitive switching loss due to non-ideal ZVS. This switching loss is related to the maximum voltage ( $V_{max}$ ) achieved by the inductor current ringing with the parasitic capacitance  $C_x$ . Suppose  $I_l = I_{l2}$  when the low-side power MOSFET ( $M_2$ ) turns off. If  $C_x$  is linear,  $V_{max}$  can be found by solving

the following equation:

$$\frac{1}{2}C_x(V_{max} - V_{out})^2 - \frac{1}{2}C_xV_{out}^2 = \frac{1}{2}L_f I_{l2}^2 \quad (8)$$

Conceptually, the energy dissipation can be calculated from the  $Q$ - $V$  curve, as indicated by the shaded area in Fig. 8.

As an extra charge  $[Q_x(V_{in}) - Q_x(V_{max})]$  must be delivered by the source and the energy stored (represented by the area under the  $Q$ - $V$  curve) in  $C_x$  is fully recovered at the high-to-low transition, the capacitive switching loss is:

$$E_{loss}(cap. sw.) = [Q_x(V_{in}) - Q_x(V_{max})] V_{in} - [E_x(V_{in}) - E_x(V_{max})], \quad (9)$$

where  $Q_x(V_x)$  is the charge stored at the inverter node at a voltage of  $V_x$ , and  $E_x(V_x)$  represents the energy stored at the same potential. A similar analysis is given in reference [7].

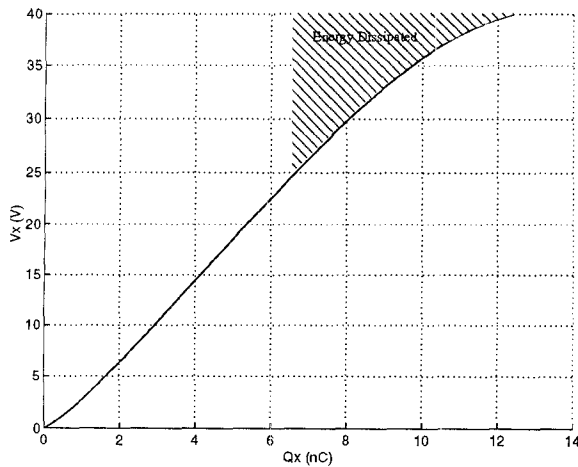


Fig. 8. Simulated  $Q$ - $V$  curve of the parasitic capacitance  $C_x$ , associated with both  $M_1$  and  $M_2$ .

### III. CIRCUIT IMPLEMENTATION

The controller circuit in Fig. 3 was fabricated through a standard  $1.2\mu$  CMOS process. The following sections give brief descriptions of the circuit implementation

#### A. Gate Driver

The two gate drivers are implemented with cascaded inverter stages with a tapering factor of 6. Experimental results show that a rise/fall time of 10ns is achieved with a 1nF capacitance loading.

#### B. Adaptive Deadtime Control Loop

Each  $V_{ds}$  comparator of the adaptive deadtime control loops detects the zero-crossing of an external FET's drain-source voltage at a falling edge. With an 8-to-1 external divider, the input overdrive is roughly 100mV. However, at maximum input voltage, the comparator must recover from a high initial (reverse) overdrive. For fast recovery, a cascade of low-gain stages comparator is used [8, 9]. For the  $V_{ds}$  comparator of the low-side deadtime loop, a PMOS input pair is used as the required input common mode voltage includes the ground potential whereas the high-side loop uses a NMOS input pair to allow zero-crossing detection at the supply rail.

Compared to the  $V_{ds}$  comparators, the requirements for the  $V_{gs}$  comparators are much more lenient. As the gate voltage is quite sharp (10ns rise/fall time), a digital schmitt trigger has been used. The delay of each  $V_{gs}$  comparator, however, needs to be carefully matched with the corresponding  $V_{ds}$  comparator.

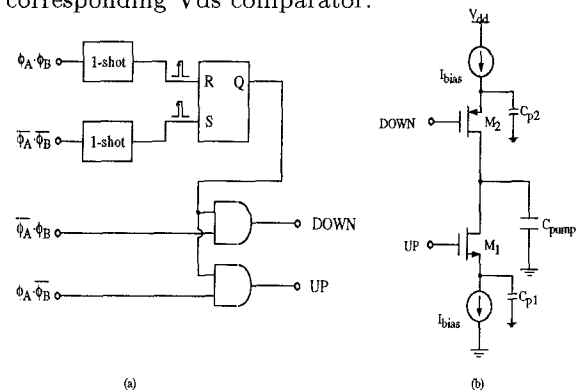


Fig. 9. Circuit implementation: (a) edge comparator, (b) charge pump

The edge comparator used in the adaptive deadtime loop is similar to one in a typical phase-locked-loop. The major difference is that the former one only activates the

output between the positive edges of its inputs. The block diagram in Fig. 9(a) shows the realization. Note that when the two inputs are perfectly matched due to the action of the adaptive loop, the asynchronous sequential circuit is not working in the fundamental mode, i.e. more than one inputs change at the same time. Care must be taken to prevent possible hazard.

Finally, Fig. 9(b) shows a simple implementation of the charge pump. The parasitic capacitances,  $C_{p1}$  and  $C_{p2}$ , result in charge injection when the corresponding switch turns on. The effect can be minimized through proper sizing of the switch, the tail current and the main capacitor,  $C_{pump}$ .

### C. On-Chip Passive Compensation

The major challenge to an on-chip realization of the passive compensation is the limited amount of capacitance that can be realized. The problem is further aggravated by the fact that high quality double poly capacitor is unavailable in the digital CMOS process used. For an example, consider the passive network of  $C_2$ - $R_5$ - $R_4$  in Fig. 7(b).  $R_4$  and  $R_5$  are realized as poly resistors, their values bounded above due to considerations of area and parasitic capacitance. As a result, a fairly high value of  $C_2$  (20pF) is needed. A solution is to use the gate capacitance of a PMOS (Fig. 10). As the input voltage of the voltage-controlled oscillator,  $V_c$  never rises above 2V in steady state while  $V_{out}$  is nominally 5V, the PMOS is always guaranteed to be in strong inversion. Moreover, the parasitic capacitance,  $C_{p2}$  is shorted by the low-impedance source,  $V_{out}$ .

However, the same technique cannot be applied to the integrating capacitors  $C_{1+}$  and  $C_{1-}$  since the voltage across  $C_{1-}$  need not be higher than  $V_{th}$ . Therefore,  $C_{1+}$  and  $C_{1-}$  are realized with metal2-metal1-poly capacitor. The values are chosen to be as small as tolerance and matching allow. A MOSFET-C integrator is then formed by two MOSFETs biased in triode, which implement  $R_{3+}$  and  $R_{3-}$  with the required time constant.

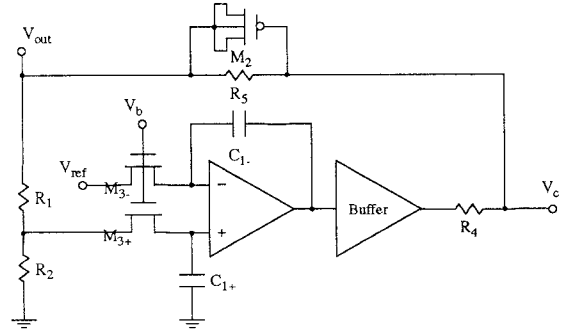


Fig. 10. Loop compensation schemes: (a) conventional PID controller; (b) passive compensation

## IV. TEST RESULTS

A prototype of the high frequency buck converter with the IC controller has been built to evaluate the performance. Fig. 11 shows the measured total power loss at different input voltages with the two deadtimes manually adjusted to their respective optimal values. At the maximum input voltage ( $V_{in}=40V$ ), a total loss of 1.74W was measured, which corresponds to an efficiency of 75%. Also shown in the graph are the different predicted power losses. These include conduction loss, capacitive switching loss, inductive switching loss, gate capacitance loss and driver loss, and standby dissipation. The total predicted loss roughly agrees with the measured results.

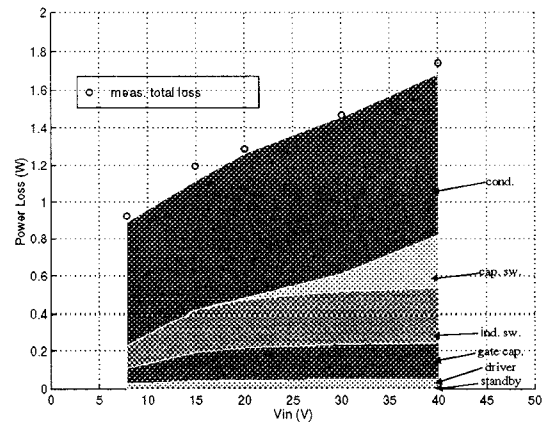


Fig. 11. Measured and predicted power losses of the buck converter

Fig. 12 shows the total power dissipation as a function of the low-side deadtime at 20V input. The high-side dead-

time was fixed at its optimal value manually. It is clear that at such a high input voltage, an early turn-on incurs far more loss than a late turn-on, due to the excessive capacitive switching loss. Therefore, a reasonable strategy for a fixed deadtime control is to use the maximum required values. For this particular application, it would mean using the optimal deadtime for an input voltage of 40V and no load for the low side deadtime, and the optimal deadtime for a 40V input and full load for the high side.

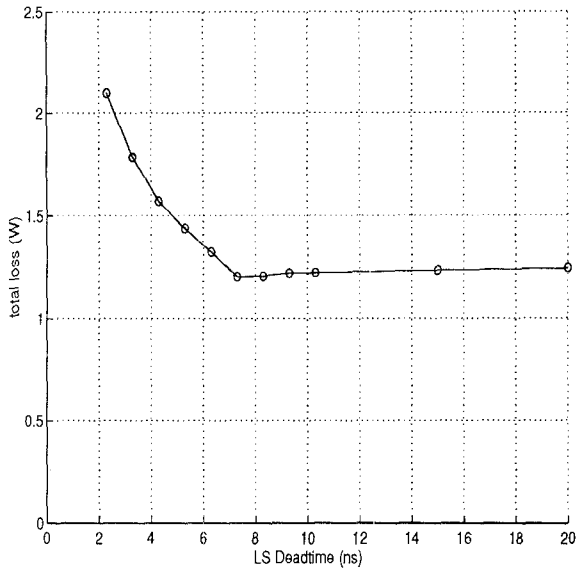


Fig. 12. Total power loss vs varying low-side deadtime ( $V_{in}=20V$ )

The relative performance of various deadtime control strategies are compared in Fig 13. The circle (o) data are measured by manually adjusting the two deadtimes to their optimal values at each operating point. On the other hand, the cross (x) data curve corresponds to a fixed deadtime control as described above. Finally, the plus (+) data curve shows the measured efficiency using the adaptive deadtime control. A possible explanation for the relatively high measured loss at 50% load with the fixed deadtime strategy is that the selected deadtime was actually somewhat too short. This illustrates the difficulty in precisely tuning a deadtime for a given application. One actually needs fairly precise circuit parameter data, as well information on the range of operating conditions.

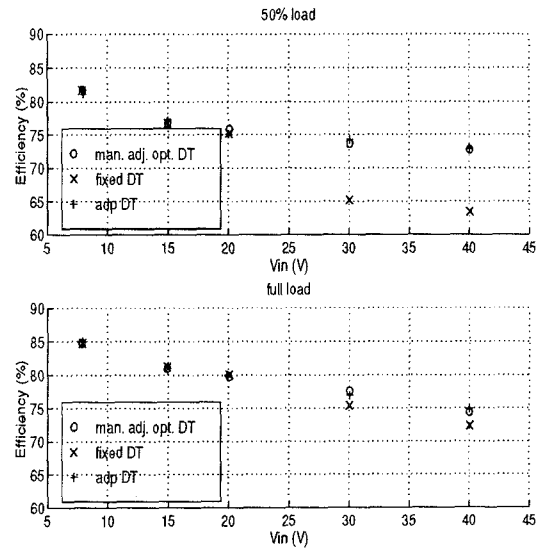


Fig. 13. Efficiency vs input voltage of the buck converter. Top: 50% load. Bottom: full load.

Oscilloscope photos of steady state waveforms for the circuit operating with the adaptive deadtime control are displayed in Fig. 14 and 15.

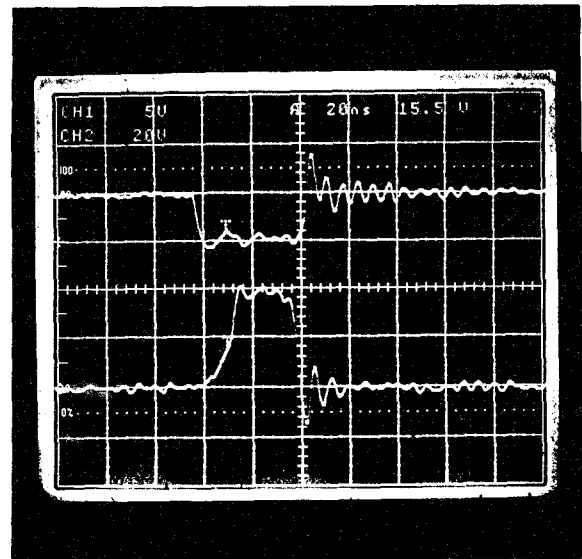


Fig. 14. Measured steady-state waveforms with adaptive deadtime control. Top: NMOS gate waveform,  $V_{g2}$  (5V/div). Bottom: inverter node waveform,  $V_x$  (20V/div). The horizontal scale is 20ns/div.



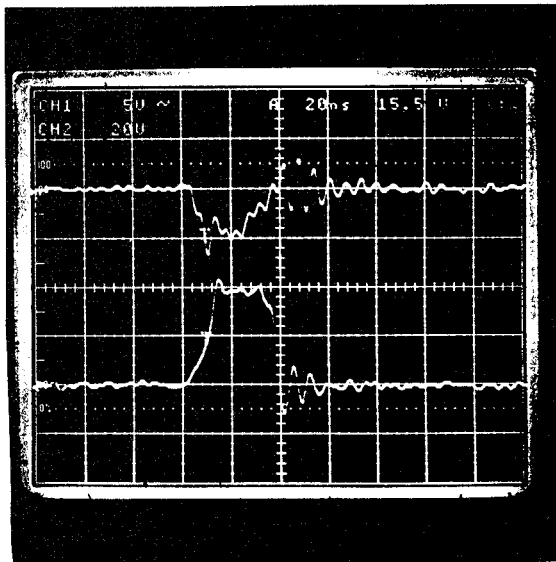


Fig. 15. Measured steady-state waveforms with adaptive deadtime control. Top: PMOS gate waveform,  $V_{g1}$  (5V/div). Bottom: inverter node waveform,  $V_x$  (20V/div). The horizontal scale is 20ns/div.

## V. CONCLUSION

This paper reported on the design, fabrication, and test of a controller IC for a buck converter, designed to operate in a constant off-time, variable frequency mode. This mode is advantageous to support soft-switching over a wide input voltage range. Operation up to 5MHz allows potential use with a microfabricated inductor. Considerable attention was paid to the control of deadtimes. Specifically, the adaptive deadtime scheme proposed in [3] was fully implemented and tested.

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