Phase Current Unbalance Estimation in Multiphase Buck Converters

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***Abstract*—A method for estimating the phase current unbalance in a multiphase buck converter is presented. The method uses the information contained in the voltage drop at the input capacitor's effective series resistance (ESR) to estimate the average current in each phase. Although the absolute estimation of the currents depends on the value of the ESR and is therefore not absolutely accurate, the relative estimates of the currents with respect to one other are shown to be very accurate. The method can be implemented with a low-rate down-sampling A/D converter and is not computationally intensive. Experimental results are presented, showing good agreement between the estimates and the measured values.**

***Index Terms*—Current sensing, current sharing, dc/dc converters, multiphase buck converter, voltage regulation modules (VRM).**

I. Introduction

THE multiphase synchronous buck converter is the topology of choice for low-voltage high-current dc/dc converter applications [1]–[7]. The advantages of this topology are numerous. In a converter with N phases the ripple frequency is Nf_s, where f_s is the switching frequency of each phase, therefore both the ripple is reduced and the requirements of the input and output filters are relaxed. Each switch and inductor conducts N times less current than in an equivalent conventional buck converter. Finally, there are more opportunities of control in one clock cycle, meaning that the delay in the control loop gets reduced and a higher bandwidth can be achieved.

However, the multiphase topology requires more components and a more complex controller. Furthermore, there is a potential problem with current unbalance. The thermal constraints as well as the dimensioning of the semiconductors and inductors of each phase depend on the maximum current they deliver. If all phases are balanced, the maximum phase current is equal to the maximum load current divided by N. However, small variations in the characteristics of each phase could generate a significant current unbalance, leading to the need to over design the components. Additionally, if the currents are not balanced properly, frequency components below Nf_s are present in the input current. In conclusion, many of the advantages of the multiphase topology are lost if the currents are not balanced.

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The topic of current sharing has been widely studied in the context of paralleling dc/dc converter modules (see, for example [8]–[10] and references therein). In general, it is assumed that individual current measurements are available and the information is shared among the converters. In [8], a master-slave approach is presented. In [9], the average inductor current information is shared among the converters. In [10], the information contained in the switching ripple is used. A classification of paralleling schemes and current-sharing methods can be found in [11].

In a multiphase topology, the challenges are similar but the controller usually only needs the total current and not the individual phase currents for achieving a good dynamic response. As a consequence, for phase balancing purposes, auxiliary and lower-resolution phase current measurement circuits are employed. The most common phase-balancing methods in commercial high-current applications use phase current measurements obtained by inductor sensing [2]–[4] or R_{DS} sensing [5]–[7]. Both methods require *a priori* knowledge of a parasitic series resistance (inductor DCR in the former and MOSFET R_{DS} in the latter) for each phase and need to track its variation with temperature. Other approaches have been proposed, like an inductor sensing variation [12] and a hysteretic control method [13].

In [14] and this work, a method for estimating the current unbalance based on samples of the input voltage is described. The merit of this approach is that the same sensing element [the input capacitor effective series resistance (ESR)] is used for all phases, thus eliminating the uncertainty when comparing measurements for different phases. Further, variations of the ESR value with temperature, frequency, and other parameters do not affect the relative measurement of the phase currents with respect to one another. In [14], the input voltage is sampled directly during the conduction time of each phase, and the samples are compared to obtain the unbalance information. However, the input voltage carries a lot of undesired high-frequency content due to the switching of large currents, dramatically reducing the signal-to-noise ratio (SNR) of the sampled values, rendering the method impractical. Furthermore, if the on-times of the different phases superpose (duty-cycle greater than $1/N$), the samples are not useful.

In this paper, a different approach for sampling the voltage input waveform is presented. Instead of relying on the instantaneous values of the waveform, a frequency analysis is performed on a filtered version of the waveform. This approach results in a much better SNR. A linear relationship between the sampled waveform and the amplitude of the phase currents is derived. The numerical processing required is equivalent to a low-order matrix-vector multiplication or a low-order fast Fourier transform (FFT), and needs to be updated at a slow rate. With the

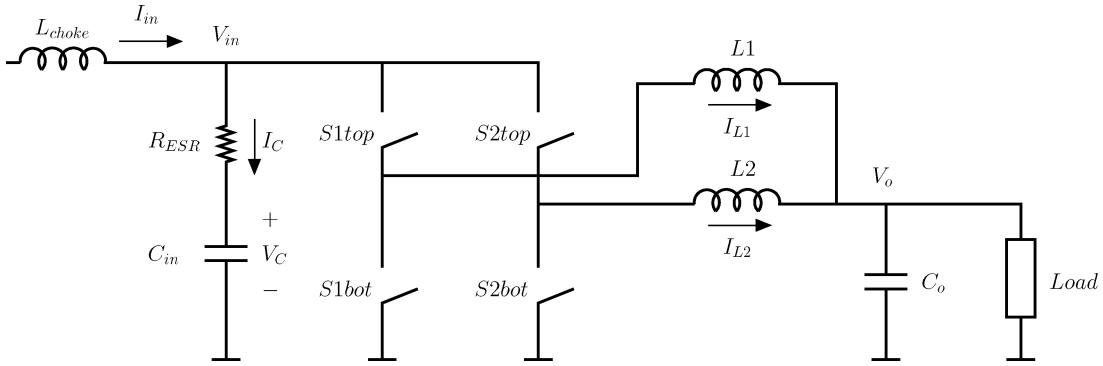

Fig. 1. Two-phase buck converter. The input capacitor's ESR is shown explicitly.

increasing popularity of digital capabilities in dc/dc controllers, this functionality is not difficult nor costly to implement.

As described above, this method uses the input capacitor ESR as a unique sensing element for all phases. Therefore, the relative relationship of the phase currents' estimates with respect to one another is accurate, although the absolute value still carries the uncertainty in the value of the sensing element. The unbalance information can be used in an active current sharing method to achieve good current sharing among all phases.

This paper is organized as follows. The current unbalance estimation method is described in Section II. Some practical considerations are addressed in Section III. Finally, experimental results are reported in Section IV.

II. Method Description

The main idea behind the method comes from the understanding of the waveform at the input voltage of a multiphase buck converter. In Fig. 1 a buck converter with two phases is shown to illustrate the derivation of the method. Usually the input current $I_{\rm in}$ has a very small ac component due to the presence of an inductor (choke). Therefore, the ac component of the current through the top switch (e.g., $S1top$) is provided by the input capacitor $C_{\rm in}$, creating a voltage drop on its ESR that is proportional to the inductor current during the conduction time of the corresponding phase. This creates a perturbation on the input voltage $V_{\rm in}$. Since the conduction time of the phases is multiplexed in time, the resulting $V_{\rm in}$ waveform contains the information of the dc amplitude of each of the phase currents. This is illustrated in Fig. 2. In this particular example, the average current in phase 2 is larger than in phase 1. Given that the difference in the phase currents can be inferred directly from the waveform, it could be argued that sampling the input voltage during the conduction time of each phase could provide the unbalance information. Unfortunately, the samples taken of this waveform are noisy, so this approach becomes impractical. Additionally, in some cases the conduction times of different phases could overlap (for example with a duty-cycle larger than 50% in a two-phase system). For these reasons, it is more practical to analyze the harmonic content of the waveform, as will be described next.

In general, for a buck converter with N phases

$$V_{\rm in} = V_C + R_{\rm ESR} I_C \tag{1}$$

$$I_C = I_{\rm in} - \sum_{i=1}^{N} u_i I_{Li} \tag{2}$$

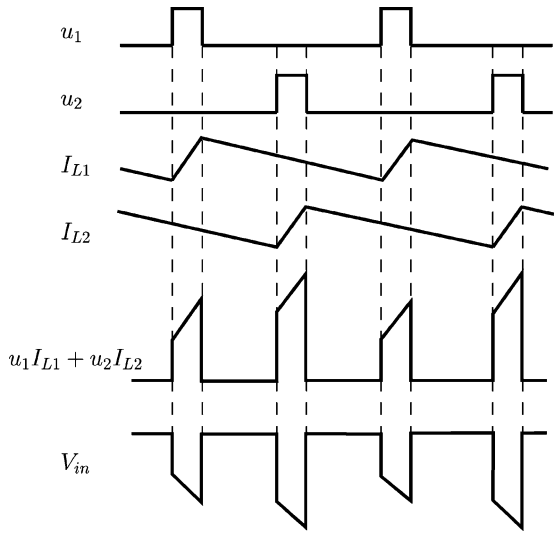

Fig. 2. Voltage and current waveforms in a two-phase buck converter with unbalanced currents.

and then, combining (1) and (2)

$$V_{\rm in} = V_C + R_{\rm ESR} I_{\rm in} - R_{\rm ESR} \sum_{i=1}^{N} u_i I_{Li} \tag{3}$$

where

$$u_i(t) = \begin{cases} 1, & \text{if } Sitop \text{ is ON} \\ 0, & \text{if } Sitop \text{ is OFF} \end{cases}, \quad \text{for } i = 1 \ldots N.$$

As mentioned above, in steady-state operation the input current $I_{\rm in}$ can be considered constant. The purely capacitive voltage V_C can also be considered constant as long as the time constant $R_{\rm ESR} C_{\rm in}$ is such that the capacitor impedance behaves resistively at the switching frequency. If that is not the case, as could happen with ceramic capacitors, then an extra circuit as depicted in Fig. 3 can be used to eliminate the variations due to the charging/discharging of the capacitor. This circuit works as follows. The voltage V_s can be expressed in terms of the current I_C

$$V_s = \frac{R_s C_s s}{R_s C_s s + 1} V_{\rm in} \tag{4}$$

$$V_{\rm in} = \frac{R_{\rm ESR} C_{\rm in} s + 1}{C_{\rm in} s} I_C \tag{5}$$

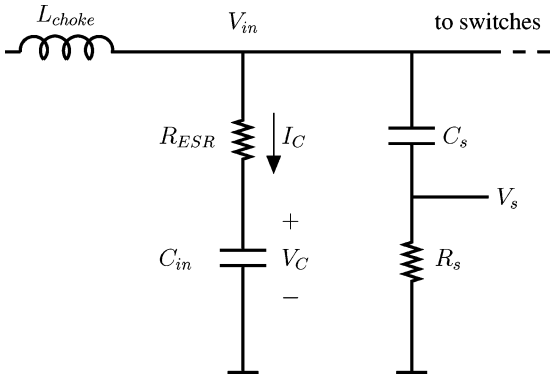

Fig. 3. Capacitor current sensing.

$$\Rightarrow \quad V_s = \frac{R_{\rm ESR}C_{\rm in}s+1}{R_sC_ss+1}\frac{R_sC_s}{C_{\rm in}}I_C \tag{6}$$

If the RC time constants of the two branches are equal (i.e., $R_{\rm ESR}C_{\rm in} = R_sC_s$), then

$$V_s(t) = R_{\rm ESR}I_C(t). \tag{7}$$

Substituting I_C from (2), it is concluded that

$$V_s = R_{\rm ESR}I_{\rm in} - R_{\rm ESR}\sum_{i=1}^{N} u_iI_{Li}. \tag{8}$$

Notice that this waveform is the same as the input voltage, but without the capacitor voltage V_C. This means that not only are the variations in the capacitor charge excluded, but also that the dc component is eliminated, making the waveform voltage levels more suitable for sampling. If $C_s \ll C_{\rm in}$, the effect of adding this circuit to the converter is negligible. In the following derivations, it will be assumed that the waveform to be processed is $V_s(t)$ and not $V_{\rm in}(t)$.

The relative amplitude of the phase currents will be reflected in the harmonic content of the waveform $V_s(t)$, in particular in frequencies kf_s for $k = 1 \ldots N-1$, where f_s is the switching frequency. For perfectly balanced operation, the V_s waveform would have zero content at these frequencies. In the case illustrated in Fig. 2, $V_{\rm in}(t)$ (or equivalently, V_s) has a harmonic component at frequency f_s due to the difference in the average current in the two phases. It is easy to see that the lowest harmonic frequency present in a two-phase balanced circuit would be $2f_s$. It will be shown below that frequencies above $(N-1)f_s$ can be eliminated without losing the unbalance information, allowing for the sampling of a "clean" waveform, without all the high-frequency content usually present at the input voltage node.

The harmonic content of V_s can be computed by using the Fourier series expansion of a pulse train, and applying the time-shift and superposition properties. A pulse train of amplitude one and duty cycle D (Fig. 4) has the following Fourier coefficients:

$$c_0^{PT} = D \tag{9}$$

$$c_k^{PT} = c_{-k}^{PT} = D\cdot\frac{\sin k\pi D}{k\pi D}. \tag{10}$$

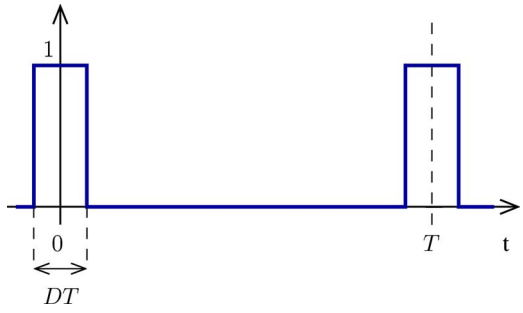

Fig. 4. Pulse train.

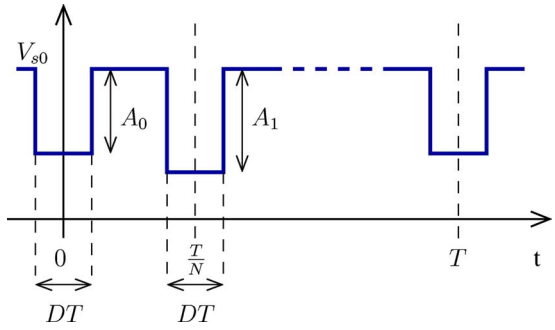

Fig. 5. Waveform $V_s(t)$ as a superposition of pulse trains.

The time origin is located at the middle of the pulse. Notice that it is sufficient to do the computation with a rectangular pulse, and not a trapezoidal one as in Fig. 2, because the higher frequency components are of no interest since the method relies on lower frequency harmonics.

The waveform $V_s(t)$ can be expressed as a constant term $V_{s0} = R_{\rm ESR}I_{\rm in}$, minus the sum of N pulse trains of amplitude A_m time-shifted by mT/N, $m = 0 \ldots N-1$ (Fig. 5). The results are general and valid even if the pulses overlap (i.e., $D > 1/N$). Then, the Fourier series expansion of $V_{\rm in}(t)$ is

$$V_s(t) = \sum_{k=-\infty}^{+\infty} c_k e^{jk\omega t} \tag{11}$$

where the Fourier coefficients can be obtained from (9) and (10), applying the time-shift and superposition properties

$$\begin{aligned} c_0 &= V_{s0} - c_0^{PT}\cdot\sum_{m=0}^{N-1} A_m \\ &= V_{s0} - D\cdot\sum_{m=0}^{N-1} A_m \end{aligned} \tag{12}$$

$$\begin{aligned} c_k &= -c_k^{PT}\cdot\sum_{m=0}^{N-1} A_m e^{-j\frac{2\pi km}{N}} \\ &= -D\cdot\frac{\sin k\pi D}{k\pi D}\cdot\sum_{m=0}^{N-1} A_m e^{-j\frac{2\pi km}{N}}. \end{aligned} \tag{13}$$

The first N Fourier coefficients from (12) and (13) can be written in a more compact form as

$$\mathbf{c} = V_{s0}\mathbf{e_1} - \mathbf{P_D}\mathbf{S_N}\mathbf{a} \tag{14}$$

where

$$\begin{aligned}
\mathbf{c} &= [c_0 \quad c_1 \quad \cdots \quad c_{N-1}]^{\mathsf{T}} \\
\mathbf{e_1} &= [1 \quad 0 \quad \cdots \quad 0]^{\mathsf{T}} \\
\mathbf{P_D} &= D \cdot \operatorname{diag}\left[1 \quad \tfrac{\sin \pi D}{\pi D} \quad \cdots \quad \tfrac{\sin (N-1)\pi D}{(N-1)\pi D}\right] \\
\mathbf{S_N} &= \begin{bmatrix} W_N^0 & W_N^0 & \cdots & W_N^0 \\ W_N^0 & W_N^1 & \cdots & W_N^{N-1} \\ W_N^0 & W_N^2 & \cdots & W_N^{2(N-1)} \\ \vdots & \vdots & & \vdots \\ W_N^0 & W_N^{N-1} & \cdots & W_N^{(N-1)(N-1)} \end{bmatrix} \\
W_N &= e^{-j\frac{2\pi}{N}} \\
\mathbf{a} &= [A_0 \quad A_1 \quad \cdots \quad A_{N-1}]^{\mathsf{T}}.
\end{aligned}$$

Notice that $\mathbf{S_N}$ is the discrete Fourier transform (DFT) matrix which is invertible, with inverse $(1/N)\mathbf{S_N^*}$ [15].

Now the problem of computing the Fourier coefficients from a sampled version of the waveform $V_s(t)$ is addressed. Let $x_k = V_s(kT_{\text{samp}})$, where $T_{\text{samp}} = 1/(2Nf_s)$, i.e., the waveform is sampled at $2N$ times the switching frequency. The waveform should be filtered with a lowpass antialiasing filter with a cut-off frequency equal to Nf_s for full recovery of the low frequency harmonics. Then, the relationship between the Fourier coefficients of the continuous-time signal and the sampled values is given by the DFT [15]

$$\begin{aligned}
\mathbf{c}' &= \frac{1}{2N}\mathbf{S_{2N}}(1:N, 1:2N)\mathbf{x} \\
&= \tilde{\mathbf{S}}_{\mathbf{2N}}\mathbf{x}
\end{aligned} \tag{15}$$

where $\mathbf{x} = [x_0\ x_1\ \cdots\ x_{2N-1}]^{\mathsf{T}}$, and the $2N$-point DFT matrix is truncated to ignore the negative-frequency components, generating $\tilde{\mathbf{S}}_{\mathbf{2N}}$. The prime notation is used to emphasize that these are the Fourier coefficients of the voltage waveform that is actually sampled. This waveform is different from the input voltage waveform used to derive (14) in two aspects. First, there is a distortion introduced by the antialiasing filter, and second, there is a phase shift introduced if the sampling is not performed synchronized with the time origin used to derive (14). These two effects are deterministic and easy to characterize as follows.

The presence of a lowpass filter before the sampling process may introduce an amplitude and phase distortion in the waveform, that can be taken into account by introducing a correction matrix $\mathbf{C}$ that includes the transfer function of the filter evaluated at the frequencies of interest

$$\mathbf{C} = \operatorname{diag}\left[H(0) \quad H(2\pi f_s) \quad \cdots \quad H\left((N-1)2\pi f_s\right)\right] \tag{16}$$

where $H(\omega)$ is the frequency response of the lowpass filter.

In order to be consistent with the derivation of the Fourier coefficients in (10), the origin $t = 0$ has to be positioned at the middle of the conduction time of the phase associated with amplitude A_0. It is usually more convenient for the sampling synchronization to position the origin at the beginning of the conduction period. This would, according to the time-shift property, introduce a phase-shift of $k\pi D$ for each Fourier coefficient c_k, that can be summarized in a correction matrix $\mathbf{R}$ defined as

$$\mathbf{R} = \operatorname{diag}\left[1 \quad e^{-j\pi D} \quad \cdots \quad e^{-j(N-1)\pi D}\right]. \tag{17}$$

Then, combining both effects, the relationship between the Fourier coefficients of the sampled waveform and the ideal one is

$$\mathbf{c}' = \mathbf{RCc}. \tag{18}$$

Combining (14), (15), and (18), we obtain

$$\tilde{\mathbf{S}}_{\mathbf{2N}}\mathbf{x} = \mathbf{RC}(V_{s0}\mathbf{e_1} - \mathbf{P_D}\mathbf{S_N}\mathbf{a}) \tag{19}$$

yielding the vector of phase current amplitudes

$$\mathbf{a} = \mathbf{S_N^{-1}}\mathbf{P_D^{-1}}(V_{s0}\mathbf{e_1} - \mathbf{C^{-1}}\mathbf{R^{-1}}\tilde{\mathbf{S}}_{\mathbf{2N}}\mathbf{x}). \tag{20}$$

Since the objective is to estimate the current unbalance, the difference of each amplitude with respect to the average is derived as

$$\mathbf{a_{diff}} = \mathbf{a} - \frac{1}{N}\mathbf{1}\mathbf{1}^{\mathsf{T}}\mathbf{a} \tag{21}$$

where $\mathbf{1} = [1\ 1\ \cdots\ 1]^{\mathsf{T}}$. Finally, combining (20) and (21), it is concluded that

$$\begin{aligned}
\mathbf{a_{diff}} &= -\left(\mathbf{I} - \frac{1}{N}\mathbf{1}\mathbf{1}^{\mathsf{T}}\right)\mathbf{S_N^{-1}}\mathbf{P_D^{-1}}\mathbf{C^{-1}}\mathbf{R^{-1}}\tilde{\mathbf{S}}_{\mathbf{2N}}\mathbf{x} \\
&= \mathbf{M_{N,D}}\mathbf{x}.
\end{aligned} \tag{22}$$

Notice that the term involving the dc component of the input voltage gets canceled, confirming that it is irrelevant for the unbalance estimation.

The current unbalance estimation problem was reduced to a linear transformation of a $2N$-dimensional vector into an N-dimensional one. This transformation can be accomplished by a matrix-vector multiplication. The matrix $\mathbf{M_{N,D}}$ only depends on the number of phases, the steady-state duty-cycle, and the characteristics of the antialiasing filter, so it would be constant for most applications.

The vector $\mathbf{a_{diff}}$ does not need to be computed every switching period because the current unbalance does not change very fast. Actually, it could be recomputed once every few milliseconds, every few seconds, or much less frequently depending on the application. For this reason, this estimation method does not require much computation power.

III. Method Implementation

The implementation of this current unbalance estimation technique requires sampling the input voltage waveform and digital processing of the samples obtained. In this section, some practical aspects of the implementation are addressed.

A. Sampling the Input Voltage Waveform

As stated above, the dc value of the input voltage is not relevant for estimation purposes. Moreover, the common-mode

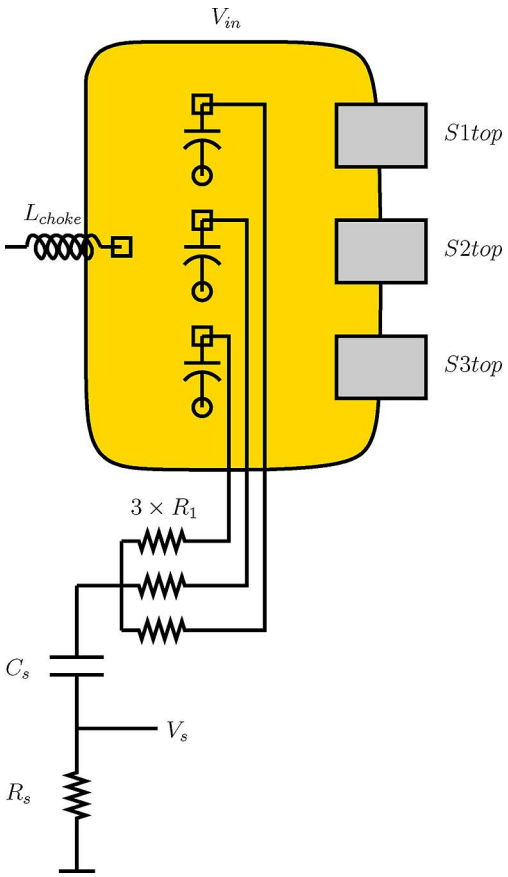

Fig. 6. Capacitor current sensing using the resistive averaging technique. A similar arrangement can be used at the ground node if necessary. Example with three phases.

voltage of this waveform may be beyond the range of the controller integrated circuit (IC) technology. The sensing circuit shown in Fig. 3 not only eliminates the fluctuations in the capacitor charge but also suppresses the dc voltage acting as a passive high-pass filter.

Another practical issue arises when the input capacitor consists of several pieces spread on the printer circuit board (PCB), usually following the spread of the different phases. During the conduction time of each phase, most of the current flows through the capacitors closer to the top switch of the corresponding phase. In order to capture all capacitors in a single voltage waveform, resistive averaging is proposed as shown in Fig. 6 for the case of a three-phase circuit. If the resistor values are small, namely $R_1 \ll NR_s$, then this circuit is equivalent to the one in Fig. 3, but now the average of the voltages in all capacitors is sensed.

The waveform also needs to be filtered with a lowpass antialiasing filter, with a cutoff frequency equal to Nf_s. This can be done with an active filter inside the controller chip.

There need to be $2N$ samples per switching period. The sampling rate however can be arbitrarily reduced by undersampling, as long as the converter is approximately in steady-state. For example, instead of acquiring all the samples in one switching period, the first sample could be acquired in one period, the second sample in the following period, and so on. Since the waveform is stationary, the result is equivalent.

TABLE I
NUMBER OF OPERATIONS FOR TWO ESTIMATION METHODS

	Matrix Method		FFT Method	
N	additions	multiplications	additions	multiplications
4	28	32	116	80
8	120	128	308	208
16	496	512	764	512
32	2,016	2,048	1,820	1,216

Although the derivation assumes $2N$ samples per switching period, this is the minimum needed. More samples per period can be taken, relaxing the requirements for the antialiasing filter at the expense of a faster sampling rate and more computation. The only change needed to contemplate more samples is to generate a new matrix $\tilde{\mathbf{S}}_{\mathbf{2N}}$ equal to $\tilde{\mathbf{S}}_{\mathbf{K}} = (1/K)\mathbf{S}_{\mathbf{K}}(1:N, 1:K)$, where $K > 2N$ is the number of samples.

If there is a transient between samples, the estimated unbalance information would not be correct. Given that the time constant of the changes in the current unbalance is large compared to the dynamics of the system, the output of this estimation method could be filtered digitally to smooth out the errors due to transients. This would particularly be the case if the estimated unbalance information is used to balance the circuit in a closed-loop active balancing system with low bandwidth.

B. Computation

Once the samples are available, all the computation that is needed is given by the linear transformation (22), that amounts to the multiplication of a complex-valued N-by-$2N$ matrix by a real-valued vector of length $2N$. Since the results are ideally real numbers (the vector of amplitudes $\mathbf{a_{diff}}$), then the imaginary parts can be ignored because in the end they will add up to zero. The operations needed for obtaining the results are $2N^2$ multiplications and $2N^2 - N$ additions.

Alternatively, the form given in (22) indicates that the transformation is comprised of a $2N$-point DFT ($\tilde{\mathbf{S}}_{\mathbf{2N}}$), followed by a diagonal multiplication ($\mathbf{P_D^{-1}C^{-1}R^{-1}}$), an N-point inverse DFT (IDFT) ($\mathbf{S_N^{-1}}$), and the calculation of the difference of each component with the average. It could be appropriate to use FFT techniques to obtain a more efficient implementation of this transformation. The computation would have four steps. Each M-point DFT or IDFT step implemented with Radix-2 FFT algorithms requires $(M/2)\log_2 M$ complex multiplications and $M \log_2 M$ complex additions [15], where M is equal to $2N$ in one case and N in the other. The diagonal matrices add N complex multiplications. Finally, the average and difference computations contribute $2N - 2$ real additions. The total is then $N((3/2)\log_2 N + 2)$ multiplications and $N(3\log_2 N + 4) - 2$ additions. Most of these are complex, although with some clever manipulations some could be reduced to real operations. Assuming no reduction is performed, each complex multiplication is equivalent to four real multiplications and two real additions, and each complex addition is equivalent to two real additions.

The two computation methods are compared in Table I. It is evident that the FFT method is more efficient only for a large number of phases. It is concluded that the matrix-vector multiplication method should be used in most practical cases.

TABLE II
VRM EVALUATION BOARD CHARACTERISTICS

Component/Parameter	Value
# phases	3
f_{sw}	$243kHz$
D	0.11
V_{in}	$12V$
L_{choke}	$630nH$
C_{in}	$6 \times 470\mu F$
R_{ESR}	$18m\Omega/6$
top switch	FDD6296
bottom switch	2×FDD8896

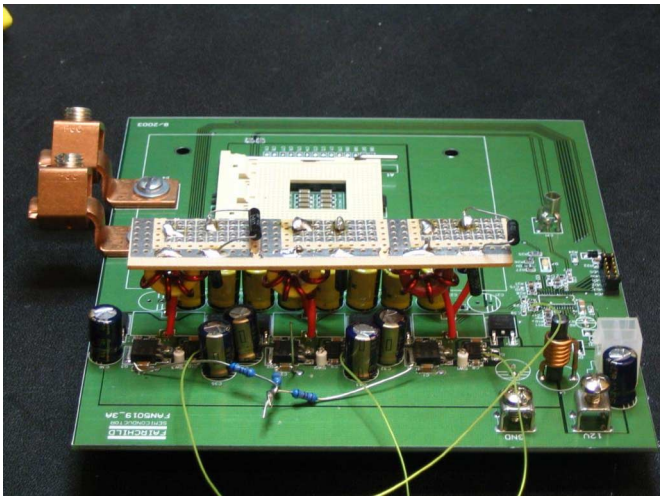

Fig. 7. Experimental setup.

In some applications, the matrix $\mathbf{M_{N,D}}$ can change due to its dependence on the steady-state duty-cycle D. If those changes are substantial, several matrices can be precomputed and in every computation cycle the appropriate one is selected corresponding to the duty-cycle during the acquisition time. It should be noted also that the inversion of matrix $\mathbf{P_D}$ is not possible if $kD \approx 1$ for $k \in [1, 2, \ldots, N-1]$. In this case, the algorithm should be modified to exclude the problematic harmonic and to instead include higher harmonics to the equation until the problem becomes well-conditioned.

IV. EXPERIMENTAL RESULTS

A three-phase evaluation board for a commercial VRM (FAN5019_3A of Fairchild Semiconductor, whose main characteristics are listed in Table II) was used as a test-bed for this concept. The power train was run in open loop, and different distributions of the load current among the three phases were created by inserting small resistors of different values in series with the inductors. Since the time constant of the input capacitor was large with respect to the switching period, no capacitor current sensing circuit was used, but the input voltage waveform was captured with a digital oscilloscope in ac-coupling mode. The resistive averaging technique (see Fig. 6) was used to average the input voltage at the capacitors located next to each phase. It was noted that symmetry of the

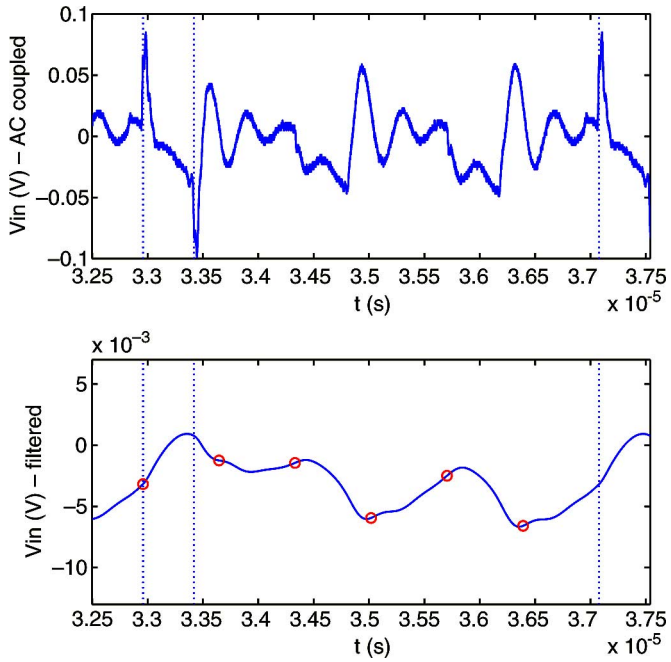

Fig. 8. Input voltage waveform in a three-phase buck converter. Top: before filtering; Bottom: after filtering. The vertical lines indicate the timing of phase one. The circles indicate the samples.

layout was critical to obtain good data. The evaluation board with the modifications described is shown in Fig. 7.

The data processing, including the antialiasing filter and sampling, was performed numerically in a PC. Eleven series of data were taken with each series corresponding to a specific distribution of the phase currents. Fig. 8 shows an example of the sampled input voltage waveform before and after the antialiasing filter, and the samples. In this figure, the benefits of filtering the signal before sampling are evident, since much of the high frequency content is eliminated.

Fig. 9 shows the estimation results. The figure is a plot obtained from eleven triplets of data, each comprising three phase current measurements and corresponding estimates. For each data point, the horizontal coordinate indicates the measured deviation value of the current, relative to the nominal average of 4 A per phase. For this same point, the vertical coordinate indicates the estimated value. The estimated currents were derived by dividing $\mathbf{a_{diff}}$, as derived in (22), by the nominal value of the input capacitor ESR. Since this value has a lot of uncertainty, the points are not aligned with the diagonal $y = x$ but with a line with a smaller slope. However, the agreement between the estimates and the actual values is good. The estimation error is within 0.7 A. As a reference, the total current was 12 A, averaging 4 A per phase. The rated current per phase in this circuit is 35 A, thus the error is on the order of 2% of full scale. Moreover, if the information is intended to be used as part of an active current balancing system then the sign of the current unbalance is of the most importance, therefore the uncertainty in the ESR value is a second order effect.

V. CONCLUSION

A method for estimating the phase current unbalance in a multiphase buck converter was presented. The method is based

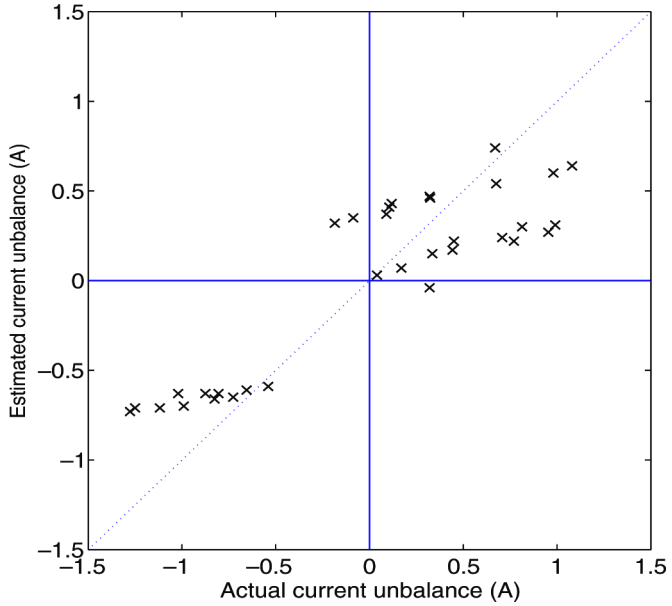

Fig. 9. Experimental results: estimated unbalance versus actual unbalance. Unbalance current is defined as the difference between the phase current and the average over all phases. The figure shows eleven series of data with three points each, corresponding to the three phases. Ideally, all points should be on the diagonal.

on the frequency analysis of the input voltage ripple and requires a low-order matrix-vector multiplication. The most relevant implementation issues are the sampling of the input voltage and the real-time computation of the results. Both issues were discussed and engineering solutions were presented. The accuracy of the method was assessed in an experimental setup that allows to introduce arbitrary phase unbalance conditions, capture the input voltage waveforms, and perform the computation off-line. Experimental results show good agreement between measured and estimated phase current deviations with respect to the average. The estimated values can be used in an active balancing method to achieve good current sharing among all phases.

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