High Precision Load Current Sensing using On-Line Calibration of Trace Resistance in VRM Applications

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Abstract— **A method for the on-line calibration of a circuit board trace resistance at the output of a buck converter is described. The input current is measured with a precision resistor and processed to obtain a DC reference for the output current. The voltage drop across a trace resistance at the output is amplified with a gain that is adaptively adjusted to match the DC reference. This method is applied to obtain an accurate and high-bandwidth measurement of the load current in the modern microprocessor voltage regulator application (VRM), thus enabling an accurate DC load-line regulation as well as a fast transient response. Experimental results show an accuracy well within the tolerance band of this application, and exceeding all other popular methods.**

I. Introduction

Voltage regulators for modern microprocessors (VRMs) pose unprecedented demands on DC-DC power converters, in terms of regulation, bandwidth, and cost [1]. Adaptive voltage positioning (AVP), also known as load-line regulation, was adopted as an effective technique to reduce the amount of capacitance at the output [2]. This technique requires the output voltage to change with the load current, as if the output impedance of the power converter were a resistor of small value (around $1m\Omega$). The controller can be designed to make the effective closed-loop output impedance resistive, or to meet another desired specification, over a wide frequency range, by processing the output current information [2].

For this reason, and due to the tight regulation window required by the application, a precise and high-bandwidth measure of the output current is needed. Existing current-sensing techniques are [3], [4]: (1) series sense resistor at the output, (2) MOSFET R_{DS} sensing, (3) inductor sensing, (4) series sense resistor at the input, and (5) SENSEFET. An on-line calibration method for MOSFET R_{DS} sensing that requires additional power train components, was described in [5]. An observer-based approach requiring intensive numerical processing was reported in [6]. For efficiency, cost, and relative accuracy, inductor sensing is the preferred method at the present time [1], although it has the disadvantage that both the effective series resistance and the L/R time constant of the inductor need to be known and tracked as they change with temperature.

Most of the methods described sense the inductor current, which has the same DC value as the output current, and tracks it well up to the closed-loop bandwidth of the converter. In designs with electrolytic capacitors, the output capacitor's ESR is chosen to be equal to the desired output impedance, as given by the load-line specification. This allows the converter to follow the load-line ideally at an arbitrary high bandwidth [2]. However, if ceramic capacitors are used the ESR is substantially lower than the load-line impedance rendering the previous design method impractical. The concept of generalized load-line was introduced [7] as a practical design objective for VRM systems with ceramic capacitors. The bandwidth in such a system is given by the time constant $\tau = R_{LL}C_o$ where R_{LL} is the desired load-line and C_o is the output capacitor value. In some cases it could be very difficult to follow the load-line over this frequency range, especially as C_o is decreased to reduce costs. In order to enhance load-line tracking without pushing the feedback bandwidth close to instability, output current feedforward was proposed [7]. In this case, the inductor current information is not useful and the load current must be sensed. In [7] the authors used inductor sensing plus a similar technique to sense the output capacitor current, and combined both to obtain the output current. Thus, the method used poses the same practical challenges as inductor sensing.

Ideally, a VRM system would include an output current sensing circuit with the following characteristics:

1) accurate in spite of uncertain elements
2) high-bandwidth
3) power-efficient
4) low-cost, implying among other things a low part count and a low pin count in the controller IC

This paper presents a method that approaches these ideal conditions. The method senses the output current by using the output trace resistance (or any parasitic resistance at the output of the converter) as a sensing element. The value of the trace resistance is calibrated on-line by a slow estimation loop. The estimation algorithm is based on the DC correspondence between the output current and the input current. The latter is accurately measured with a sense resistor and used as a reference. This method can

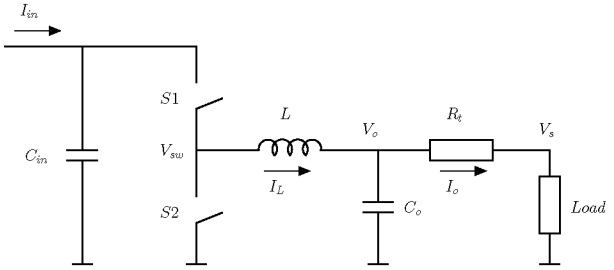

Fig. 1. Buck converter

achieve high-accuracy and high-bandwidth measurement of the output current with a small efficiency penalty due to the input-side resistor. Further, the measured input current may be useful for control purposes.

II. Method Description

Fig. 1 shows a buck converter. The output trace resistance is shown explicitly as element R_t. The input current I_{in} is measured by placing a sense resistor before the input capacitor. Usually an inductor is located at this place as a choke, so this current is mostly DC and free of high frequency noise. In steady-state, the average current through the input capacitor is zero, so we are effectively measuring the average current through the high-side switch. This current can be ideally expressed as uI_L, where $I_L(t)$ is the inductor current, and

$$u(t) = \begin{cases} 1, & \text{if S1 is ON} \\ 0, & \text{if S1 is OFF.} \end{cases} \quad (1)$$

We can also argue that the average current through the output capacitor is zero, so the average inductor current is equal to the average output current. Then,

$$\langle I_{in} \rangle = \langle uI_L \rangle \quad (2)$$

$$\langle I_L \rangle = \langle I_o \rangle \quad (3)$$

where $\langle \bullet \rangle$ indicates the DC or average component of the signal. In steady-state and in continuous conduction mode (CCM), it holds that

$$\langle uI_L \rangle = \langle uI_o \rangle \quad (4)$$

as illustrated in Fig. 2. Therefore, we can conclude that

$$\langle I_{in} \rangle = \langle uI_o \rangle. \quad (5)$$

This relationship establishes the basis of the on-line calibration algorithm. In Fig. 3 we show a block diagram of the estimation loop. The current sense amplifier (CSA) measures the voltage drop on the trace resistance ($V_o - V_s$). Its output is the estimated current $\hat{I}_o$. This value is multiplied by the function $u(t)$, simulating the operation of the top switch. The difference between this signal and the input current I_{in} is sent to the input of an integrator, whose output sets the gain of the CSA, therefore closing the loop and forcing the integrator to converge to the correct gain. If the gain is too low, the input of the integrator will be positive and the gain will increase, and *vice versa*. The loop will converge to set the gain such that the condition expressed in (5) is met, therefore achieving the desired result $\hat{I}_o = I_o$. The bandwidth of this adaptive tuning loop should be slow enough as to average-out the effect of switching and load transients, but fast enough to allow for tracking temperature changes. This gives a practical criteria to set the gain of the loop. A low bandwidth is also needed to guarantee the stability of the adaptive loop.

Notice that, although the adaptation loop is slow, the actual measurement of the output current is high-bandwidth, because it is given by the voltage drop $V_o - V_s$ across the passive trace resistance amplified with a variable gain amplifier.

III. Method Analysis

Some of the assumptions made in the previous section are valid only in ideal circuits. First, there are many factors that make (5) only an approximate equation. Second, the PCB trace that goes from the output capacitors to the load behaves as a two-terminal resistor only over a certain bandwidth due to parasitic elements. These issues are addressed in the following subsections.

A. Errors Due to Simplified Switching Model

In a practical implementation, (5) is only approximate. The sources of error are described below.

1) Reverse Recovery: Not all the current that goes through the high-side switch flows to the inductor. A correction has to be made to the input current information in order to reflect more accurately the inductor current. Some of the charge that flows through the high-side MOSFET ends up charging/discharging parasitic capacitances and, most importantly, are recombined in the low-side MOSFET's antiparallel diode (reverse recovery). This effect can be modeled by rewriting (2) as [8, pp. 244-247]

$$\langle I_{in} \rangle = \langle uI_L \rangle + Q_{rr} f_s + t_{rr} f_s \langle I_L \rangle \quad (6)$$

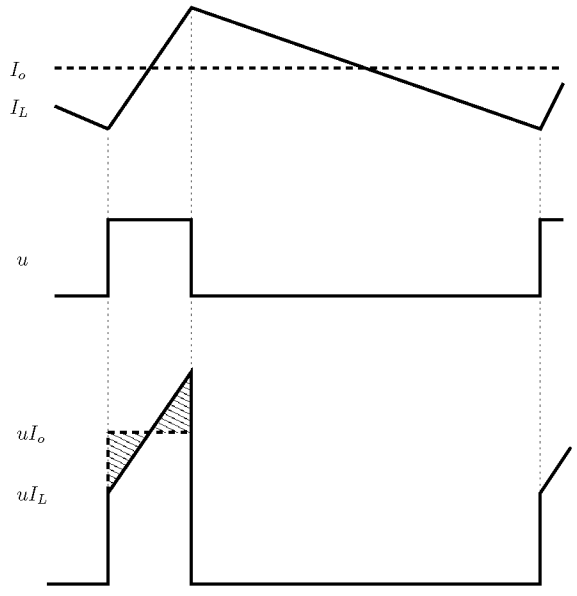

Fig. 2. In steady-state and CCM, $\langle uI_L \rangle = \langle uI_o \rangle$ because the areas of the shaded triangles are equal.

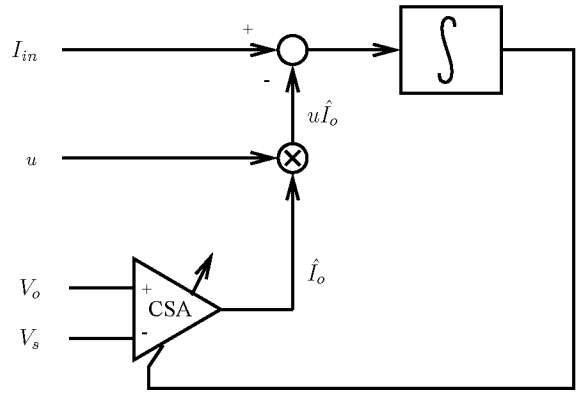

Fig. 3. Current sense amplifier with gain estimation loop.

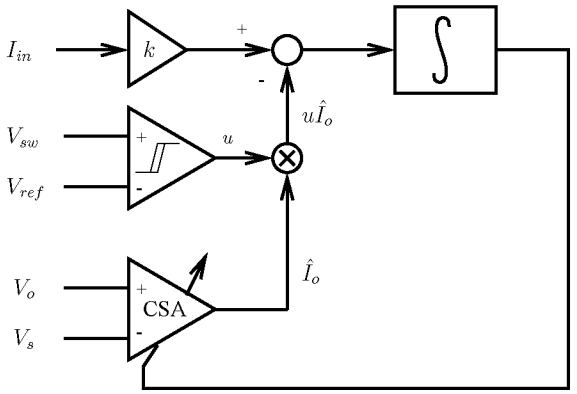

Fig. 4. Current sense amplifier with gain estimation loop, modified to contemplate non-ideal effects.

where Q_{rr} is the reverse recovery charge, t_{rr} is the reverse recovery time, and f_s is the switching frequency. This equation includes both the effect of the charge flowing to the diode and the delay in the switching node voltage due to the reverse recovery time. Rearranging terms, and introducing (4), we conclude that

$$\langle I_{in} \rangle \left(1 - \frac{t_{rr} f_s}{D}\right) - Q_{rr} f_s = \langle u I_o \rangle. \tag{7}$$

This expression is more accurate than (5), and can be easily contemplated in the estimation circuit of Fig. 3 by introducing a gain factor slightly less than unity. In practice, the constant term $Q_{rr} f_s$ is very small (comparable to the voltage offset of the amplifiers), so it can be neglected. The gain factor is represented in Fig. 4 by the block with gain $k = 1 - \frac{t_{rr} f_s}{D}$.

2) Switching Command Delay: The function $u(t)$ is an idealization of the switching action. In practice, there is a delay between the gate-drive command and the effective switching. This error can be reduced by extracting u directly from the switching node, and not from the gate-drive command. This implementation is illustrated in Fig. 4 by introducing a hysteretic comparator to sense the switching node voltage.

3) Transients: It is clear that (5) was derived under the assumption of steady-state operation, since it is based on the fact that the average current on the input and output capacitors is zero. Besides, the output voltage changes with the load due to AVP, so some of the current through the inductor goes into charging/discharging the output capacitor during load transients. However, the effect of transients on the adaptation algorithm is negligible provided that the adaptation is slow enough. The following analysis illustrates how to set bounds on the adaptation loop bandwidth.

Assume there is an output current step ΔI_o, then the average inductor current will converge exponentially to the new output current value with time constant equal to $\tau = R_d C$, where R_d is the load-line value and C is the output capacitor value [7]. During the transient, (3) is not valid, since the difference between $\langle I_o \rangle$ and $\langle I_L \rangle$ is equal to $\Delta I_o \exp^{-t/\tau}$. The integral of that difference is $A_0 \Delta I_o \tau$, where A_0 is the gain of the integrator (i.e., the transfer function of the integrator is $\frac{A_0}{s}$). If we bound the relative error due to this transient, we can write

$$\frac{A_0 \Delta I_o \tau}{1/R_t} < \epsilon \tag{8}$$

where $1/R_t$ is the ideal gain of the CSA and ϵ is the desired relative error. This equation gives the following upper bound in the integrator gain

$$A_0 < \frac{\epsilon}{\Delta I_o \tau R_t}. \tag{9}$$

For a representative VRM [1], $\Delta I_o^{\max} = 100A$, $\tau = 1\mu s$, and $R_t = 0.3m\Omega$. If we select $\epsilon = 0.5\%$, we obtain $A_0 = 165 \times 10^3$. The quantity of interest for this calculation is the loop bandwidth, that can be extracted from the circuit of Fig. 4 by linearization. The loop gain can be expressed as

$$H(s) = \frac{A_0}{s} I_o R_t D \tag{10}$$

therefore the loop bandwidth is

$$\omega_{BW} = A_0 I_o R_t D. \tag{11}$$

Notice that the bandwidth depends on the output current. The limitation in the integrator gain gives a bound in the loop bandwidth. For a typical current of $30A$, this bandwidth is

$$\omega_{BW}^{\max} = 148 rad/s \tag{12}$$

or equivalently, a time constant of $42ms$. This is fast enough to track any thermal transient.

4) Discontinuous Conduction Mode: The relationship (5) is valid only in CCM. The converter enters Discontinuous Conduction Mode (DCM) at light loads for some architectures. It is shown in Section IV that the signal is so low at light loads, that the integrator needs to be stopped to prevent a drift in the estimate, so the adaptation loop should never operate in DCM.

B. Errors Due to Lumped Resistance Model

The output trace behaves resistively over a certain frequency range, but at high frequencies the parasitics of the PCB trace make the resistive model unrealistic. This imposes a practical limit in the bandwidth of the sensing method.

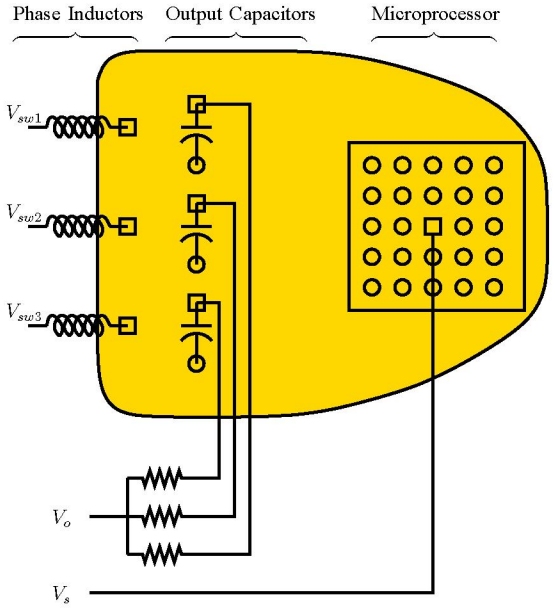

Fig. 5. Kelvin sensing technique in a 3-phase VRM.

A first-order estimation of the frequency response of two parallel copper plates in a PCB is derived in the Appendix. The trace can be approximated by an $\mathcal{LC}$ low-pass filter with a cutoff frequency equal to

$$f_c = \frac{1}{2\pi\sqrt{\varepsilon_r \varepsilon_0 \mu_0} L} \tag{13}$$

where L is the length of the trace. For a representative PCB (FR4) $\varepsilon_r = 4.7$, then the cutoff frequency can be expressed in international units as

$$f_c = \frac{22 \times 10^6}{L}. \tag{14}$$

For example, a $2cm$ trace would have a cutoff frequency of $1.1GHz$. It is safe to state that the trace will behave resistively at least up to one decade below the cutoff frequency, in our example $110MHz$. We conclude that, for all practical purposes, the parasitic dynamic components of the PCB trace will not affect the measurement of the output current.

Another potential source of error is the fact that in a practical layout the V_o node is spread since there are many output capacitors in parallel. This is especially the case in multi-phase buck converters, where the phases are kept apart for thermal considerations. The actual output trace is a wide plate of copper. The lumped resistor model might not be adequate due to the difference in the current density in different portions of the plate, which varies during transients. This can be mitigated by measuring the voltage at V_o using the Kelvin sensing technique, so as to average out the voltage at different points in the plate. The technique is illustrated in Fig. 5 for a three-phase VRM.

Finally, in a multi-phase buck converter, and under the assumption that the phase currents are balanced and the adaptation is slow enough to ignore transients, the u signal can be obtained from the switching node of any phase.

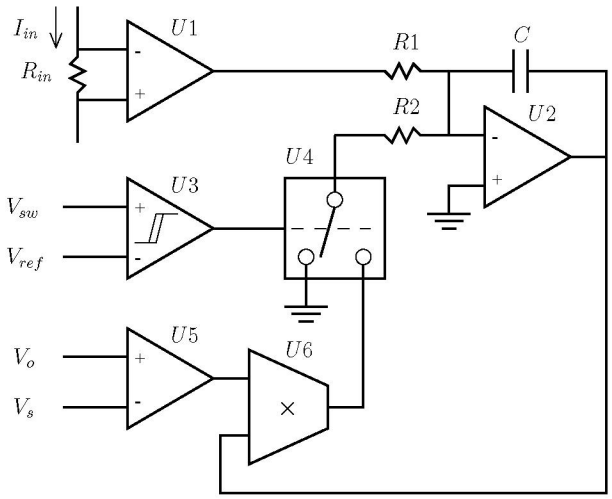

Fig. 6. Estimation breadboard schematic (simplified).

IV. Experimental Results

A prototype breadboard implementing the circuit in Fig. 4 was built using standard off-the-shelf parts. A simplified schematic of the board is shown in Fig. 6, and the main component values are shown in Table I. Notice that the factor k is implemented by changing the ratio of resistors $R1$ and $R2$. The board was connected to the 3-phase VRM evaluation board FAN5019_3A of Fairchild Semiconductor, whose main characteristics are listed in Table II. The output voltage was detected using Kelvin sensing as described above. The current estimation error was assessed at DC while the VRM board was running at different loads.

The results are shown in Fig. 7. The dotted line represents the measurements performed without adjusting the input current reference ($k = \frac{R2}{R1} = 1$). The solid line represents the measurements after trimming the gain in the input current path, accounting for the current loss due to reverse recovery. The trimming was done based on empirical observations; however the gain introduced agrees very well with the gain computed using (7) based on the MOSFET datasheet. The gain was modified by changing $R1$ to $34K\Omega$ and $R2$ to $32K\Omega$, obtaining $k = \frac{R2}{R1} = 0.94$. The computed value from the datasheet was $k = 0.93$.

The absolute error remains low for the whole range of load currents, but the relative error is high at light load. At load values below $5A$, the integrator in the estimation circuit starts to drift. This is reasonable because the signal level is too low to provide enough information, and the offset voltage of the amplifiers start to dominate the signal. The same situation arises if the converter enters DCM at light load. For these reasons, the integration should be stopped at light load in order to avoid this drift. From the results shown in Fig. 7, a threshold of $20A$ would guarantee an estimation error below 2%. To achieve this, R_t should be calibrated during operation at load currents above the threshold, and the calibration should be frozen at load currents below the threshold. Notice that, while the adaptive loop is frozen, the CSA still senses the output current with a constant gain, so

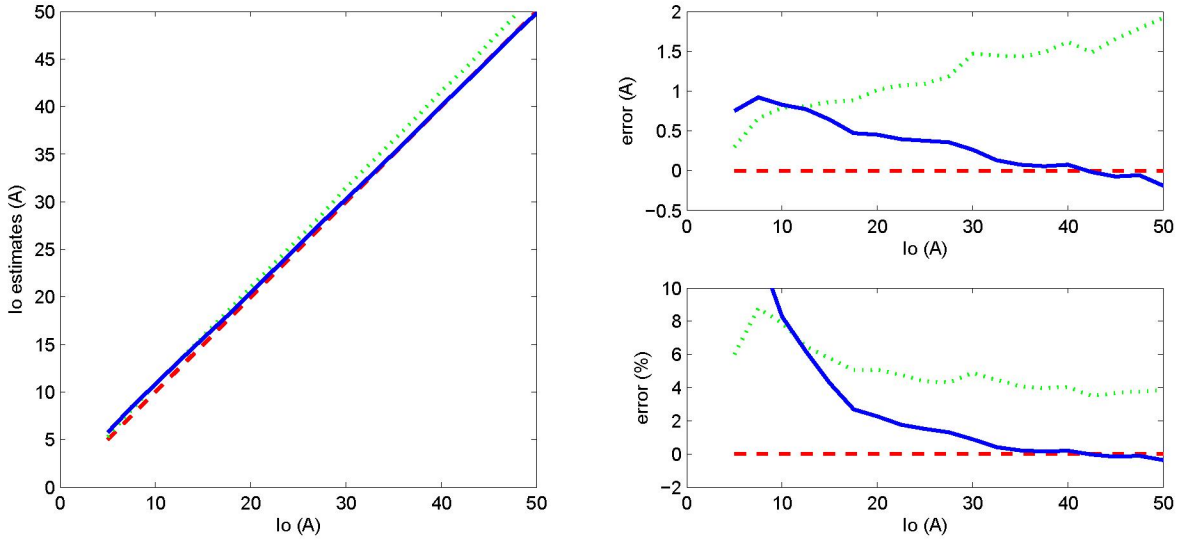

Fig. 7. Experimental measurements of the current estimation method. Left: measured values. Right: absolute (top) and relative (bottom) errors. (Dashed line: correct value; Dotted line: measurement without trimming; Solid line: measurement after trimming.)

TABLE I
BREADBOARD COMPONENTS

Component	Value
$U1$	AD623
$U2$	TL082
$U3$	AD8611
$U4$	ADG820
$U5$	AD620
$U6$	AD835
R_{in}	$10m\Omega$
$R1$	$33K\Omega$
$R2$	$33K\Omega$
C	$10\mu F$

TABLE II
POWER TRAIN COMPONENTS AND PARAMETERS

Component/Parameter	Value
VRM controller	FAN5019
# phases	3
f_{sw}	$257kHz$
V_{in}	$12V$
V_{out}	$1.2V$
L (per phase)	$680nH$
C	$8 \times 820\mu F$
top switch	FDD6296
bottom switch	2×FDD8896
t_{rr}	$27ns$
Q_{rr}	$12nC$

the current measurement at light load is still accurate.

The architecture of the estimation circuit allows for an efficient mixed-signal implementation, in which the integration can be performed digitally, with the ability to stop the integration without drift, while the signal conditioning is performed in the analog domain.

V. CONCLUSIONS

This paper describes a method that allows for an efficient, accurate, and high-bandwidth measurement of the output current in a buck converter. This enables a VRM application to follow the load-line with precision, and to use output current feedforward for a fast transient response.

The method uses the PCB trace resistance at the output of the converter as a sensing element. A slow adaptive loop estimates the gain of the sensing amplifier based on the DC relationship between the output current and the input current, which is measured with a precision sense resistor. The effect of transients and switching non idealities are quantified and included in the method derivation.

A breadboard was constructed and experiments show a precision better than 2% for currents above 20% of the rated maximum. The adaptation loop should never operate at low currents to avoid drifts in the estimate because of the the low signal level compared to the voltage offset of the amplifiers. The estimated current however is accurate for the whole operating range.

Although the method presented makes emphasis on tuning the resistance of the PCB trace, it could be equally used to tune any other sense resistance located in series with the output current or the inductor current, including inductor sensing.

APPENDIX
PCB TRACE FREQUENCY RESPONSE

Consider a stripline consisting of a pair of rectangular copper plates of length L and width W, separated by a dielectric material of thickness $h \ll L, W$ and relative permeability $\mu_r \approx 1$. When a current I flows lengthwise through one of them and returns in the opposite direction through the other, a magnetic field $H = \frac{I}{W}$ is formed in the dielectric. The magnetic flux is then

$$\Phi = \mu_0 H L h = \frac{\mu_0 L h}{W} \times I,$$

so we conclude that the inductance is

$$\mathcal{L} = \frac{\mu_0 L h}{W}.$$

The capacitance, on the other hand, can be computed using the well-known equation for a parallel plate capacitor

$$\mathcal{C} = \frac{\varepsilon_r \varepsilon_0 L W}{h}.$$

If we estimate the cutoff frequency as $f_c = \frac{1}{2\pi\sqrt{\mathcal{L}\mathcal{C}}}$ then we obtain the result

$$f_c = \frac{1}{2\pi\sqrt{\varepsilon_r \varepsilon_0 \mu_0} L}.$$

Notice that the dependence on the width of the plate and the thickness of the dielectric cancel out, and the final result depends only on the length and the dielectric constant.

ACKNOWLEDGEMENTS

The authors want to thank Tien Han and Tim Ng for their help in building the hardware, Steve Cartier for his assistance during the experiments, and Francesco Carobolante for providing support for the project.

This work was supported by the UC Micro program and Fairchild Semiconductor.

REFERENCES

[1] (2005, Apr.) Voltage Regulator-Down (VRD) 10.1 Design Guide. Intel Corp. [Online]. Available: http://developer.intel.com/design/Pentium4/guides/302356.htm

[2] R. Redl, B. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter," in *Proc. IEEE Applied Power Electronics Conference*, vol. 1, 1998, pp. 170–176.

[3] H. Forghani-zadeh and G. Rincón-Mora, "Current-sensing techniques for DC-DC converters," in *Proc. IEEE International Midwest Symposium on Circuits & Systems*, 2002.

[4] R. Lenk. (1999) Application Bulletin AB-20 Optimum Current Sensing Techniques in CPU Converters. Fairchild Semiconductor. [Online]. Available: http://www.fairchildsemi.com/an/AB/AB-20.pdf

[5] Y. Zhang, R. Zane, A. Prodić, R. Erickson, and D. Maksimović, "Online calibration of MOSFET on-state resistance for precise current sensing," *IEEE Power Electronics Letters*, vol. 2, no. 3, Sept. 2004.

[6] J. Luo, N. Pongratananukul, J. Abu-Qahouq, and I. Batarseh, "Time-varying current observer with parameter estimation for multiphase low-voltage high-current voltage regulator modules," in *Proc. IEEE Applied Power Electronics Conference*, 2003.

[7] A. Peterchev and S. Sanders, "Load-line regulation with estimated load current feedforward: Application to Voltage Regulation Modules," in *Proc. IEEE Power Electronics Specialists Conference*, 2004.

[8] R. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. Kluwer Academic Publishers, 2000.