Synchronous Rectification with Adaptive Timing Control

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Abstract— **This paper describes a MOSFET synchronous rectifier suitable for use in high-frequency DC-DC converters. The MOSFET control circuitry is designed to replicate the basic functionality of a rectifier diode, turning on when the voltage across the device falls to zero, and turning off when the current through the device tries to reverse. This synchronous rectification device can be incorporated into a wide range of converter topologies, without the restrictions imposed on other synchronous rectification schemes. In order to minimize the losses resulting from gate drive timing errors at high switching frequencies ($\sim 1MHz$), adaptive timing control loops are used to null the inherent delays of the control and driver circuitry. The power FETs and control circuitry are integrated in a $1.2\mu m$ CMOS process.**

I. Introduction

MOSFET synchronous rectifiers are being employed to replace less efficient diode rectifiers, particularly in low-output-voltage DC-DC converters. There have been several approaches for synthesizing the required gating waveforms in an isolated topology, including:

- Transmitting gate timing information across the isolation boundary, utilizing either optical or magnetic coupling [1].
- Deriving the gating waveforms from auxiliary windings on the main power transformer [2, 3].
- Driving a cross-coupled pair of MOSFETs directly from the voltage appearing on the main transformer secondary (Fig. 1), with the devices arranged either in a single-ended configuration (with a free-wheeling device), or as a full-wave, center-tapped bridge [4, 5, 6, 7, 8].
- Monitoring the MOSFET's drain current and/or drain-source voltage to determine the proper gating waveforms [9, 10, 11, 12].

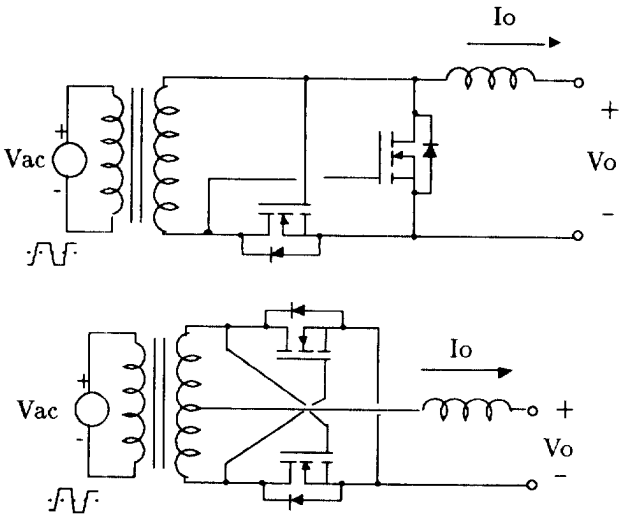

Fig. 1. Single-ended and full-wave cross-coupled gate-drain connection

We briefly summarize some of the disadvantages or restrictions regarding the gating options itemized above. Coupling the timing information across the isolation boundary requires additional components, adding to the cost and complexity of the converter [1, 3]. When auxiliary windings are used, or the FETs are driven directly from the transformer secondary voltage, restrictions are imposed on the converter topology, modulation scheme, and/or input voltage range. Careful design is needed to ensure that the voltage waveform is appropriate for driving the gates; in particular, there should be no intervals when the driving voltage is zero or below the gate threshold, as might occur in some converters using PWM control. The body diodes of the MOSFETs will conduct during such intervals, resulting in increased conduction losses. Other nonideal waveforms include those whose voltages levels are too high (dependent on the input voltage range)

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or whose transitions are slow. High drive voltages impose greater voltage stress, perhaps dictating rectifier technology, and incurring increased gate drive losses. Nevertheless, these schemes are attractive due to their inherent simplicity, and excellent results have been reported using such techniques [6, 8].

MOSFET synchronous rectifiers which rely on sensing the drain current to determine both the turn-on and turn-off timing are sensitive to false triggering during the turn-off transition when circuit parasitics may cause a damped oscillation of the drain current around zero [11, 12]. Techniques to combat the possibility of false turn-on include blanking after the transition or the incorporation of hysteresis in the current comparator. The latter option has the undesirable result of decreasing the dynamic load current range of efficient rectifier operation; if the load current does not exceed the turn-on current level threshold, the rectifier will default to operation using the body diodes.

In our work, we attempt to replicate the functionality of an ideal diode by turning on the MOSFET when its drain-source voltage collapses to zero, and turning off the MOSFET when its drain current decays to zero. This operation can be depicted by a simple state diagram as shown in Fig. 2. We monitor the drain current by looking at the voltage drop across the on-state resistance of the FET, eliminating the need for other methods such as current-sensing transformers or current-sensing MOSFETs [12].

While we strive for universal applicability in our implementation of the synchronous rectifier, there exist converter topologies in which any synchronous rectifier is at a disadvantage compared to a Schottky rectifier. These are converters in which the rms-to-average ratio of the rectifier current is inherently high, as in the output diode of a basic flyback converter.

II. Principle of Adaptive Timing Control

As converter switching frequencies are increased in an effort to improve converter power density, gate timing errors start to have a significant impact on overall synchronous rectifier efficiency. For example, consider a MOSFET rectification device being driven with a 50 percent duty cycle at 1 MHz, with its gate-drive turn-on edge arriving 50 nsec late. The body diode will conduct for 10 percent of the total conduction interval, typically increasing conduction losses by 40 percent. This increase in loss might obviate the use of a synchronous rectifier in place of a standard Schottky rectifier. Early turn-off might be even more problematic than late turn-on due to reverse recovery losses in the body-drain diode. In light of these considerations, we have designed an adaptive timing control system which effectively nulls out delays in the control and gate drive circuitry to maintain high efficiency at switching frequencies in the megahertz range [14].

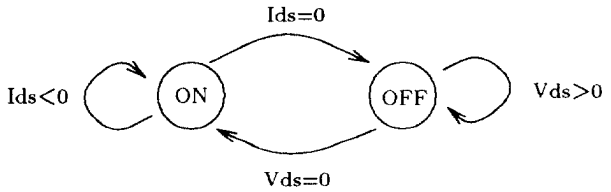

Fig. 2. State transition diagram for control of the synchronous rectifier

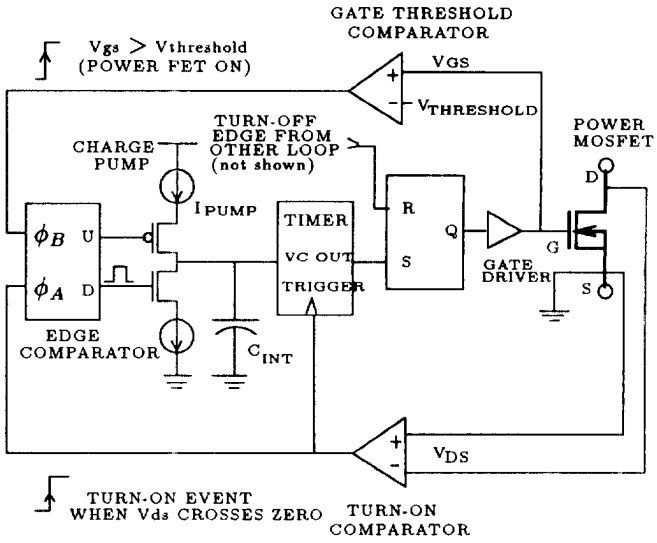

Fig. 3. Turn-on loop circuitry

A. Overview of adaptive turn-on loop

In this section, we describe the basic operating principle of the adaptive timing control. Each rectifier FET has two independent feedback loops; one for determining the turn-on edge timing, and one for the turn-off edge. To simplify the exposition, we can concentrate on the block diagram of the loop for the turn-on control as shown in Fig. 3.

We would like to turn on the MOSFET at the instant that its drain-source voltage is forced to zero by the external power circuit. If we attempt to drive the MOSFET on as soon as this event is detected, we suffer delays through both the comparator and gate drive circuitry. In the adaptive scheme presented here, the detected event will initiate the gate turn-on for the *following* cycle of operation. An error signal is developed during each cycle and used in an

adaptation loop to asymptotically eliminate timing errors in periodic steady-state operation.

The 'turn-on' comparator shown if Fig. 3 is used to detect the occurrence of the turn-on event, i.e. when the drain-source voltage crosses zero. A second comparator, the 'gate threshold' comparator, is used to indicate when the channel of the power MOSFET is enhanced by comparing the gate-source voltage to the nominal gate threshold voltage. The outputs of the turn-on comparator and threshold comparator are fed into an edge comparator, similar to the digital phase detector found in some phase-locked loops. If a positive edge at ϕA leads a positive edge at ϕB, the UP output is driven active for the time lag between them. Conversely, when ϕB leads ϕA, the DOWN output is asserted. Activation of these outputs causes the charge pump to either increase or decrease the voltage stored on the integrating capacitor. In the default state, both FETS of the charge pump are off and the integrating capacitor holds its stored charge. Each loop also contains a monostable (one-shot) timer whose timing interval is determined by the voltage stored on the integrating capacitor.

B. Periodic steady-state operation

Typical waveforms depicting steady-state circuit operation are shown in Fig. 4. When a turn-on event occurs (V_{ds} crosses zero), the turn-on comparator detects the event. After time interval τ_{VDS}, corresponding to the turn-on comparator delay, its output transitions high, triggering the one-shot timer. At the end of the programmed timing interval τ_{TIMER}, the timer output sets the latch. The gate drive buffer circuitry will then start charging up the gate input capacitance of the power FET. Gate voltage will cross the gate threshold voltage after interval τ_{DRIVER}, dependent on the delay and rise-time of the gate drive buffer circuitry. The gate-threshold comparator monitors this event and produces a positive-going edge after interval τ_{VGS}, corresponding to the delay through its circuitry.

For ideal steady-state operation, we require that the power FET is driven on at the instant that its drain-source voltage is crossing zero. We can achieve this by adjusting the timer interval τ_{TIMER} such that

$$\tau_{SW} = \tau_{VDS} + \tau_{TIMER} + \tau_{DRIVER}$$

where τ_{SW} is the power circuit switching period. Note that the delays through the comparators and drive circuitry can be compensated through suitable adustment of τ_{TIMER}.

C. Adaptative mode with error signal

If the one-shot timer interval is incorrect, the power FET will be gated on either early or late. In either case, an error signal is developed to adjust τ_{TIMER} in the right

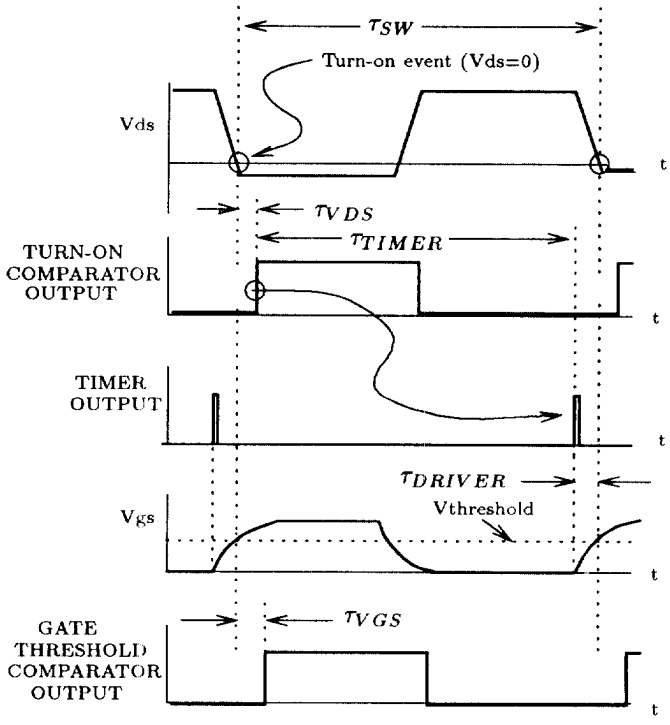

Fig. 4. Ideal waveforms of the adaptive timing loop in steady-state

direction, reducing the timing error for the next cycle of operation.

Waveforms corresponding to early turn-on of the power FET are shown in Fig. 5. If the FET is driven on too early, the gate-threshold comparator output edge will lead the turn-on comparator output edge. These edges are fed into the edge comparator, which activates its DOWN output for the duration of the time lag between them. The charge pump will decrease the voltage stored on the integrating capacitor, with the result that the one-shot will have a longer timing interval the next time it is triggered.

Waveforms corresponding to late turn-on of the power FET are shown in Fig. 6. This case needs to be handled in a different manner than the previous case. If the turn-on comparator has indicated that the drain-source voltage has reached zero, but the timer has has not completed its present timing interval, the circuit does not wait for that timing operation to complete before driving the power FET. Instead, the circuit aborts the present timing cycle, sets the output latch, and retriggers the timer to begin a new cycle. In this mode, the gate drive is guaranteed to arrive late by no more than $\tau_{VDS} + \tau_{DRIVER}$, corresponding to the delays through the comparator and driver circuitry. During the time lag between the respective output edges of the turn-on comparator and the gate-threshold comparator, the edge detector activates its UP

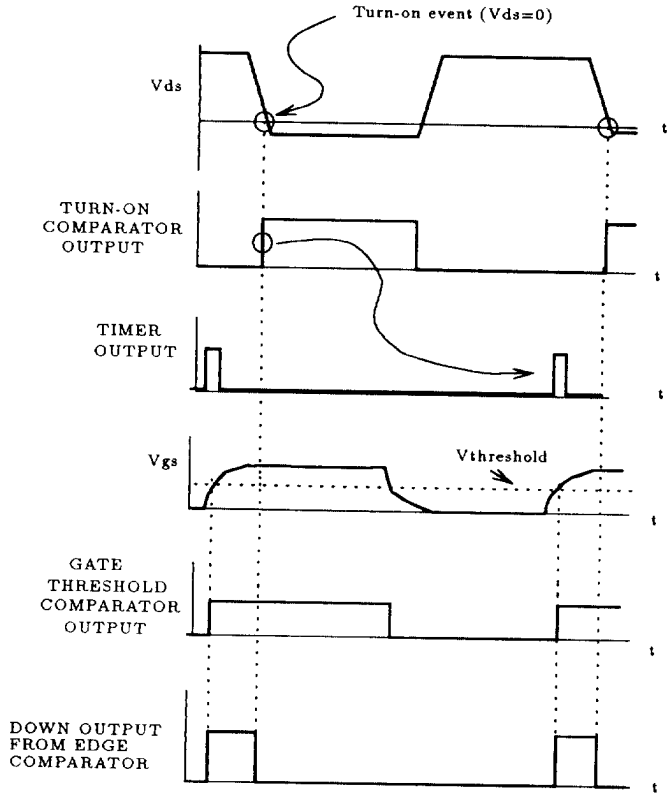

Fig. 5. Waveforms of operation with early gate drive arrival

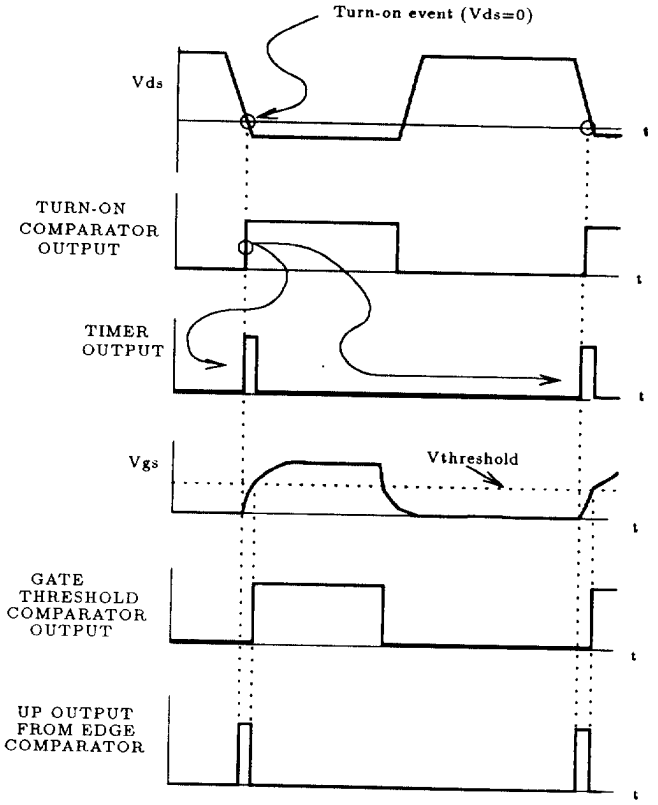

Fig. 6. Waveforms of operation with late gate drive arrival

output. The resulting increase in voltage on the integrating capacitor will decrease the timer interval for the next cycle of operation.

D. Turn-off loop

Another independent adaptation loop effects the turn-off timing of the power FET by resetting the output latch at the appropriate time. This loop has an edge detector, charge pump, integrating capacitor and timer, analogous to those of the turn-on loop. The turn-off comparator, however, needs to detect the zero-crossing of load current through the power FET. It does this by monitoring the small voltage drop developed across the power FET's on-state resistance. Under light load conditions, this signal may be only a few tens of millivolts. See Section IV. C for discussion of the turn-off comparator circuit.

III. Loop Stability and Transient Response

Stability analysis of the adaptation loop may be simplified by assuming linear transfer characteristics for the blocks comprising the loop. Dynamics of the loop may then be described by a linear constant-coefficient difference equation. The system is first-order due to the presence of a single integrator in the loop.

The voltage on the integrating capacitor, $v[k]$, defines the state of the system at time step k. Variable $\tau_{SW}[k]$ defines the power circuit switching period at time step k. The voltage-to-time-interval transfer characteristic of the voltage-controlled one-shot timer may be described by the linear relationship

$$\tau_{TIMER}[k] = \tau_0 - A_1 v[k]$$

with τ_0 a constant and A_1.the effective gain selected by the designer.

Near equilibrium, the loop is governed by the difference equation

$$v[k+1] = v[k] - A_2\{A_1 v[k] - \tau_0 - \tau_{VDS} - \tau_{DRIVER} + \tau_{SW}[k]\}$$

where A_2 is the effective gain of the charge pump. This gain corresponds to the voltage slewing rate of the integrating capacitor, determined by design parameters I_{PUMP}/C_{INT} (Fig. 3).

For stable operation, we require that

$$|\, 1 - A_1 A_2 \,| < 1.$$

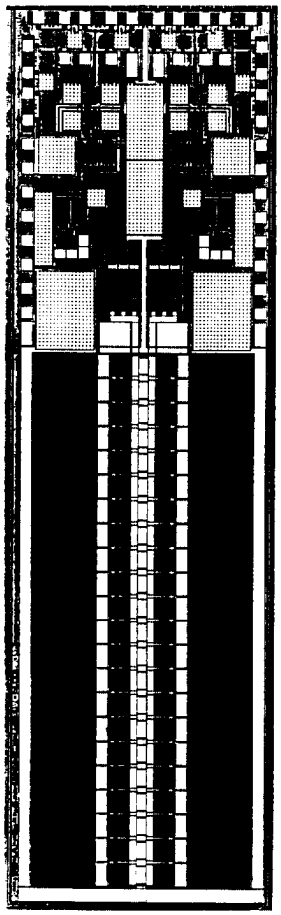

Fig. 7. Chip photograph. The two power FETs are shown in the lower portion of the figure. Die size=9.4mm x 2.8mm

With $A_1, A_2 > 0$, the stability constraint becomes

$$A_1 A_2 < 2.$$

Off-line converters might display switching modulation at a multiple of the line frequency, as the primary side controller attempts to regulate the converter output voltage. Bandwidth of the adaptive loop should be set wide enough to track these perturbations of the switching period.

The foregoing analysis rests on the assumption that the power switching waveforms of interest (drain-source voltage and current in the power FET) are unaffected by gate drive timing errors. While this may be a valid assumption under the influence of small timing errors, interactions between the power circuit and gating circuit will certainly occur under large timing errors.

IV. Circuit implementation

The integrated synchronous rectifier consists of two power MOSFET devices, each with its own independent control and drive circuitry. The single package is suitable for either a full-wave center-tapped bridge rectifier, or a single-ended half-wave rectifier, using one of the FETs as the free-wheeling device. The control, driver circuitry, and power MOSFETs are fabricated in a $1.2\mu m$ lateral CMOS process in an effort to obtain low power dissipation in the controller (Fig. 7). Advantages of this approach include:

- The relatively low gate threshold of these devices allows use of a gate drive level of 3.3 volts or less, significantly reducing gate drive losses.
- Tighter control over source inductance is achieved than by using a commercial packaged FET with separate control/driver circuitry.
- Critical sensing of drain-source voltage can be achieved without the contribution of the di/dt drop, due to load and gate drive, across the source inductance. Additionally, driving the gate through a kelvin source return results in faster transition times for the gate terminal.

The first generation of fabricated devices have been plagued by a problem which prevents us from biasing up all of the circuitry. Experimental data will be available after subsequent devices are fabricated.

A. Power MOSFET design considerations

The design of low on-resistance lateral power MOSFETs in a process intended for standard CMOS VLSI requires that careful attention be paid to parasitic resistances present both on-chip and in the packaging. A chip-on-board technology was chosen for the prototype application circuit in an effort to minimize bond wire resistance on the source and drain terminals. A major constraint was imposed by the sheet resistance of the chip metalization. The two-metal process that was used has a specified sheet resistance of $35m\Omega/\square$. If the total on-resistance design specification is, say, $20m\Omega$, only one half square of metalization in the drain-source current path will contribute the dominant term to the total on-resistance. Metalization resistance can be minimized by laying out the transistor with an aspect ratio that is long and narrow, keeping the source and drain pads in close proximity.

Fig. 8 shows an overview of the power FET layout, along with the last stage of its gate drive circuitry. The two power FETs have continuous drain and source pads running parallel to the long dimension of the chip. Multiple bond wires are parallelled along the length of the pads, resulting in a low impedance interconnect to the printed circuit board. The drain bond wires are routed over the source bond wires as shown in the lower portion of Fig. 8. The $R_{ds(on)}$·Area product is comparable to the latest generation of low-voltage vertical devices [13]. Key MOSFET specifications are summarized in Table A.

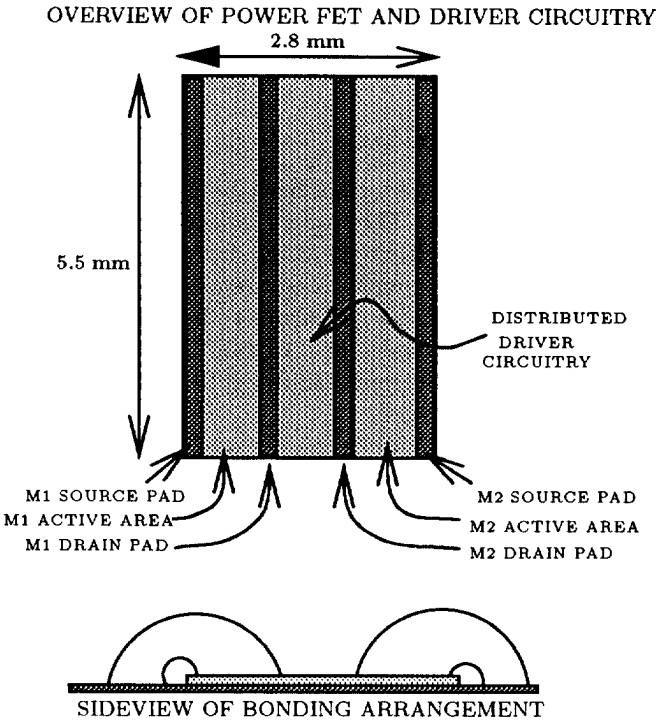

Fig. 8. Overview of power transistor layout and bonding scheme

TABLE A: POWER MOSFET SPECIFICATIONS

Effective channel length	$0.9\mu m$
Gate oxide thickness	$209\AA$
Maximum V_{ds}	$12V$
Gate width	$45cm$
Channel resistance @ $V_{GS} = 3.3V$ [a]	$10.2m\Omega$
Metalization resistance [b]	$6.3m\Omega$
Bonding resistance [b]	$4.3m\Omega$
Total estimated on-state resistance	$20.8m\Omega$
Total gate charge @ V_{GS}=3.3V [a]	$3.1nC$
Total FET area [c]	$5.20mm^2$
$R_{ds(on)} \cdot Area$	$1.1m\Omega \cdot cm^2$

[a]Simulation result, 25°C
[b]Estimated result.
[c]Includes bond pad area.

B. Gate drive circuitry

Each power MOSFET is driven with a six-stage inverter chain, designed with a constant tapering factor of 6.6 [14]. The last stage is distributed along the length of the power transistor, yielding a low impedance drive for the gate input capacitance (Fig. 8). With this scheme, simulation results indicate that the power MOSFET can be switched on or off within 10nsec.

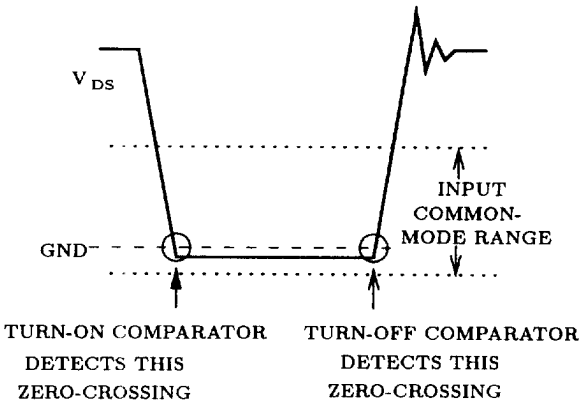

Fig. 9. Typical drain-source voltage waveform

C. Analog comparators

The gate threshold comparator detects when the power FET is gated on or off by comparing the gate-source voltage with a gate threshold voltage reference. Since the threshold voltage parameter exhibits wide variability over process runs and temperature, it is advantageous to generate a gate threshold reference on chip rather than rely on a nominal threshold voltage that is typical for the process [11]. N-channel transistors, connected with a gate-drain short, are biased to serve as threshold sense cells for each gate threshold comparator.

Both the turn-on and turn-off comparators monitor the drain-source voltage across the MOS rectification device for zero crossings. Since the supply for the control circuitry is designed to bootstrap from the output of the converter, these comparators require a common-mode input voltage range extending several hundred millivolts below their negative (ground) supply rail. Conceptually, a single ideal voltage comparator could serve both functions. However, performance limitations of real (non-ideal) comparators necessitate the use of two different comparator designs to meet the demands imposed by the application.

A typical drain-source voltage waveform that the comparators monitor is shown in Fig. 9. The time when each comparator is called upon to detect its zero-crossing is indicated, along with the common-mode input voltage range. Note that the turn-on comparator needs to make its decision soon after sustaining a large input overdrive well above the upper limit of its common-mode range, but the turn-off comparator does not require quick overdrive recovery. On the other hand, the turn-off comparator must be able to resolve a zero-crossing with a signal magnitude of perhaps only $20mV$ (under light load conditions), while the turn-on comparator has no special requirement for low input-offset voltage.

A comparator with active-offset cancellation was de-

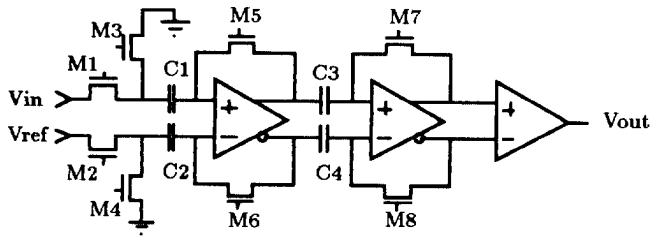

Fig. 10. Active-offset cancellation topology for turn-off comparator

signed to detect the zero-crossing for the turn-off transition [15, 16]. An overview of the topology is presented in Fig. 10. When the comparator is in reset-mode, MOS switches M3-M8 are all closed, while M1 and M2 remain open, isolating V_{in} and V_{ref} from the input. Offset voltage is stored on the interstage coupling capacitors. Input capacitors C1 and C2 also serve the purpose of level-shifting the input voltage so that the effective common-mode input range extends below ground. Once the power FET has been gated on, compare-mode is entered by releasing M3-M8 and closing M1-M2. Differential voltage stored on the capacitors now subtracts from the input voltage, effectively nulling the offset voltage of the comparator circuitry. Reset-mode is re-entered after the comparator has detected a zero-crossing of the load current. Simulation results indicate a comparator delay time of 10nsec while drawing 500μA from a 3.3V supply.

This active-offset cancellation topology cannot be used for the turn-on comparator. If the input voltage is too far from ground potential at the instant that the compare mode is entered, the offset voltage stored on the coupling capacitors will be corrupted. The compare-mode would have to be entered during a very narrow window of time just prior to the negative-going zero-crossing of the drain-source voltage if the offset information is to remain valid.

A simple comparator composed of cascaded, resistively-loaded differential pairs is used for the turn-on comparator [17]. The common-mode input voltage range captures ground potential by the use of p-channel input devices. Good overdrive recovery is obtained by maintaining a low impedance at the differential pair drain nodes. While low offset-voltage is not critical for the application, it is minimized by the use of common-centroid, large-geometry input devices. Simulation results indicate a comparator delay time of 12nsec while drawing 400μA from a 3.3V supply. A similar comparator is used for the gate threshold comparator.

Note that the delays through the turn-on (or turn-off) comparator and the gate-threshold comparator have to be well matched. Although the absolute value of the delays is nulled by the action of the adaptation loop, the mismatch is not nulled and subsequently contributes an error term in the gate drive timing.

V. System issues

A. Bootstrap operation

Our prototype circuit has been designed to operate from a 3.3 volt supply. This supply voltage for the chip may be bootstrapped from the converter output. During the initial power converter start-up transient, the synchronous rectifier chip will not yet have its bootstrapped supply. The body-drain diodes of the MOS rectification devices will rectify load current, allowing the power converter's output voltage to rise.

When the synchronous rectifier control circuitry does receive its bootstrapped supply, the voltage on the integrating capacitors will initially be zero, resulting in long timing intervals from the voltage-controlled one-shot timers. Gate drive will arrive late, as previously described. During the interval $\tau_{VDS} + \tau_{DRIVER}$ ($\sim 25nsec$) following collapse of the drain-source voltage, the body-drain diode of the power FET will conduct the load current. Gate drive will also be removed late by similar operation of the turn-off loop. As the integrating capacitors of each loop charge up to their steady-state values, timing errors are reduced.

B. Clamping the rectifier turn-off voltage transient

If the MOS rectification device is operated in a full-wave, center-tapped, half-bridge rectifier configuration, its off-state voltage will be at least twice the output voltage. The device might see a peak voltage during its turn-off transient of four times the output voltage in a voltage-fed topology [12]. With an output voltage of 3.3 volts, this peak could exceed the $V_{ds(max)}$ rating of our low-voltage process. Clamping the transient at a safe value [18], and recycling the clamp energy into the chip bias supply provides efficient usage of the clamp energy.

C. Master-slave capability

In order to accomodate converters of various output current ratings, the integrated circuit is designed to be operated in a master/slave mode. The drain-source terminals of the power FETs in the slave chips are wired in parallel with the master's power devices. Control circuitry in the slaves is disabled. The master sends out gating waveforms to the drive buffers on the slave chips.

VI. Conclusions

Design considerations for an integrated synchronous rectifier have been presented. Adaptive timing control

loops can be used to minimize the losses resulting from gate drive timing errors. Fabrication of lateral, low on-resistance power MOSFETs in a standard low-voltage CMOS VLSI process requires that careful attention be paid to parasitic resistances present both on-chip and in packaging. The $R_{ds(on)} \cdot Area$ product that is achievable compares favorably with the latest generation of vertical low-voltage MOSFETs currently available.

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