Current-Controlled Synchronous Rectification

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Abstract— **This paper presents several strategies for implementing a current-controlled synchronous rectifier. One approach utilizes a current-sensing transformer in series with the rectifying MOSFET to derive the required gating signals. The second method uses the mirror current of a current-sensing MOSFET. Experimental results obtained with current-driven rectifiers in a center-tapped, full-wave configuration are presented.**

I. Introduction

MOSFET synchronous rectifiers are being employed to replace less efficient diode rectifiers, particularly in low-output-voltage DC-DC converters. In many applications, synchronous rectifiers are used in a voltage-fed inductor-loaded configuration. Gate drive signals may then be derived from auxiliary windings on the power transformer [1, 2]. Alternatively, a gate-drain cross-coupled connection for a pair of MOSFETs might be used (Fig. 1), eliminating the need for additional secondary transformer windings [3, 4].

When the rectifier is current-fed and capacitor-loaded, the MOSFET gating signals can no longer be easily derived from voltages appearing on the transformer secondary, since these voltages are predominantly controlled by the state of the rectifier itself. Secondary currents must be used to determine the timing of drive signals. True current-controlled synchronous rectifiers have not been widely reported in the literature, but see [5, 6].

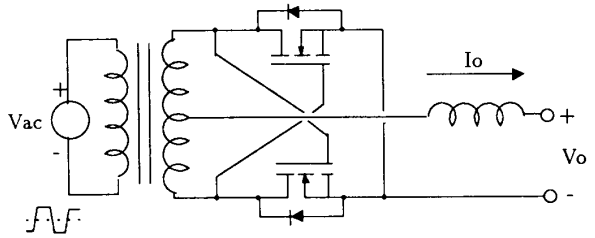

Fig. 1. Cross-coupled gate-drain connection

The current-fed, capacitor-loaded rectifier topology offers several advantages over voltage-fed, inductor-loaded configurations. In a center-tapped, full-wave, current-fed circuit, the rectification devices will exhibit zero-voltage transitions provided the two secondary windings are tightly coupled. Additionally, the off-state voltage across the rectifiers is clamped by the output capacitor, reducing peak device stress. The desire to implement a suitable synchronous rectifier for the current-fed topology has motivated the present research project.

Three possible gate-drive control schemes have been identified for current-controlled synchronous rectifiers:

- The voltage developed across the MOSFET's drain and source terminals as a result of current flow through its on-state resistance can be used to qualify gating signals.
- Current-sensing MOSFETs can provide gating signals via their mirror current.
- A current-sensing transformer can be placed in series with the MOSFET to monitor rectifier current.

In all three schemes, the integral body diode provides a path for initial current conduction before the channel is enhanced. Gate drive is applied when this current reaches a turn-on threshold. The gate drive is maintained until the external circuit causes the current to decay below some specified turn-off threshold.

The first approach listed above suffers from the conflicting requirements of minimizing conduction losses while maximizing the signal-to-noise ratio, particularly at low levels of load current. For this reason, we have not pursued this approach in our work.

The second two approaches offer greater latitude in scaling the signal appropriately for a particular application. We have decided to investigate both of these schemes.

One goal of this research effort is to eventually fabricate a monolithic three-terminal synchronous rectification device which will function in some applications as a replacement for existing rectifier diodes. Two of the terminals would correspond to the anode and cathode of the rectifier while the third terminal would be provided with the

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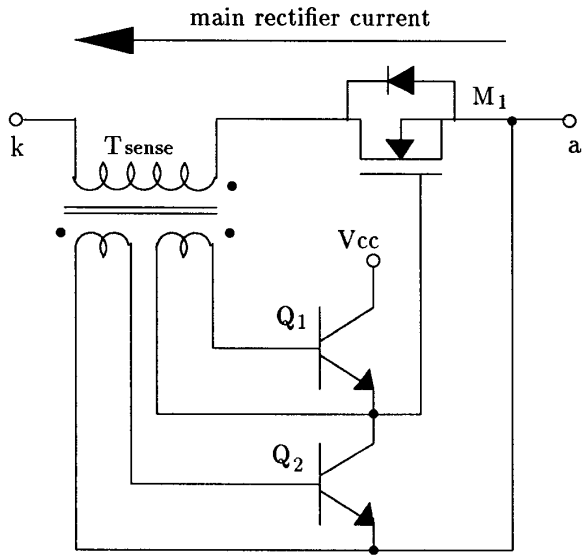

Fig. 2. Rectifier gate drive circuit

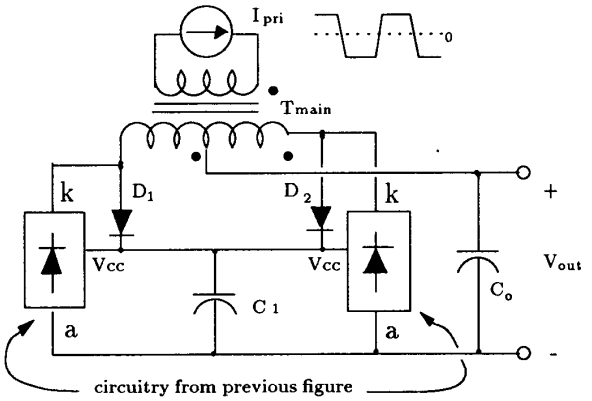

Fig. 3. Overall rectifier organization

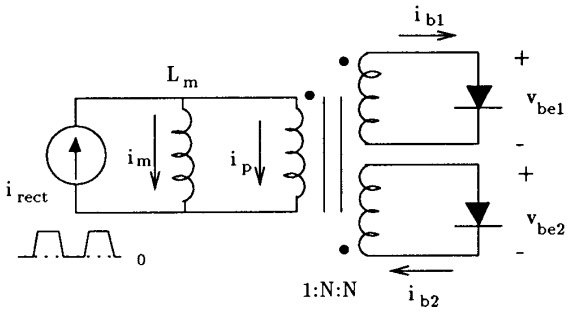

Fig. 4. Equivalent sense transformer circuit

supply voltage for the control circuitry and internal gate drive. Such a bootstrap supply could be easily derived from a convenient circuit node; alternatively the supply could be developed from the off-state voltage across the rectifier itself subject to constraints on maximum duty-cycle and converter switching frequency [7].

The scope of the work presented in this paper is to demonstrate the viablity of the latter two current-controlled synchronous rectification schemes mentioned above. We have implemented these two approachs with discrete components to gain insight into relevant design issues, in preparation for the proposed monolithic implementation.

II. Principles of Operation

A. Current-Sensing Transformer Approach

The arrangement of the MOSFET gate drive circuit is shown in Fig. 2. Totem-pole drivers $Q_1 - Q_2$ are themselves driven from the secondaries of the current-sensing transformer T_{sense}, in response to the main rectifier current flowing through M_1.

We have selected a current-fed isolated converter topology, as described in [8], to provide a test-bed for our synchronous rectifier prototypes. Relevant features of this converter, with respect to output rectifier design, include:

- The primary of the main transformer is driven by a fixed-frequency, 50% duty-cycle square-wave current. This current is represented by the equivalent source I_{pri} in Fig. 3.
- The rectifier is loaded by capacitor C_O.

The overall organization of the synchronous rectifiers in a center-tapped full-wave configuration is as shown in Fig. 3. Diodes $D_1 - D_2$ and capacitor C_1 develop bootstrap voltage V_{cc} from the secondary of main transformer T_{main} for the collector supply of the totem-pole bipolar junction transistors (BJT).

An equivalent circuit seen by each of the sense transformers is shown in Fig. 4. Leakage inductance is neglected here. The secondary windings are loaded by the base-emitter junctions of the totem-pole BJTs. Current source i_{rect} represents the half-wave rectified current seen by the primary winding.

Idealized waveforms for the circuit are displayed in Fig. 5. To insure against premature gate-drive transi-

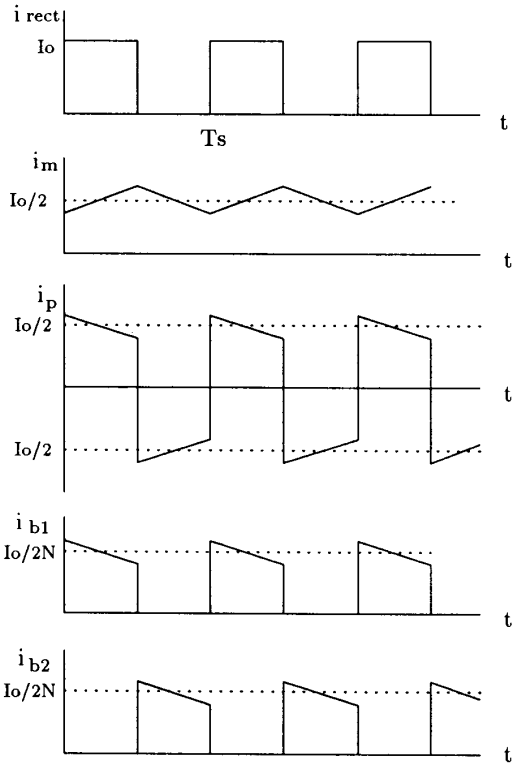

Fig. 5. Idealized waveforms

tions, the magnetizing current i_m must be continuous. This constrains the magnetizing inductance L_m, referred to the primary, to satisfy:

$$L_m > \frac{V_{be} T_s}{2N \cdot I_{min}}$$

where T_s is the switching period and I_{min} is the minimum load current.

The deadtime between drive pulses is inherent in the circuit design. Ideally, each BJT totem-pole inverter switches when rectifier current equals its associated sense transformer magnetizing current, referred to the primary. Assuming a large magnetizing inductance, this magnetizing current is approximately the average of the half-wave rectified current, as seen in Fig. 5. The deadtime then is half the commutation interval (Fig. 6).

Storage time in the BJTs causes turn-off delays which can be detrimental to proper rectifier operation. Before current commutates from one sense winding to the other, reverse base current is actively drawn from the outgoing BJT. Although this decreases the turn-off delay, care must still be exercised in selecting transistors with adequate

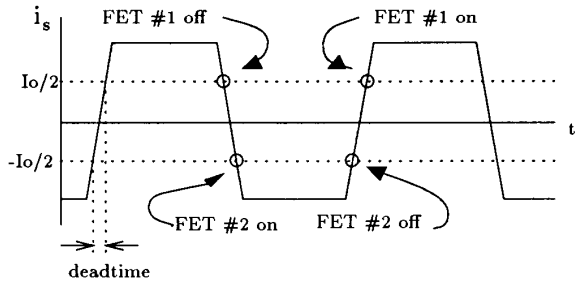

Fig. 6. Unrectified secondary current showing deadtime intervals

saturated switching characteristics. If necessary, drivers $Q_1 - Q_2$ may be clamped to keep them out of saturation.

The synchronous rectifier circuit outlined in this section has several shortcomings that become apparent as converter switching frequencies and power densities increase. The voltage drop across the base-emitter junctions of the BJTs is reflected back to the primary by the sense transformer turns ratio. This voltage should be kept small since it directly adds to the voltage drop across the MOSFET in the on-state. Two secondary windings of, say, 100 turns each would render the current-sensing transformers awkward to fabricate, particularly with the planar geometries now being used in some high frequency (>500kHz) converters. The size and/or cost of the sense transformers, whether wound or planar, might detract from the overall utility of this approach. However, the possiblity of utilizing microfabricated transformers could prove attractive in the future [9].

Inductance in series with the MOSFETs, introduced by the leakage of the sensing transformers, would be detrimental to current commutation in the rectifier. Additionally, it should be noted that operation of the rectifier with sinusoidal load currents, as would occur in some resonant topologies, might result in excessive deadtime between rectifier conduction intervals.

B. Current-Sensing MOSFET Approach

To circumvent these difficulties, a synchronous rectifier scheme based on current-sensing MOSFETs has been designed (Fig. 7).

In this circuit, $Q_1 - Q_2$ form a transresistance amplifier for the FET mirror current I_{sense}. Unlike standard virtual-ground sensing techniques [10, 11, 12], this arrangement requires only a single polarity supply, while providing a unipolar voltage output (at the collector of Q_2) for a bipolar current input.

The signal is fed through level-shift/buffer $Q_3 - Q_4$ to Schmitt trigger $Q_5 - Q_6$. Ideally, the turn-off threshold

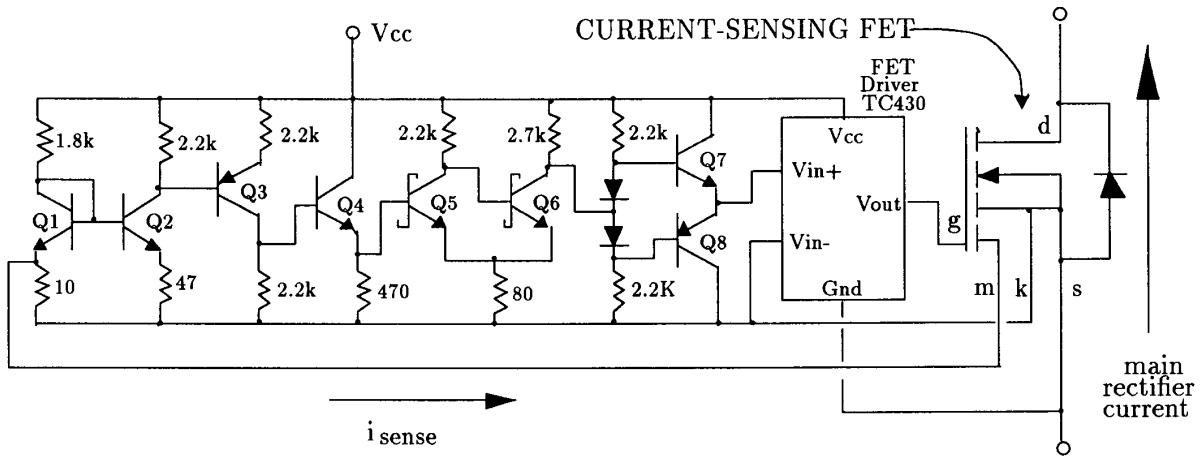

Fig. 7. Gate drive circuitry for use with the current-sensing MOSFET

of the circuit would be set to achieve zero-current switching in the synchronous rectifier. This could be realized by matching the propagation delay through the driver circuitry to the time required for the rectifier current to decay to zero.

The current-sensing MOSFET is used in the third quadrant (positive current flowing from source to drain) during its conduction interval. When the channel is enhanced, the body diode is not active and the current-sensing ratio is identical to that in first-quadrant operation. During body diode conduction, non-linearities are introduced in the sense ratio if appreciable resistive loading is present in the mirror circuit [10, 12]. This loading is kept acceptably low ($<10\Omega$) in the circuit of Fig. 7. Accuracy requirements for the sense signal in this particular application are substantially more relaxed than the accuracy requirements in some other applications using the current-sense signal, such as current-limiting circuits.

III. Experimental Results

A. Current-Sensing Transformer Prototype

An experimental prototype of the synchronous rectifier was constructed for the previously cited DC-DC converter [8]. The current-sense transformers were wound on gapped E-E ferrite cores, using a single turn primary and 100 turn secondary windings. IRFP064 MOSFETs, with a nominal $9m\Omega$ on-state resistance, were used for the synchronous rectifiers. This initial prototype was operated at a 25kHz switching frequency. Circuit waveforms for the rectifier are shown in Fig. 8.

The upper trace shows the FET's drain-source voltage.

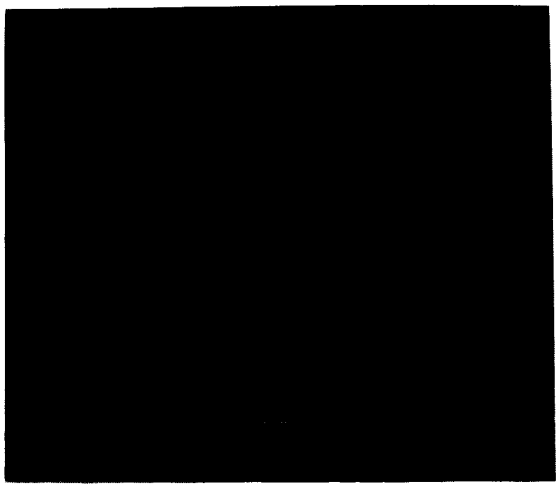

Fig. 8. Rectifier waveforms. TOP: V_{DS} (5V/div); MIDDLE: V_{GS} (5V/div);A BOTTOM: I_{source} (5A/div); 5μsec/div.

Evidence of body diode conduction can be seen just after turn-on. About 1.5 μsec later, gate drive voltage is applied (middle trace), reducing the voltage drop across the FET. The lower trace shows current flow through the device.

Fig. 9 compares the gate drive waveforms of the two MOSFETs. Cross-conduction in the rectifier is avoided by the non-overlapping drive waveforms, as discussed in section II(A).

Measured converter efficiency vs. load current at a 3.3V output voltage is displayed in Fig. 10. Further improve-

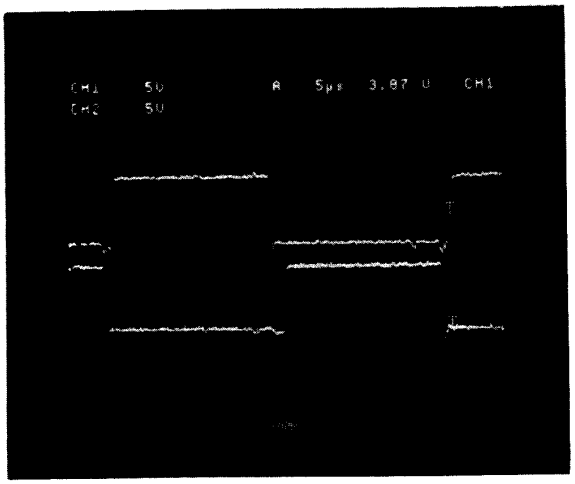

Fig. 9. Gate drive waveforms. TOP: V_{GS1} (5V/div); BOTTOM: V_{GS2} (5V/div); 5μsec/div.

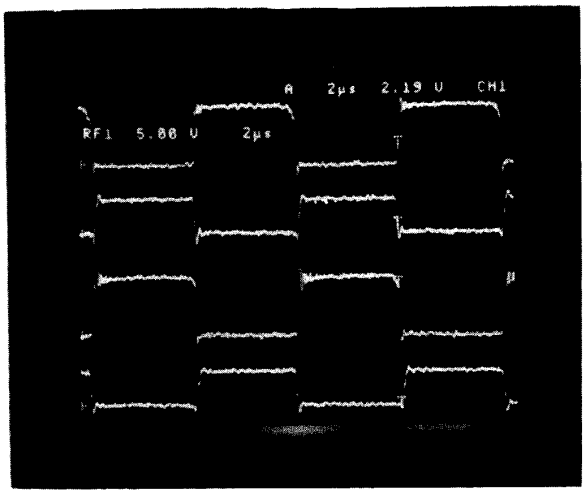

Fig. 11. Rectifier waveforms at 100kHz. TOP: V_{DS1} (5V/div); SECOND: V_{GS1} (10V/div); THIRD: V_{DS2} (5V/div); BOTTOM: V_{GS2} (10V/div); 2μsec/div.

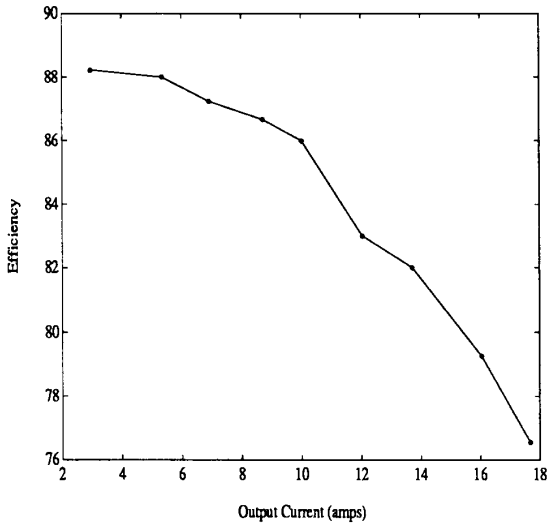

Fig. 10. Measured efficiency vs. load current at $V_{out} = 3.3V$

ments in efficiency are limited primarily by conduction losses in the syncronous rectifier FETs. Some reduction of $R_{DS(on)}$ could be achieved by driving the FETs used in the prototype with a higher gate drive voltage than the 8 volts developed in the bootstrap voltage V_{cc}. The use of external anti-parallel Schottky diodes across the FETs could reduce losses during the brief interval of body diode conduction at device turn-on.

B. Current-Sensing MOSFET Prototype

The circuit of Fig. 7 was constructed on a breadboard with discrete transistors and a commercial MOSFET driver IC. Current-sensing FETs (IRCP054), with a nominal $R_{DS(on)}$ of $14m\Omega$ were used for the rectification devices. Since propagation delay through the circuit can impose limitations on high frequency operation, efforts were made to minimize this delay. Devices $Q_5 - Q_6$ are high-speed switching transistors which were clamped with external Schottky diodes. The other transistors were selected for their high f_T specifications (>1GHz). Propagation delay from the input at the emitter of Q_1 to the output node of $Q_7 - Q_8$ was measured at approximately 75 nanoseconds. The FET driver chip was selected for its drive current capability and fast response.

The circuit was initially operated at a 100kHz switching frequency. Fig. 11 shows drain-source voltages across the MOSFETs along with their respective gate drive voltage waveforms. Body diode conduction is evident for about 100 nsec after turn-on. This interval is consistent with the measured propagation delays through the discrete circuitry and integrated FET driver.

As a measure to reduce noise transients in the sensitive control circuitry during device switching, the output of the FET driver was referenced to the main source terminal of the power MOSFET, while the control circuitry was referenced to the kelvin terminal. A common-mode choke was added to the gate drive lead wires to force gate current transients to return directly to the FET driver. The slight overshoot in the gating waveforms (Fig. 11) is a result of stray inductance introduced into the gate drive lead wires.

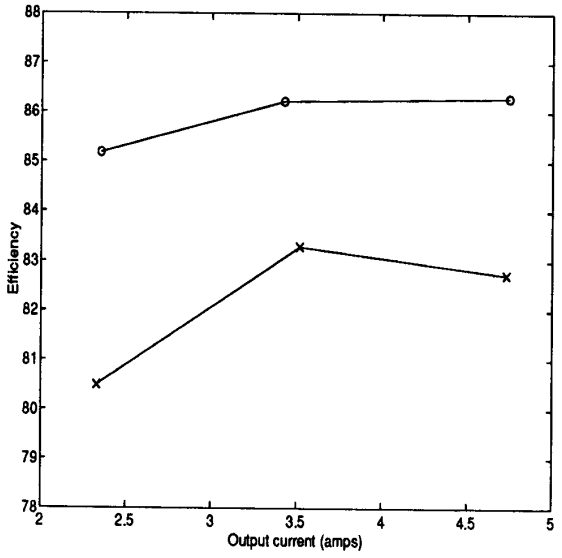

Fig. 12. Measured efficiency vs. load current at $V_{out} = 3.3V$ and 100kHz switching frequency. o=synchronous rectifiers. x=Schottky diodes.

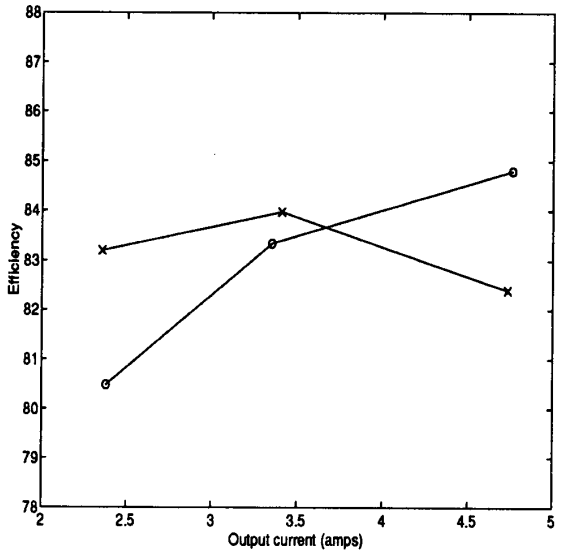

Fig. 13. Measured efficiency vs. load current at $V_{out} = 3.3V$ and 300kHz switching frequency. o=synchronous rectifiers. x=Schottky diodes.

Efficiency measurements for the converter were recorded both with Schottky rectifier diodes and the synchronous rectifier to provide a basis for comparison. The Schottky diodes (unpackaged International Rectifier dice SC200S030S) had a forward voltage drop of approximately 0.32 volts at 5.0 amps and 25°C. Comparative testing was done at converter switching frequencies of 100kHz, 300kHz, and 500kHz. Power consumed by the gate drive circuitry of the primary-side FETs is not included in this efficiency data. The remaining losses are in the main transformer, saturable reactors, primary-side FETs and interconnecting conductors, as well as in the rectifiers itself. While it would be desirable to present data representing isolated rectifier losses, this proved to be difficult in practice.

Fig. 12 shows the efficiency data at 100kHz. At this frequency and load current range, the synchronous rectifier provides a 3% to 5% boost in efficiency. The conduction and body diode losses in the FETs, estimated at about 450mW with a 5 amp load current, roughly balance the 350mW that is being dissipated in the control and gate drive circuitry.

Efficiency data obtained at the converter switching frequency of 300kHz is presented in Fig. 13. The synchronous rectifier offers a slight improvement over the Schottky diodes in the upper range of load currents. Power dissipation in the control and driver circuitry is starting to dominate the conduction and body diode losses at low output currents.

At a switching frequency of 500kHz (Fig. 14), the synchronous rectifier offers no advantage over the Schottky diodes, particularly at low output currents. Losses in the control and driver circuitry (775 mW) are now a significant fraction of total converter losses.

Fig. 15 shows drain-source voltages across the MOSFETs along with their respective gate drive voltage waveforms at a 500kHz switching frequency. Body diode conduction is still evident for about 100 nsec after turn-on, but this interval is now a substantial fraction of the 1 μsec rectifier conduction interval. Assuming a load current of 5 amps and a body diode voltage drop of 0.8 volts, power loss in the body diode is 400 mW. In comparison, power loss in the device during the remaining 900 nsec of the conduction interval is only 315 mW. Propagation delay through the control and driver circuitry is clearly critical in determining upper bounds on rectifier switching frequency. A monolithic implementation will reduce this propagation delay and improve high frequency performance.

IV. Conclusion

Two strategies for implementing current-controlled synchronous rectifiers have been presented. A current-sensing transformer approach has proven feasible at a switching frequency of 25kHz. When power density and/or cost considerations are predominant, fabrication of suitable sense transformers might become problematic. A second scheme based on current-sensing MOSFETs has been designed. A discrete prototype of this circuit has demonstrated an effi-

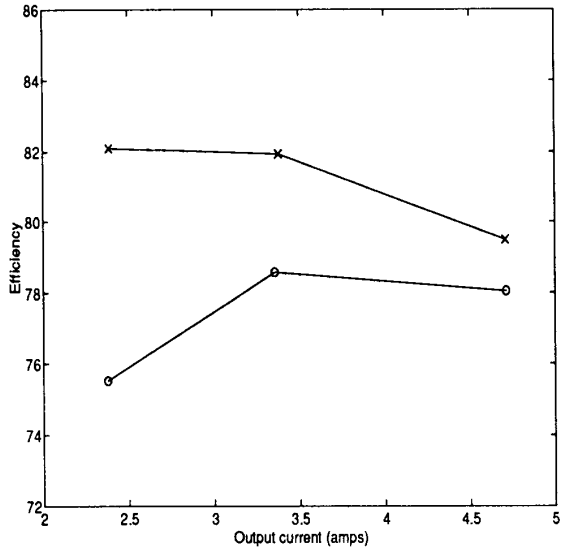

Fig. 14. Measured efficiency vs. load current at $V_{out} = 3.3V$ and 500kHz switching frequency. o=synchronous rectifiers. x=Schottky diodes.

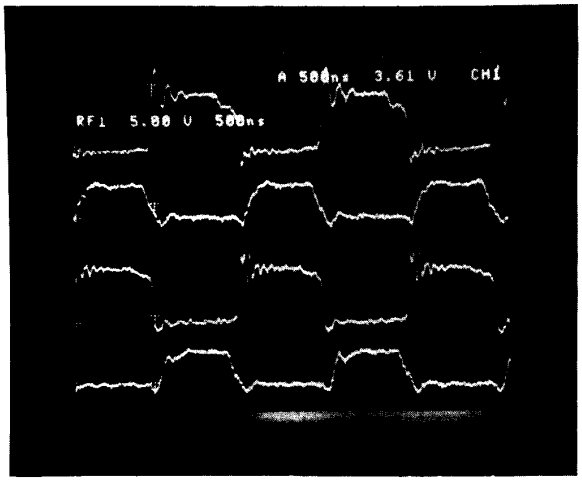

Fig. 15. Rectifier waveforms at 500kHz. TOP: V_{DS1} (5V/div); SECOND: V_{GS1} (10V/div); THIRD: V_{DS2} (5V/div); BOTTOM: V_{GS2} (10V/div); 500nsec/div.

ciency improvement over Schottky rectifiers up to 300kHz. Losses in the gate drive, control circuitry, and body diode start to dominate in the 500kHz operating regime. The current-sensing MOSFET approach is suitable for monolithic fabrication. Improvements in propagation delay and power consumption that a monolithic implementation could achieve over discrete circuitry are expected to extend operation of the rectifier into the 500kHz to 1MHz operating region.

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