Optimum Biasing for Parallel Hybrid Switching-Linear Regulators

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***Abstract*—Hybrid combinations of switching and linear regulators have been proposed for both audio amplifiers and dynamic supply modulators for radio frequency (RF) power amplifiers (PAs). Such topologies may provide benefits in terms of efficiency, dynamic range, and speed of dynamic response compared to pure linear regulators or class-D switching amplifiers. This paper presents a framework for analyzing the bias constraints of switching and linear voltage regulators operated in a parallel-hybrid configuration. Particular emphasis is given to polar and envelope tracking RF power amplifier (RF PA) applications. Ideal expressions are derived for the optimum current contribution of the switching regulator under quasi-static operating conditions. In contrast to previous work, it is shown that the optimum mean current contribution of the switching regulator is not necessarily the dc current to the load. Explicit expressions for theoretical maximum efficiency are derived for envelope waveforms that result from two-tone and sinusoidal amplitude modulation of the RF carrier; IS-95 CDMA and IEEE 802.11a/g wireless LAN envelope waveforms are treated in simulation and experiment. Theoretical predictions are validated with measured results.**

***Index Terms*—Class-D amplifier, dc–dc converter, dynamic supply, linear regulator, power amplifier (PA).**

I. Introduction

EFFICIENT modulation of the power supply can increase the average efficiency of wireless transmitters, improving battery life in portable communication systems, especially when the power amplifier (PA) tends to operate at less than maximum power [1]–[3]. Transmitter architectures that require dynamic regulation of the supply voltage, such as those employing polar and envelope tracking techniques, will become increasingly important as high data-rate standards such as wideband code-division-multiple-access (WCDMA) and IEEE 802.11a/g gain widespread adoption [3]–[6]. Such high-bandwidth modulation formats result in envelope signals with high peak-average power ratio (PAPR), and often require power control to prevent interference in a cellular-type network [2], [7]. By efficiently regulating the supply voltage synchronously with the envelope of the RF carrier, the efficiency of the transmitter may be higher in the power range where the PA is most likely to operate, raising average efficiency and increasing battery life [8].

While dynamic power supply transmitter architectures provide significant power savings compared to traditional architectures, they require accurate, wideband modulation of the power supply to meet strict spectral performance requirements. Small mismatch in the phase or amplitude of the supply voltage relative to the RF path can lead to degradation of the error-vector magnitude (EVM) of the transmitted signal [6]. Also, noise or voltage ripple on the power supply can be upconverted into the RF spectrum, degrading the signal/noise ratio (SNR) and potentially violating the spectral mask [9]. It is therefore of critical importance that the supply modulator accurately and efficiently replicate the desired envelope signal with negligible amounts of phase or voltage deviation.

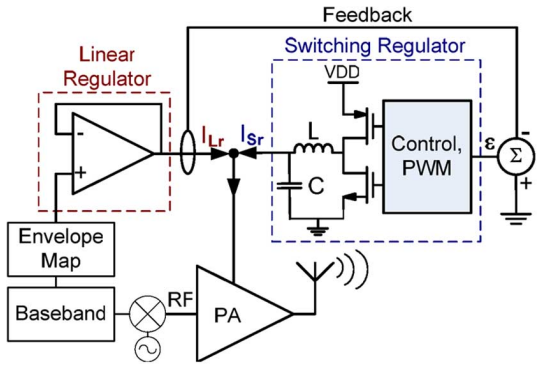

Fig. 1. Traditional parallel linear-switching hybrid regulator topology.

Hybrid combinations of linear and switching regulators are well suited to dynamic supply applications because they combine favorable aspects of both switching and linear regulators. Specifically, high gain-bandwidth linear regulators can provide fast voltage regulation with a high dynamic range [4], [10], [11], while properly designed switching regulators can achieve high efficiency for a large range of conversion ratios and load conditions [12], [13]. Because of the benefits of the combined solution, hybrid regulator topologies have been proposed for both transmitter applications [14]–[16], and high-efficiency audio amplifiers [17], [18]. In audio applications, low signal bandwidth makes the hybrid topologies less attractive compared to pure switching regulator (class-D) topologies, which have been shown to achieve high efficiency and excellent fidelity [19]–[21]. However, in transmitter applications, high envelope bandwidths make class-D solutions less attractive due to losses associated with high switching frequencies [8], [22]–[24]. In this case, hybrid topologies are practical because they can eliminate the tradeoffs among efficiency, bandwidth, and spectral fidelity [14], [16].

Fig. 1 shows a schematic representation of a hybrid regulator consisting of parallel linear and switching stages. For this topology, several control methodologies have been proposed to combine the outputs of the two different regulator blocks. The

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linear regulator is typically used as a follower stage that supplies a buffered version of the reference voltage to the regulator output. Local feedback around the linear stage is used to reduce output impedance and improve accuracy. The bandwidth of the system is determined by the gain-bandwidth product of the linear regulator which can be high in modern semiconductor processes [10], [11]. If the linear regulator is designed with high closed loop bandwidth, it can be used to attenuate switching harmonics from the dc–dc converter stage [17], [18], and can also supply a portion of the dynamic power of the signal [15], [16]. Traditionally, to achieve the desired control, the output current of the linear regulator is sensed and is used as an error signal for the switching regulator. In work reported in the literature, the switching regulator forces the average or dc linear regulator current to zero with linear (proportional-integral) control, [14], or hysteretic control, [15]. The switching regulator can also have a non-zero bandwidth and supply some of the dynamic power. A method to determine the optimum bandwidth of the switching stage through simulation is proposed in [16].

In this work, we study the parallel linear-switcher combination for applications related to dynamic power supplies for RF power amplifiers. We expand on the work in [14]–[18] with particular emphasis on the optimum bias condition. In our approach we assume that the switching regulator operates as a quasi-static current source. This assumption is valid under the practical condition that the envelope frequency is much higher than the bandwidth of the switching regulator. This work does not consider directly the topic of the switching regulator providing part of the *ac* current to the load. Instead we generalize the analysis by treating the switching regulator current as quasi-static. In this case, by changing the time window of the quasi-static analysis, the switching regulator current can be optimized for higher frequency situations. However, we do not consider the concept of band separation between the switching and linear regulator currents as described in [16]. This is difficult because real wireless signals follow a pseudo-random trajectory. Additionally, many time domain signals can have the same power spectrum. This may lead to sub-optimal efficiency if the switching regulator is optimized for bandwidth alone without consideration of the time-domain bias conditions.

In our analysis, we derive expressions for the optimum switching regulator current as a function of the supply voltage, the average output voltage, and dynamic characteristics of the envelope signal. The optimization is based on the conduction angle of the linear regulator output stage. It is shown that there is an optimum efficiency for such a configuration, and that the optimum switching regulator current varies with the power of the signal. We verify some of the conclusions of [14]–[16], but show that a higher efficiency methodology is possible that involves scheduling the current provided by the switching regulator. Importantly, and in contrast to previous work, we show that for maximum efficiency, the optimum quasi-static switching regulator current may be more than the dc current to the load. We verify our predictions with measured data and demonstrate the benefits of optimum quasi-static biasing for representative wireless communication standards including IS-95 code division multiple access (CDMA) and IEEE 802.11a/g.

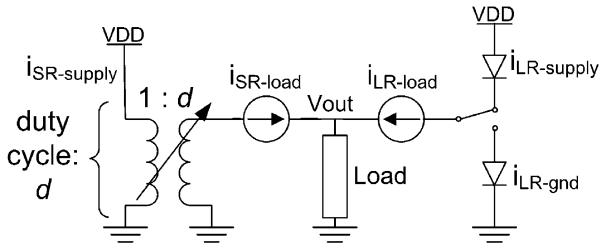

Fig. 2. Proposed hybrid switching regulator model.

II. Optimum Bias Point: Model and Calculation

To reduce voltage ripple, switching regulators must tradeoff transient response and/or efficiency by increasing the size of the filter components or increasing the switching frequency [24], [25]. Linear regulators, on the other hand, may provide spectral purity and high gain-bandwidth product, but have low power efficiency, especially at low conversion ratios. The hybrid topology can decouple efficiency from transient response and voltage ripple, allowing the performance of a linear regulator with less power consumption.

In this treatment, we model a step down (buck) dc–dc converter as a quasistatic current source with average conversion ratio, d, between the load current and the current drawn from the supply. As shown in Fig. 2, it is assumed that the switching regulator operates as an ideal transformer and has zero bandwidth over some finite time window. The average voltage across the inductor must be zero, so duty cycle is constrained to be the ratio of the average output voltage to supply voltage

$$d = \frac{\langle V_{\text{out}} \rangle}{V_{dd}} \tag{1}$$

where $\langle V_{\text{out}} \rangle$ is the average output voltage over some time window $a \leq t \leq b$, and $\langle f(t) \rangle = 1/(b-a) \int_a^b f(t)dt$. For periodic $f(t)$ with period T, a and b may be taken as nT and $(n+1)T$ for integer n to reflect integration over one full period of the envelope signal.

The linear regulator is modeled as an ideal class B topology, with a push-pull rail-to-rail output stage. It can be verified that this is typically the most efficient output stage for signals of interest [26]. With a push-pull output stage, all current sourced to the load comes from the supply, all current drawn from the load sinks to ground. For periodic modulation waveforms, the conduction angle of the linear regulator will be defined as the radial angle in degrees that the regulator draws current from the supply. The conduction angle can change because the current of the two regulator blocks is summed at the output. The switching regulator can source any proportion of the average current. This allows the linear regulator to operate with any conduction angle between 0–360°. The optimum bias point and conduction angle are derived based on average efficiency

$$\langle \eta \rangle = \frac{\langle P_L \rangle}{\langle P_S \rangle} \tag{2}$$

where $\langle P_L \rangle$ is the average power to the load and $\langle P_S \rangle$ is the average power from the supply. Assuming an ideal situation as in Fig. 2, the average power from the supply follows from

$$\langle P_S \rangle = V_{\rm DD} \cdot [\langle i_{\rm LR} \rangle + \langle i_{\rm SR} \rangle \cdot d] \tag{3}$$

where $i_{\rm LR}$ and $i_{\rm SR}$ are the linear and switching regulator currents delivered to the load, d is the duty cycle, and $V_{\rm DD}$ is the supply or battery voltage. To calculate average efficiency it is necessary to derive or measure average currents, $\langle i_{\rm LR} \rangle$ and $\langle i_{\rm SR} \rangle$. For simple envelope waveforms, such as sinusoidal AM and two-tone RF signals, expressions for (2) and (3) can be derived explicitly based on characteristics of the regulated voltage signal and the supply or battery voltage. It should be noted that while the calculation in (3) is proposed for the ideal situation, the concept extends to real switching and linear regulator components that include various forms of loss. Also, for the calculations presented in Section III, the load is assumed to be linear and resistive. Real power amplifier loads may be nonlinear and reactive. This can complicate the calculation of average efficiency, but does not reduce the utility of the optimization procedure. The explicit calculations for the sinusoidal-AM and two-tone cases are presented as an example to highlight the benefits of optimum quasi-static biasing. For cellular and wireless internet standards, such as CDMA, UMTS and the 802.11 standards, hand calculations are difficult due to the nonperiodic nature of the envelope waveform. However, assuming $\langle i_{\rm LR} \rangle$ and $\langle i_{\rm SR} \rangle$ can be measured, the optimum bias point can still be determined, as will be presented in Section V. Therefore, regardless of the complexity of the envelope waveform and losses in the switching and linear regulator components, there is significant value in optimizing the relative current contribution of the regulator stages.

III. Efficiency Optimization: Sinusoidal and Two-Tone Carrier Modulation

Envelope signals that result from explicit modulation of the RF carrier may allow direct solution of optimum biasing expressions. For the case of sinusoidal amplitude modulation of the RF carrier, the envelope voltage and current waveforms may be written as

$$\begin{aligned} v_o(t) &= v_{\rm dc} + v_a \cdot \cos(wt), \text{and} \\ i_o(t) &= i_{\rm dc} + i_a \cdot \cos(wt). \end{aligned} \tag{4}$$

Here, v_o and i_o are the output voltage and current respectively, v_a and i_a are the voltage and current amplitudes, and $v_{\rm dc}$ and $i_{\rm dc}$ are the dc values. In (4), and in the rest of this work, the load is assumed to be linear and resistive although reactive and nonlinear loads can be treated in a similar manner.

Fig. 3 shows normalized versions of the envelope signal for sinusoidal-AM and two-tone modulation of the carrier. In the sinusoidal-AM case the amplitude modulation is such that $v_a = v_{\rm dc}$. The average power delivered to the load is, therefore

$$\begin{aligned} \langle P_L \rangle &= \frac{1}{T} \int_0^T v_o(t) \cdot i_o(t) dt \\ &= v_{\rm dc} \cdot i_{\rm dc} + \frac{v_a \cdot i_a}{2}. \end{aligned} \tag{5}$$

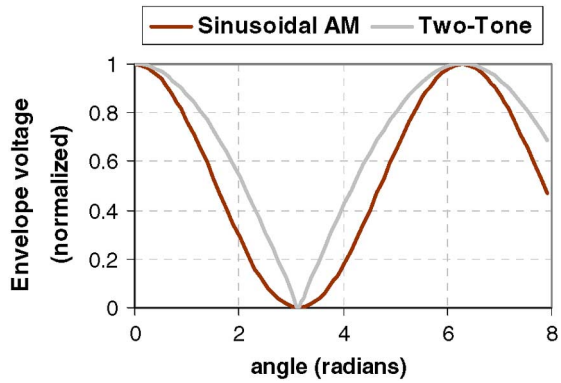

Fig. 3. Envelope waveforms: sinusoidal AM and 2-tone modulation.

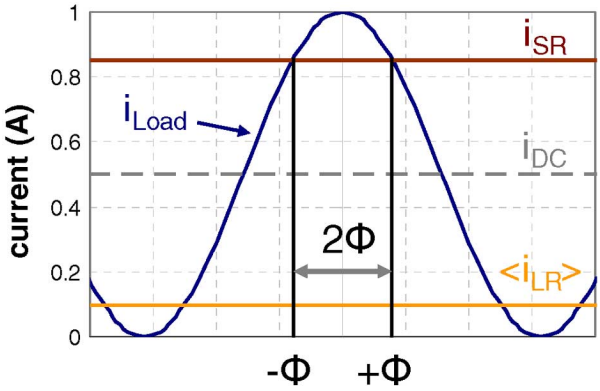

Fig. 4. Conduction angle derivation: sinusoidal AM modulation, normalized peak load current = 1A.

To derive an expression for the average power drawn from the supply, as in (3), the value for $\langle i_{\rm LR} \rangle$ is solved by assuming that $i_{\rm SR}$ is constant during the period of the envelope signal, and finding the corresponding conduction angle, 2Φ, that the linear regulator conducts current from the supply.

Fig. 4 shows a diagram of the current waveforms in the hybrid regulator. If the switching regulator supplies the dc current, the conduction angle of the linear regulator is exactly 180°. This would mean that in the push-pull output stage, the device that couples the output to the supply conducts half of the time. However, in the example shown in Fig. 4, the switching regulator supplies more than the dc current such that $2\Phi < 180°$. The net effect is that the average linear regulator current is reduced by the switching regulator current. For the waveform in (4), Φ can be solved for as

$$\Phi = \cos^{-1}\left(\frac{i_{\rm SR} - i_{\rm dc}}{i_a}\right). \tag{6}$$

Based on (6), the average linear regulator supply current can be written in terms of conduction angle as

$$\begin{aligned} \langle i_{\rm LR} \rangle &= \frac{1}{2\pi} \int_{-\Phi}^{\Phi} (i_{\rm dc} + i_a \cdot \cos(\phi) - i_{\rm SR}) d\phi \\ &= \frac{i_a}{\pi} [\sin\Phi - \Phi\cos\Phi]. \end{aligned} \tag{7}$$

Here, the average linear regulator current is only a function of the amplitude of the load current swing and the conduction

angle. The average efficiency for the ideal system, as in Fig. 2, can be written in terms of the properties of the envelope waveform using (1), (3), and (7), specifically noting that the current the switching regulator draws from the supply is reduced by conversion ratio, d. It should be noted that (7) assumes an ideal switching regulator with no loss. Average efficiency for the sinusoidal AM envelope follows:

$$\langle\eta\rangle = \frac{v_{\rm dc}\cdot i_{\rm dc} + \frac{v_a\cdot i_a}{2}}{i_{\rm SR}\cdot v_{\rm dc} + V_{\rm dd}\frac{i_a}{\pi}\left[\sin\Phi - \Phi\cos\Phi\right]}. \tag{8}$$

In (8), average efficiency is written purely in terms of properties of the envelope waveform, the supply voltage, and the conduction angle, 2Φ, of the linear regulator. Substituting (6) into (8), average efficiency is expressed as a function of the current supplied by the switching regulator, $i_{\rm SR}$. Using this result, an algebraic minimization can be done to find the switching regulator current that provides maximum average efficiency. This is the solution to $d\langle\eta\rangle/di_{\rm SR} = 0$, and can be found as

$$i^*_{\rm SR} = i_{\rm dc} + i_a\cdot\cos\left[\pi\frac{v_{\rm dc}}{V_{dd}}\right] \tag{9}$$

where $i^*_{\rm SR}$ is the optimum quasi-static switching regulator current. The maximum average efficiency, $\langle\eta\rangle^*$, for this value of $i^*_{\rm SR}$ is expressed as

$$\langle\eta\rangle^* = \frac{v_{\rm dc}\cdot i_{\rm dc} + \frac{v_a\cdot i_a}{2}}{v_{\rm dc}\cdot i_{\rm dc} + V_{dd}\frac{i_a}{\pi}\sin\left(\Phi^*\right)} \tag{10}$$

where Φ^* is the optimum conduction angle for the linear regulator, and can be written as

$$\Phi^* = \pi\frac{v_{\rm dc}}{V_{dd}}. \tag{11}$$

As seen in (9), the optimum current supplied by the switching regulator is not necessarily equal to the dc current supplied to the load, but is in fact a function of the dc and dynamic characteristics of the envelope signal as well as the supply voltage. This is a departure from the control schemes presented in [14], [15], where the mean switching regulator current is the dc load current.

The calculation is similar for two-tone signals, except different expressions are obtained for the conduction angle and optimum biasing conditions. For the case that the RF carrier consists of two tones at different frequencies, w_2 and w_1, but equal magnitudes, va, the envelope is a full-wave rectified sinusoid with a peak value of $2\times va$, as in [16]

$$v_{\rm env} = \left|2\cdot v_a\cos\left(\frac{w_2 - w_1}{2}t\right)\right|. \tag{12}$$

In this case, the conduction angle as a function of the switching regulator current is

$$\Phi = \cos^{-1}\left(\frac{i_{\rm SR}}{2i_a}\right) \tag{13}$$

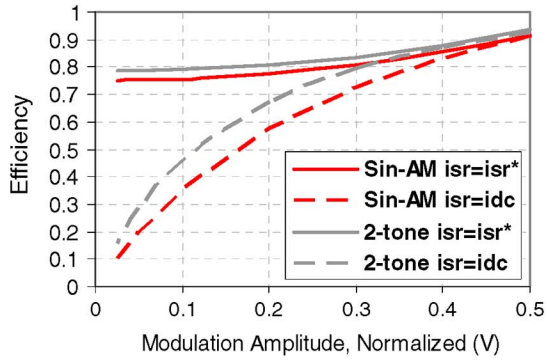

Fig. 5. Theoretical efficiency versus voltage amplitude: sin-AM and two tone cases, following (10) and (15).

where $i_a = v_a/R_{\rm load}$ is the amplitude of the current swing of one of the two tone signals. Following a similar procedure to the sinusoidal envelope signal, the optimum quasi-static switching regulator current contribution for the two-tone case is

$$i^*_{\rm SR} = 2\cdot i_a\cdot\cos\left(2\frac{v_a}{V_{dd}}\right) \tag{14}$$

where V_{dd} is the supply or battery voltage. The maximum average efficiency for the two-tone envelope signal is solved for as

$$\langle\eta\rangle^* = \frac{\pi}{2}\frac{v_a\cdot i_a}{v_a\cdot i_{\rm SR} + V_{dd}\cdot i_a\cdot\left[\sin(\Phi) - \Phi\cos(\Phi)\right]}. \tag{15}$$

For the two-tone case, ideal output efficiency is bounded between 93.3% for rail-rail modulation, and 78.5% (pi/4) as $v_a \to 0$. In theory if the switching regulator supplied the dc current, efficiency would be bounded by 92.7% to 0%. This range fits with the efficiency of 87% for a two-tone envelope as reported in [16].

IV. Theoretical Predictions and Discussion

Fig. 5 shows the theoretical average efficiency for the sinusoidal-AM and two-tone modulated carrier as the modulation amplitude is reduced. The supply voltage is normalized to 1 V, and the modulation amplitude is swept from rail-to-rail swing to nearly zero amplitude. For the sinusoidal AM signal, the carrier is fully modulated such that $v_a = v_{\rm dc}$. The two-tone case assumes two signals at different frequencies with the same amplitude, v_a, as in (12). If the switching regulator contributes the dc load current, average efficiency falls off to 0% as the modulation amplitude is reduced. However, if the switching regulator supplies the optimum current, $i^*_{\rm SR}$, as derived in (9) and (14), the average efficiency can be kept higher across the entire range of operation, as follows from (10) and (15). Therefore, the preferred approach is to regulate the dc switching regulator current to the optimum value rather than the dc value. Intuitively, this can be explained based on the operation of the linear regulator:

- At high output swing levels, the switching regulator supplies the dc current. In this case the linear regulator operation approaches class B, or 180° conduction angle for each push-pull output device. This causes the curves in Fig. 5 to converge for high amplitudes.

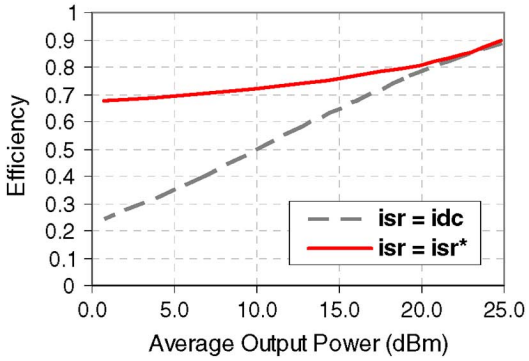

Fig. 6. Efficiency versus normalized voltage amplitude: IS-95 CDMA, from simulation.

- At low output swing the switching regulator sources more than the dc current, such that, for the sinusoidal-AM case, $\lim_{va\to 0} i_{\rm SR} = i_{\rm dc} + i_a$. In other words, the high side pass transistor operates in class-C with the transistor conducting for less than 180°. Alternatively, the low side pass transistor approaches class-A operation, drawing current only from the switching regulator output.

The trend shown in Fig. 5 is also observed for real wireless communication standards. Fig. 6 shows efficiency versus output power for envelope waveforms that correspond to IS-95 code-division multiple access (CDMA). In this case the envelope waveform follows a bandlimited pseudorandom trajectory and is difficult to quantify for hand analysis. Therefore, in Fig. 6, the curves are simulated with behavioral models for the ideal case. The efficiency range for the CDMA waveform is similar to the curves in Fig 5. This is because the sinusoidal-AM, two-tone and CDMA waveforms have similar peak-to-average power ratio (PAPR). PAPR is a measure of the amount of amplitude modulation in the signal and can quantify the difference between the extremes in the envelope voltage and the average envelope voltage [1]–[3]. Generally, higher PAPR values will lead to lower efficiency. This is because the dynamic output voltage may deviate further from the average output voltage reducing the efficiency of the linear regulator.

The difference in average efficiency between the optimum case where $i_{\rm SR} = i^*_{\rm SR}$, and the traditional case where $i_{\rm SR} = i_{\rm dc}$ becomes more pronounced with increasing power backoff. In the case where $i_{\rm SR} = i_{\rm dc}$, average efficiency approaches zero as the output power level is reduced. However, in the optimum case, the efficiency of the hybrid regulator falls asymptotically towards some minimum efficiency level, $\langle\eta\rangle_{\rm min}$. For the cases presented in Fig. 5, $\langle\eta\rangle_{\rm min}$ is between 70–80%. Even in the CDMA case, $\langle\eta\rangle_{\rm min} = 68\%$. Therefore, in situations with extreme power backoff, or when the battery voltage is much higher than the voltage required by the PA, optimum biasing can be highly advantageous. Next generation wireless standards will have power backoff ranges of up to 80 dB [7]. In addition, scaling trends in modern silicon-based power amplifiers will dictate supply voltages well below current lithium-ion battery cell voltages [27]. Both trends will result in significant power savings with the proposed biasing method.

Table I consolidates the optimum bias point expressions and values for average efficiency for the sinusoidal-AM and two-tone cases. The average efficiency boundaries for CDMA and 802.11a envelope waveforms are also shown. For the cellular and wireless internet standards, efficiency boundaries and optimum switching regulator current contribution, $i^*_{\rm SR}$, are found through behavioral simulation. Similar to the results shown in Fig. 5, significant power savings are achieved by using the optimum current, rather than the dc current.

TABLE I
EXPRESSIONS FOR OPTIMUM BIASING AND EFFICIENCY FOR DIFFERENT ENVELOPE SIGNALS

	Sinusoidal AM *	Two-tone **	IS-95 CDMA ***	802.11a/g WLAN ***
i^*_{SR}	$i_{DC} + i_a \cdot \cos(\Phi^*)$	$2 \cdot i_a \cdot \cos(\Phi^*)$	-	-
Φ^*	$\pi \frac{v_{DC}}{V_{dd}}$	$2\frac{v_a}{V_{dd}}$	-	-
$\langle\eta\rangle^*$	$\frac{v_{DC}\cdot i_{DC} + \frac{v_a \cdot i_a}{2}}{v_{DC}\cdot i_{DC} + V_{dd}\frac{i_a}{\pi}\sin(\Phi^*)}$	$\frac{\pi}{2}\frac{v_a}{V_{dd}\sin(\Phi^*)}$	-	-
$\langle\eta\rangle_{\rm max}$	$\frac{3\pi}{2\pi+4} = 91.7\%$	$\frac{\pi}{4\cdot\sin(1)} = 93.3\%$	90%	75%
$\langle\eta\rangle_{\rm min}$	$\frac{3}{4} = 75\%$	$\frac{\pi}{4} = 78.5\%$	68%	50%

* Assume full modulation: $v_a = v_{DC}$ ** Assume two tones with same amplitude, *va*
*** Efficiency boundaries found with simulation

V. EXPERIMENTAL RESULTS AND COMPARISON TO THEORY

A prototype was created to verify the biasing model and compare predictions to experimental results. A first set of experiments was performed to confirm the optimum switching regulator current contribution, $i^*_{\rm SR}$, as in (9). This was done by sweeping the switching regulator current and determining the maximum efficiency. A second set of experiments compared the maximum efficiency for the case where $i_{\rm SR} = i^*_{\rm SR}$ to the case where the switching regulator supplied the dc current, $i_{\rm SR} = i_{\rm dc}$. In the second set of experiments, measurements were taken for a range of output signal amplitudes to verify the predictions of (10) and (15). This was done for the sinusoidal-AM and two-tone modulation cases as well as for real communication standards, which included IS-95 CDMA and IEEE 802.11a wireless internet standards.

The prototype was implemented at the board level with discrete components. A fast operational amplifier (LM7171) driving a class-B common-collector buffer stage (SS8050/8550) was used for the linear regulator. The switching regulator was operated as a voltage-controlled current source using a large, low-loss inductor. In this set of experiments, the switching regulator current was regulated manually at low frequency to control the dc currents from the two regulators. It should be noted that a more advanced implementation could use conventional current-mode control to regulate the switching regulator current as higher bandwidths. Such control methods are well developed in [25], [28], [29] as well as many other references and commercial products.

The experimental efficiency, to be compared to (10) and (15), was calculated as the sum of the average linear regulator current from the supply and the weighted output current of the switching regulator. To verify the ideal expressions in Table I, the switching regulator current was weighted by the factor, d,

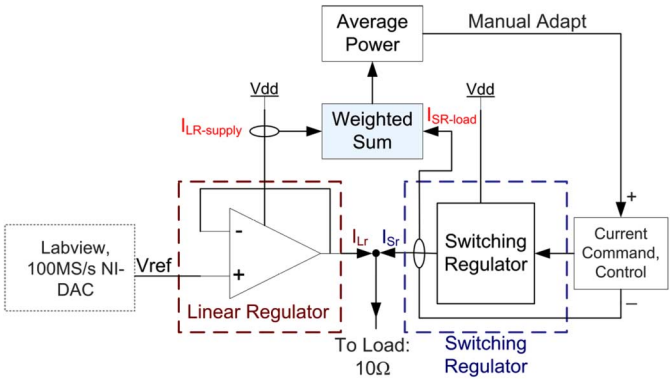

Fig. 7. Experimental setup.

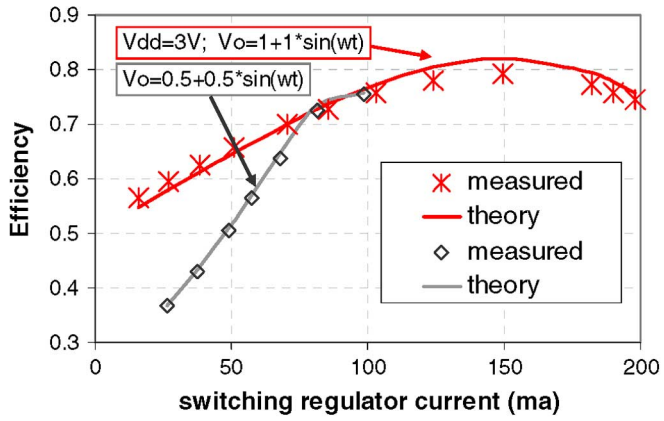

Fig. 8. Average efficiency versus switching regulator current contribution: Sin-AM modulation.

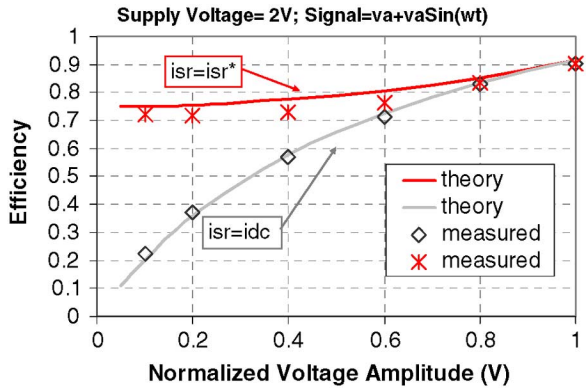

Fig. 9. Average efficiency versus envelope modulation amplitude: Sinusoidal AM modulation.

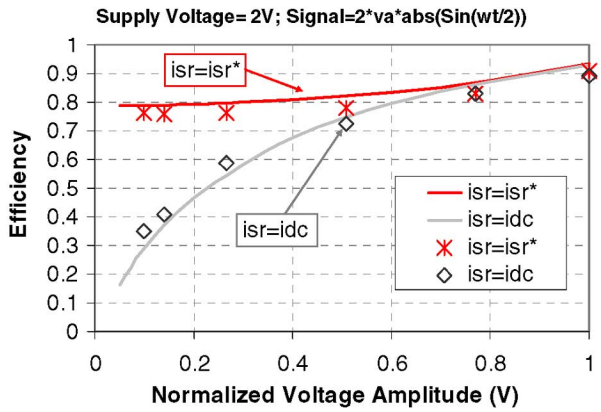

Fig. 10. Two-tone modulation: comparison of theory to measurement.

as in (1), to reflect lossless dc–dc voltage conversion. Lossless conversion was assumed to verify the ideal maximum efficiency case. To further reflect the ideal case, the bias current of 6 mA of the linear regulator was not included in the calculation.

As shown in Fig. 7, the input signal representing the dynamic envelope trajectory was delivered by a National Instruments D/A converter running at 100 MS/s. The Labview software interface was used to generate and supply envelope waveform signals with up to a 20 MHz bandwidth, including IS-95 CDMA and 802.11a WLAN wavefoms. The switching regulator current command was adjusted manually to achieve the highest average efficiency for a given input signal. To simplify the experimental setup, a resistive load was used rather than an actual PA. In this case a 10 Ω resistor was used for the load. The average currents from the parallel switching and linear blocks were measured with digital-multimeters.

Fig. 8 shows average efficiency versus the current contribution of the switching regulator for 2 amplitudes of the sinusoidal-AM waveform. The results are compared to the predicted curve from (9) for a supply voltage of 3 V. To compare the efficiency for the ideal situation, the 6 mA dc bias current of the linear regulator (LM7171) was not included in the calculation. The average voltage delivered to the load for the two curves was 500mV and 1 V, corresponding to power levels 14 dB and 8 dB below maximum power. Efficiency versus switching regulator current is seen to be in good agreement with theory. For the sinusoidal-AM waveforms shown, the peak efficiency is around 80%, which is 2% below the ideal efficiency as predicted in (10).

Similar curves were mapped out for amplitudes varying between 1/20th the supply voltage and rail-to-rail swing. The results corresponding to optimum biasing are shown in Fig. 9 for the sinusoidal-AM case. The measured data are overlaid with the theoretical predictions from Table I. Also shown in Fig. 9 is a comparison of the optimum case where $i_{\rm SR} = i^*_{\rm SR}$, and the traditional case where $i_{\rm SR} = i_{\rm dc}$. For high amplitudes, the agreement between theory and measurement is good. At lower amplitudes, measured efficiency is less than predicted due to extra bias power in the class-B output stage and tolerance in setting the bias current of the switching regulator. The efficiency when the switching regulator supplies the dc power matches theory with good agreement across the range of operation.

Fig. 10 shows measured theoretical data for the two-tone modulated signal as analyzed in Section III and summarized in Table I. The measured data are in good agreement with theory, and match with similar accuracy as the sinusoidal-AM case. The maximum efficiency for full-scale modulation is seen to be 90.6% compared to 93.3% as predicted in Table I.

Fig. 11 shows measured results for CDMA and IEEE 802.11a supply modulation waveforms. These waveforms are generated with the Agilent Advanced Design Systems (ADS) software and

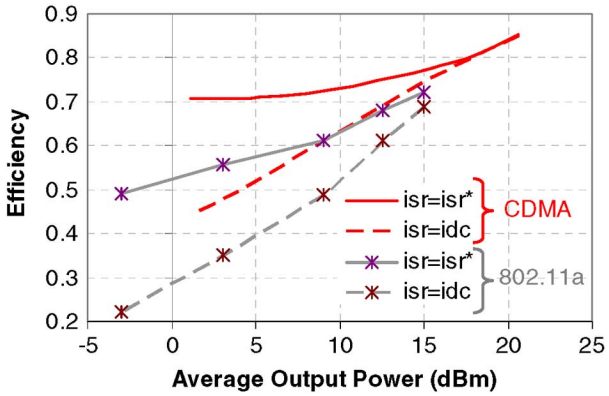

Fig. 11. IS-95 CDMA, 802.11a WLAN measured efficiency.

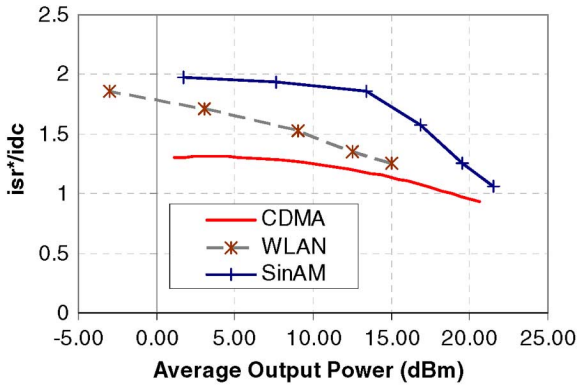

Fig. 12. Optimum switching regulator current (normalized $i^*_{\rm SR}/i_{\rm dc}$) versus output power.

converted to a format suitable for data conversion. The waveforms were delivered to the hybrid regulator with Labview and the NI 5421 DAC, as shown in Fig. 7. The x axis shows average power delivered to the 10 Ω load. In this set of experiments the maximum average power delivered in the CDMA waveforms was just over 20 dBm. The 802.11a waveforms were set to reflect a datarate of 54 MB/s, such that maximum average power was 15 dBm. The higher peak-average power ratio (PAPR) of the 802.11a standard (PAPR = 10.8 dB) is the principal reason that average efficiency is lower than the other waveforms. The higher PAPR of 802.11a indicates that the dynamic output voltage deviates substantially from the average voltage. This reduces the average efficiency of the linear regulator. In the CDMA case, Fig. 11 can be compared to the simulated results shown in Fig. 5. The x axis power scale is slightly different in the two plots because the simulation was run with a 3.3 V supply voltage and a max output power of 1 W.

Fig. 12 shows the relationship between optimum switching regulator current and output power by plotting the ratio of $i^*_{\rm SR}/i_{\rm dc}$ for several envelope signals. At high output power the Sinusoidal-AM and CDMA optimum current is nearly the same as the dc current. The WLAN optimum current is higher at maximum power because the signal has higher PAPR. In all cases, the optimum current increases as output power decreases. In the sin-AM case $i^*_{\rm SR}$ approaches $2 \cdot i_{\rm dc}$ at low output power, as in (9). Some discrepancy is observed due to tolerances in measuring and setting the $i^*_{\rm SR}$ and $i_{\rm dc}$ levels. This is seen in that the CDMA $i^*_{\rm SR}/i_{\rm dc}$ ratio falls slightly below unity at maximum power. Realistically, this is caused by measurement error and because, in the $i^*_{\rm SR}$ optimization process, efficiency versus $i_{\rm SR}$ is relatively flat at its peak. This makes it difficult to set the exact peak efficiency by hand, and leads to slight deviation in optimum $i^*_{\rm SR}$ values from theoretical predictions. Fortunately, because of the shallow minimum in power dissipation, this is without major consequence to average efficiency.

Importantly, Figs. 10–12 show that significant power savings are possible if the switching regulator supplies the optimum current, $i^*_{\rm SR}$, rather than the dc current to the load. The power savings are most dramatic at low output power levels, when the average output voltage is significantly less than the supply voltage. At low power, the switching regulator supplies more than the dc current. This reduces the net current that the linear regulator draws from the supply. In the simple cases of sinusoidal-AM and two-tone modulation, $i^*_{\rm SR}$ can be found by hand calculation with reasonable accuracy. However, the better solution may be to adaptively seek $i^*_{\rm SR}$ with an extremum-seeking adaptive control architecture, such as is presented in [12] for dead-time optimization. As demonstrated in Figs. 10–12, this method promises significant power savings for the hybrid regulator architecture for dynamic supply applications.

VI. Conclusion

We have presented a method for analyzing the bias constraints for hybrid voltage regulators consisting of linear and switching stages operated in parallel. It was shown that when the switching regulator is treated as a quasi-static current source, there is an optimum current contribution from the switching stage that is not equal to the dc current to the load. Instead, optimum efficiency is a function of the dc and dynamic characteristics of the regulated voltage signal, and the supply voltage. Theoretical and simulated results were presented for several envelope waveforms that are relevant to cellular and wireless LAN applications. Measured results were compared to theory and shown to be in good agreement. Optimum quasi-static biasing is shown to have significant advantages over the case where the mean switching regulator is the dc load current, especially for wireless standards with significant power backoff, or when the battery voltage is significantly higher than the maximum PA supply voltage. Our analysis implies a highly practical biasing scheme where the switching regulator operates with only a modest bandwidth, enabling a low cost solution with high efficiency. Overall, this work demonstrates a valuable practical and theoretical limit for the design of dynamic voltage regulation modules.

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