Power Supply Rejection for RF Amplifiers: Theory and Measurements

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***Abstract*—Supply noise is a significant problem in RF systems where it can mix with RF signals, degrading signal/noise ratios and potentially causing violation of spectral masks. This paper presents an analysis of the supply rejection properties of RF amplifiers. We extend a conventional Volterra-series formulation to treat multiport systems and use it to describe the mixing products between power supply noise and the RF carrier. It is shown that a multiport Volterra formulation can be used to treat weak nonlinearities in the system and that the nonsymmetric cross terms accurately predict low-order mixing phenomenon. We demonstrate the validity of our hand analysis through the design and fabrication of a power amplifier in 180-nm CMOS, operating between 900 MHz–2.4 GHz with a maximum output power of 15 dBm. Spectral regrowth of single-tone and EDGE modulation waveforms is shown to match within 1-3 dB across frequency and input signal power. Importantly, this analysis provides insight into the circuit-level mechanisms for susceptibility to power supply noise and can help designers improve the power supply rejection ratio robustness of system-on-chip wireless blocks and transmitter architectures.**

***Index Terms*—dc–dc converter, polar modulation, power amplifier (PA), power supply rejection ratio (PSRR), RF amplifiers, supply noise.**

I. Introduction

THE OUTPUT spectrum of RF amplifiers is highly constrained by Federal Communications Commission (FCC) specifications and performance requirements. In transmitter applications, the frequency content of the output signal must conform to a spectral mask to avoid interference with adjacent channels. Also, to guarantee an acceptable bit error rate (BER) across the wireless link, the error-vector magnitude (EVM) of the modulated RF signal must be kept within tight bounds [1]. In receivers, spectral leakage from noise or distortion can degrade the signal-noise ratio (SNR) and can cause desensitization or cross-modulation [2], [3]. Traditional distortion analysis has focused on near-band spectral regrowth caused by interaction of the input signal with amplifier and component nonlinearities [4]–[10]. However, an additional source of spectral leakage comes from noise or voltage ripple on the power supply. As demonstrated in Fig. 1, spectral energy injected from the power supply can mix with the RF carrier and be upconverted to near-band frequencies. If the RF amplifier has insufficient power supply rejection, supply noise can degrade system performance and even cause violations of the transmit spectral mask [11]. The severe impact of supply noise on wireless system performance makes it especially important to understand the interaction of supply noise with RF amplifier components for successful design of the system.

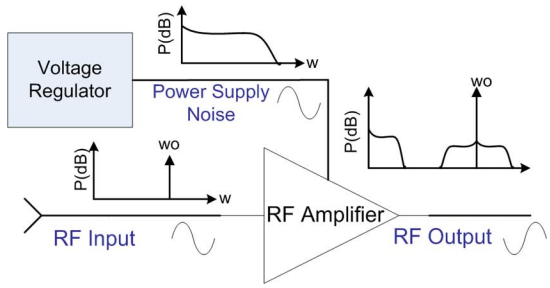

Fig. 1. Effect of supply noise on RF amplifier output spectrum.

In the context of supply noise upconversion, the Volterra series (VS) analysis is a direct and powerful approach to achieve an analytical understanding of the circuit. Harmonic balance techniques can also be applied to study this problem, particularly in simulation with Agilent's Advanced Design System (ADS) or Cadence Spectre's periodic-steady state (PSS) toolset [12]. While harmonic balance techniques are useful to determine voltage and current waveforms in a mixed linear and nonlinear system, solving the harmonic balance equation requires knowledge of the input signal. Furthermore, the order of computation increases with the number of input harmonics. This makes harmonic balance impractical for studying broadband performance metrics such as spectral regrowth and adjacent channel power ratio (ACPR), especially for real wireless systems with nonperiodic amplitude waveforms. In this regard, VS has the following advantages.

- VS can describe the linear and nonlinear dynamics of a circuit without knowledge of the input signal (provided that the circuit remains in a weakly nonlinear regime).
- The Volterra kernels can provide a compact expression of the time- and frequency-domain behavior as a function of physical device parameters, independent of the input waveform.
- The circuit is solved only once (in contrast with harmonic balance, which may need to reiterate for different input waveforms)
- VS analysis allows rapid computation of multitone and broadband behavior, as in [7], and is one of few simulation techniques that is practical for rapid computation of spectral regrowth phenomenon.

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VS is effective in the context of supply noise because noise sources are typically small-signal relative to the operating point of the amplifier. In the layout, common sources of supply noise include magnetic coupling to bond wires and power supply interconnect, electrostatic coupling between nearby traces, and current noise from analog or digital blocks passing through parasitic inductance and resistance in the power rails [13]. Supply noise may also be directly injected into the system by the voltage regulator [14]–[21]. In these cases, supply noise is typically less than 10% and often less than 1% of the dc supply voltage level. With small supply noise amplitude, linear amplifiers typically remain in the weakly nonlinear regime. In this case, VS can often predict performance over many decades of power of the RF input signal.

It is important to note that many of the important sources of supply noise are low frequency relative to the RF signal. Such noise sources are difficult to filter because at low frequency, bypass capacitors are less effective. With low-frequency noise signals, mixing products tend to be more problematic since they create in- or near-band frequency content. As a particular example, in polar and envelope tracking (ET) transmitter architectures, the voltage regulator modulates the supply voltage synchronously with the envelope of the transmitted signal. Many implementations use switching regulators to improve the efficiency of the transmitter across the range of operation [16]–[21]. While this can significantly increase average efficiency, switching regulators produce noise on the power supply at the switching frequency fundamental and harmonics. Switching noise is usually low frequency compared to RF signals and is difficult to filter completely. In the case of PA supply regulation, it is important to know how much voltage ripple is tolerable because over-designing the switching regulator for voltage ripple will be at the expense of efficiency. In our analysis, VS analysis can be used to predict the sensitivity of the power amplifier (PA) to supply ripple through the power supply rejection ratio (PSRR). This analysis can be used to maximize the efficiency of the switching regulator for a given amount of voltage ripple, while simultaneously meeting EVM and ACPR requirements in the transmitter.

In this study, we present an analysis of the power supply rejection properties of RF amplifiers. The focus is on the mechanisms for upconversion of low-frequency supply noise to the nearband RF spectrum. We formulate a VS representation of weakly nonlinear CMOS amplifiers to describe the mixing products between the power supply noise and the RF carrier.

We extend the analysis to treat multiport systems by including nonsymmetric cross terms in a conventional frequency-domain analysis. Specifically, this analysis is an adaptation of the method proposed by Chua and Ng in [9], Schetzen in [4], and described by Wambacq and Sansen in [5]. The calculations are based on nonlinearities extracted from BSIM3v3 models, but result in expressions that are simple enough to use for hand design. We demonstrate the practical use and insight gained through our analysis with the design and fabrication of a linear CMOS PA.

Section II presents the theory for multiple-port signal intermodulation starting with the memoryless analogy. Conventional VS analysis is reviewed and expanded to a multiport formulation to treat RF amplifiers with memory. Section III describes the target problem and the method for characterizing the nonlinearities in the CMOS amplifier. Section IV presents Volterra operators for the supply intermodulation sidebands. Section V compares hand analysis to simulation and experimental results. Spectral regrowth is compared for single-tone and EDGE modulated signals operating in the traditional 900-MHz band, as well as at 2.4 GHz.

II. Theory of Multiple-Port Supply Intermodulation

Power supply noise can mix with the RF carrier and be upconverted to the nearband spectrum. This process happens when the amplifier has stray paths that couple the supply voltage to nodes in the amplifier that modulate the amplitude or phase of the transmitted signal. At high frequencies, it may be easy to filter supply noise with choke inductors or bypass capacitors. It may be more difficult to filter low-frequency supply noise due to limitations on the size of filter elements. Low-frequency supply noise is also problematic because the first-order intermodulation terms may be close to the band of interest.

Analysis of supply-carrier intermodulation is complicated by the dynamics and nonlinearities of the system. If the RF amplifier circuit does not have memory, the distortion products can be analyzed in a straightforward manner with traditional power series analysis [1], [2]. This may be the case if the effects of reactive elements are not significant or can be easily included between stages that have purely conductive or resistive nonlinearities. Such may be the case in a circuit with only diode or transconductance nonlinearity followed by a reactive filter. In this case, the small-signal gain of the amplifier may be characterized as a function of the input voltage and power supply. The nonlinearities of the topology are characterized around a bias point such that the output signal $S_{\rm out}$ can be written as

$$\begin{aligned} S_{\rm out}(S_{\rm in}, S_{vdd}) &= a_{10}S_{\rm in} + a_{20}S_{\rm in}^2 + a_{30}S_{\rm in}^3 \cdots \\ &\quad + a_{11}S_{\rm in}S_{vdd} + a_{21}S_{\rm in}^2 S_{vdd} + a_{12}S_{\rm in}S_{vdd}^2 + \cdots \\ &\quad + a_{01}S_{vdd} + a_{02}S_{vdd}^2 + a_{02}S_{vdd}^3 + \cdots \end{aligned} \tag{1}$$

where a_{ij} are the gain terms as a function of the ith order of the input signal and the jth order of the ac supply voltage noise; $S_{\rm in}, S_{\rm out}$, and S_{vdd} are the signals at the input, output, and supply terminals centered around the operating point. Here, a_{10} describes the first-order forward gain term, a_{01} describes the forward gain from the supply terminal, and a_{11} describes the first-order intermodulation term between the input signal and supply noise. If the input signal follows $S_{\rm in} = v_i \cos(\omega_0 t)$, and the supply noise is a single tone that follows $S_{vdd} = v_s \cos(\omega_S t)$, the amplitude of the supply ripple sideband will be at $\omega_0 \pm \omega_S$ such that

$$v_{\rm out}(\omega_0 \pm \omega_S) = \frac{1}{2}a_{11}v_i v_S. \tag{2}$$

In this case, a useful figure-of-merit is the magnitude of the supply ripple sideband in decibels below the carrier (dBc). As seen in (2), this quantity is relevant because the magnitude of the

supply ripple sideband is directly proportional to the magnitude of the input signal for constant supply noise. It may be practical to treat the supply noise magnitude as constant to reflect the worst case analysis, or when voltage ripple from a switching regulator is of a known fixed magnitude. The supply ripple sideband in dBc is the ratio of the forward gain term to the supply ripple sideband magnitude, the quantity expressed in decibels, as follows:

$$\text{Sideband (dBc)} = \text{dB}\left(\frac{2a_{10}}{a_{11}} \cdot \frac{1}{v_s}\right). \tag{3}$$

Expanding on this figure-of-merit, if the power supply noise is fixed and of constant magnitude, it may be practical to subtract its effect from the relationship in (3). In this case, the ratio becomes signal independent and is only a function of the physical properties of the amplifier. Since the ratio is amplifier specific, it has a notable similarity to the baseband figure-of-merit, the PSRR [22]. In the remainder of this study, we will refer to this ratio as the PSRR for RF amplifiers and define it as

$$\text{PSRR (dBV)} = \text{dB}\left(\frac{2a_{10}}{a_{11}}\right). \tag{4}$$

The units of $(2a_{10})/(a_{11})$ are volts because the expression in (3) has been multiplied by the supply ripple magnitude. This leaves the units of (4) in decibels per volts (dBV). The physical interpretation of PSRR in (4) is the sideband dBc that would occur for a 1-V (0 dBV) supply ripple magnitude. It should be noted that (2) is defined for the memoryless power-series analysis. Next we will describe analysis of power supply intermodulation for systems with dynamics and frequency-dependent nonlinearities.

A. Single-Input (Two-Port) Volterra Analysis

VS can be used to analyze the behavior of nonlinear systems with memory. As long as the system is weakly nonlinear, only a few terms of the series are needed to predict important distortion phenomenon. With a VS representation, the time-domain output of a time-invariant nonlinear system for an input $x(t)$ can be written as

$$y(t) = \sum_{n=0}^{\infty} F_n(x(t)) \tag{5}$$

where

$$F_n(x(t)) = \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} h_n(\tau_1, \ldots, \tau_n) \times x(t-\tau_1)\ldots x(t-\tau_n)d\tau_1 \ldots d\tau_n. \tag{6}$$

In (6), $h_n(\tau_1, \ldots \tau_n)$ are known as the nth-order Volterra kernels of the system. F_n, which represent the convolution integral in (6), are known as the Volterra operators or Volterra transfer functions [4]. From the perspective of (5) and (6), VS appear as a generalized convolution in the time domain. The time-domain Volterra kernels can be used in the frequency domain as Volterra operators or Volterra transfer functions to perform circuit calculations [4], [5], [9], [23]. In this case, the Volterra operators are frequency-dependent transfer functions $H_n(j\omega_1, j\omega_2, \ldots, j\omega_n)$ that capture the phase and amplitude response of the circuit for a given set of frequencies [4]. Many good references elucidate this concept as well as the use of mixed time–frequency-domain descriptions of dynamical nonlinear systems [4]–[10], [23]–[26].

B. Multiport Volterra Analysis

The extension of two-port Volterra analysis to multiport systems can be done by extending the convolution integral in (6) to higher dimensions. The most compact VS representation makes use of tensor notation to concisely describe the multiport operators. The resulting formulation includes both direct terms between each input and the output and cross terms that describe intermodulation among the inputs. As in (1), the first-order cross term can be used to describe mixing between supply noise and RF carrier. The increased dimensionality of multiport Volterra analysis complicates hand analysis, but the first- and second-order terms are still manageable, and can provide considerable insight into the supply noise mixing effect

$$v_{\text{out}}(t) = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} F_{mn}(v_1(t), v_2(t)) \tag{7}$$

$$F_{mn}(v_1(t), v_2(t)) = \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} h_{mn}(\tau_1, \ldots, \tau_{m+n}) \times v_1(t-\tau_1)\ldots v_1(t-\tau_m) \times v_2(t-\tau_{m+1})\ldots v_2(t-\tau_{m+n})d\tau_1 \ldots d\tau_{m+n} \tag{8}$$

$$\begin{aligned} S_{\text{out}} = {} & A_{10}(j\omega_a) \circ S_1 + A_{20}(j\omega_a, j\omega_b) \circ S_1^2 \\ & + A_{30}(j\omega_a, j\omega_b, j\omega_c) \circ S_1^3 + \cdots \\ & + A_{01}(j\omega_a) \circ S_2 + A_{02}(j\omega_a, j\omega_b) \circ S_2^2 \\ & + A_{03}(j\omega_a, j\omega_b, j\omega_c) \circ S_2^3 + \cdots \\ & + A_{11}(j\omega_a, j\omega_b) \circ S_1 S_2 \\ & + A_{21}(j\omega_a, j\omega_b, j\omega_c) \circ S_1^2 S_2 \\ & + A_{12}(j\omega_a, j\omega_b, j\omega_c) \circ S_1 S_2^2 + \cdots. \end{aligned} \tag{9}$$

The time-domain VS formulation for a system with two input ports and a single output may be written as in (7), where (8) is the multiport analogy to the convolution integral in (6). In (7) and (8), h_{mn} is the multidimensional Volterra kernel, v_1 and v_2 are the two input signals, and F_{mn} is the multidimensional Volterra operator in the time domain. In the frequency domain, the VS can be written as in (9). Here, the notation A_{ij} denotes the Volterra operator for the ith order of input S_1, and the jth order of input S_2. The $j\omega_n$ terms are dummy frequency variables that can assume the relevant frequency content of the input signal. The operator "$\circ$" represents the frequency-domain operation of the transfer function on the signals at the appropriate frequencies as is standard in phasor transfer function analysis. The notation in (9) is borrowed from [25]. In (9), A_{10} and A_{01} are the first-order (linear) Volterra operators for each of the two input terminals. The operator A_{11} describes the second-order cross term. A_{21} and A_{12} describe the third-order cross terms. It should be noted that the VS in (9) has structural similarity to the

memoryless analogy in (1). The main difference is that the operators in (9) are a function of the frequency content of the input signal and reflect the weakly nonlinear dynamics of the system.

An additional source of supply modulation may be caused by the PA itself. This happens if the supply terminal (v_s in Fig. 2) is not low impedance to the RF or envelope signal. In this case, the supply terminal may change with the signal amplitude, resulting in second-order and higher order distortion terms. Fortunately, if the system is properly defined, these effects can be captured in conventional two-port VS analysis and will be reflected in the forward-direct operators A_{20}, A_{30}, etc. While self-induced supply noise may be a serious problem in many situations, these effects can be alleviated with good supply bypassing and voltage regulation techniques. In this case, it is necessary to create a low-impedance supply at frequencies correlated with the operation of the PA. In this study, we focus on uncorrelated noise and treat the supply terminal as a separate input. Therefore, the focus is on the A_{11} operator. It should be noted as a possible simplification of the analysis that the self-induced noise can be characterized separately and treated as an independent noise source on the supply. In this case, the A_{11} operator can be used to study both independent and correlated noise from the system.

In this study, we define the N-port amplifier as a black box with $(N-1)$ separate inputs and a single output port. The amplifier represented in Fig. 1 is defined as a three-port system where the inputs are the conventional signal input and the supply terminal. The signal input port may be either single ended or differential, whereas the supply terminal is typically referenced to ground. In this case, A_{10} would correspond to the forward gain at w_0, A_{01} would correspond to the forward supply noise gain at w_S, A_{11} would correspond to the first sideband at $w_O \pm w_S$, and A_{12} and A_{21} would correspond to the second sidebands at $w_O \pm 2w_S$ and $2w_O \pm w_S$. The PSRR of the circuit is, therefore, written as

$$\mathrm{PSRR} = \mathrm{dB}\left|\frac{2A_{10}(j\omega_0)}{A_{11}(j\omega_0, j\omega_S)}\right| \tag{10}$$

where the absolute value is taken to mean the magnitude of the complex operator ratio. It should be noted that the cross terms are not necessarily symmetric since, generally, $A_{11}(j\omega_1, j\omega_2) \neq A_{11}(j\omega_2, j\omega_1)$. Intuitively, this is because the signals may follow different nodal paths to the output, therefore, the frequency content of signals at different ports is not necessarily interchangeable. Asymmetric Volterra transfer functions can be made *partly symmetric* with techniques presented in [23]. As in the case with conventional symmetric operators, partly symmetric operators are desirable to improve computation time and complexity.

III. Target Problem and Characterization of Nonlinearities

In order to demonstrate multiport supply rejection analysis, we designed and fabricated a CMOS PA in 180-nm technology. Fig. 2 shows the basic amplifier cell including inductance at the source and drain to model the effects of the bond wires and RF choke elements. We chose the common-source topology because it is the fundamental gain stage for many RF subsystems

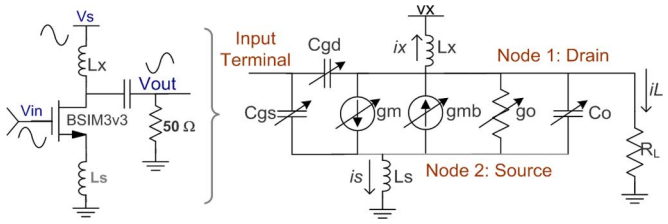

Fig. 2. CMOS inductor-degenerated common source amplifier showing nonlinear elements.

including PAs and low-noise amplifiers. Fig. 2 also shows the major sources of nonlinearity in the CMOS amplifier. In this example, the dominant sources of nonlinearity are the transconductance (gm), output conductance (go), and drain-bulk junction capacitance (Cjd). Other distortion contributors include the body-effect transconductance and gate capacitors, although these typically have a small effect on supply noise upconversion.

Nonlinearities for the system in Fig. 2 were extracted from BSIM3v3 models for static and dynamic nonlinearities. Fig. 3 shows the results of Spectre simulation of the drain current versus gate–source and drain–source voltage. The planar representation of current shows direct dependence on first-order and higher order terms of v_{gs} and v_{ds}. Importantly, there is also cross dependence on terms related to $v_{\mathrm{gs}} \times v_{\mathrm{ds}}$. These cross terms result in mixing effects between the signal and supply and are important to capture for noise analysis. Fig. 3 also highlights the dc operating point relative to the *I–V* plane. The typical operating region follows the loadline for the amplifier, but deviates from a straight line in the *I–V* plane because of nonlinearity, reactive dynamics, and voltage ripple on the supply. Voltage ripple extends the operating region in the vertical (v_{ds}) dimension by swinging the voltage at the drain of the active device.

The nonlinear current and charge relationships were matched to a polynomial fit with least squares regression analysis [5], [6], [10]. The polynomial expansion is fit to physical device parameters such as transconductance and junction capacitance using both current and charge relationships

$$\begin{aligned} id = {} & gm_1 vgs + gm_2 vgs^2 + gm_3 vgs^3 + \cdots \\ & - gmb_1 vsb - gmb_2 vsb^2 - gmb_3 vsb^3 - \cdots \\ & + gmo_{11} vds \cdot vgs + gmo_{12} vds \cdot vgs^2 \\ & + gmo_{21} vds^2 vgs + \cdots \\ & + go_1 vds + go_2 vds^2 + go_3 vds^3 + \cdots \\ & + C_1 \frac{d}{dt} vdb + \frac{C_2}{2}\frac{d}{dt} vdb^2 + \frac{C_3}{3}\frac{d}{dt} vdb^3 + \cdots . \end{aligned} \tag{11}$$

In (11), gm_i represents the forward transconductance, gmb_i is the body transconductance, gmo_{ij} is the output-transconductance cross term as a function of the ith order of vds, and the jth order of vgs, go_i is the output conductance, and C_i is the output capacitance. C_i represents the first-order and higher order parameterization of the output capacitance term (represented as C_o in Fig. 2). The nonlinearity is extracted from the nominally linear charge–voltage relationship, as in [4] and [5], resulting in the factors of 1/2 and 1/3 in the second- and third-order power series terms.

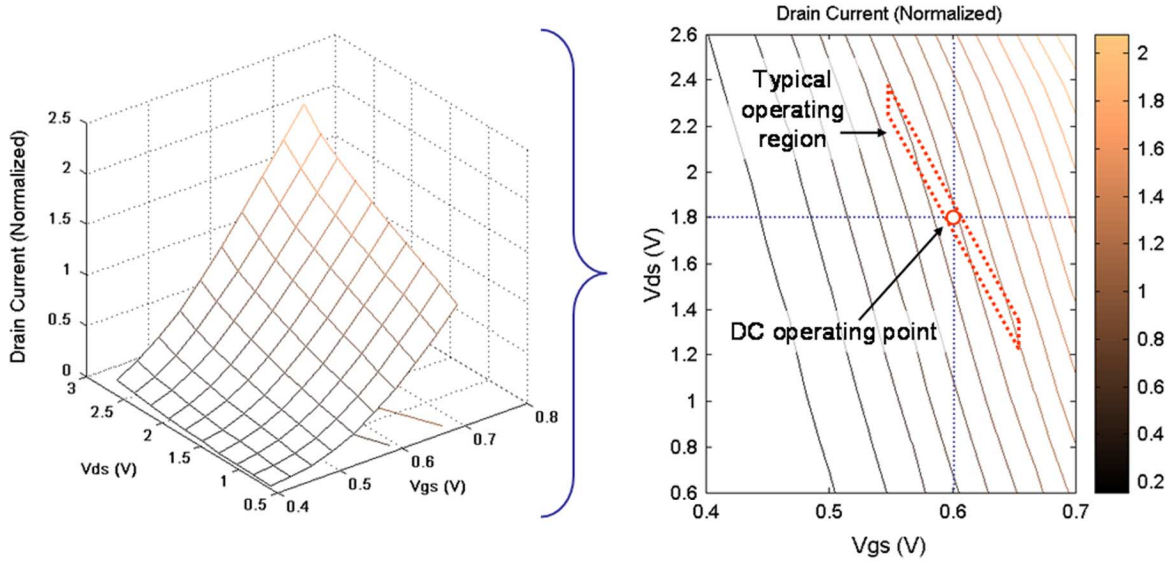

Fig. 3. MOSFET drain current versus gate–source and drain–source voltage. Nonlinearities are extracted around the dc operating point highlighted in this figure.

IV. Solution of Volterra Operators

To solve for the Volterra operators in (9), nodal equations are written and the system is solved sequentially for each order of the polynomial expansion in (11), beginning with the first-order term. This procedure is well described in [4], [5], and [25]. A unique VS is written for each independent node in the system, not including the input terminal, which, in this example, is controlled by a voltage source. The notation for the multinode system can be simplified with a superscript indicating for which node the series is intended. For the source-degenerated amplifier in Fig. 2, there are two independent nodes: one at the source of the active element, and one at the drain of the active element, assuming the blocking capacitor is a short at the frequencies of interest. Using this terminology, the VS in (9) can be written as

$$S_n = \sum_{i=0}^{\infty}\sum_{j=0}^{\infty} A_{ij}^{n}(j\omega_a,\ldots,j\omega_k) \circ S_1^i S_2^j \tag{12}$$

where notation A_{ij}^{n} indicates the operator for the ith order of phasor input S_1 and the jth order of phasor input S_2 for the nth independent node in the circuit. For each node n, all of the first-order terms are solved without initially including the effects of the higher order terms. It should be noted that the first-order terms should match conventional small-signal analysis. The second-order terms are solved based on the nodal constraints of the circuit, the second-order nonlinear currents, and the first-order terms. This process repeats, solving the system of equations for each node in the circuit, until the desired maximum order of the analysis has been achieved [4], [5], [25].

In the rest of the analysis, *node-1* and the corresponding set of operators A_{ij}^{1} will be for the *output node*, while *node-2* and A_{ij}^{2} will be used for the *source node* of the active device. The first-order transfer function for the system in Fig. 2 is solved as

$$A_{10}^{1}(j\omega_a) = -y_S(j\omega_a)\frac{gm_1}{K_0(j\omega_a)} \tag{13}$$

where y_S is the admittance of the source degeneration. The w_a term is a dummy frequency variable that represents the frequency content of the input signal [4], [25]. For inductive degeneration, $y_S(j\omega_a) = (j\omega_a L_S)^{-1}$. The constant K_0 is the recurring denominator in many of the operators, and is evaluated at w_a in (14) as follows:

$$K_0(j\omega_a) = (gm_1 + gmb_1 + y_1)\cdot(y_X + y_L) + y_S \cdot(y_X + y_1 + y_L). \tag{14}$$

In (14), $y_1(j\omega_a) = go_1 + j\omega_a C_1$ is the first-order drain–source admittance representing both first-order conductance go_1 and first-order capacitance C_1, as in (11). The drain–supply admittance is captured in the term $y_x(j\omega_a) = (j\omega_a L_C)^{-1}$, which represents the admittance of the choke inductance L_C. The admittance of the load impedance is captured in $y_L = (R_L)^{-1}$. In (14), the notation for the admittance parameters $y_i(j\omega_a)$ has been simplified to y_i to condense the expression, but it should be noted that these are still a function of $j\omega_a$. For the rest of the first-order terms, we will not explicitly indicate the frequency dependence $(j\omega_a)$ to simplify the expressions.

The rest of the first-order operators follow as

$$A_{01}^{1}(j\omega_a) = \frac{gm_1(y_X + y_L)}{K_0} \tag{15}$$

$$A_{10}^{2}(j\omega_a) = \frac{y_X(gm_1 + y_1 + gmb_1 + y_S)}{K_0} \tag{16}$$

and

$$A_{01}^{2}(j\omega_a) = \frac{y_X y_L}{K_0}. \tag{17}$$

In (15)–(17), the denominator expression K_0 is the same as in (14), and is evaluated at the frequency content of the input signal w_a, as are all the admittance terms. These expressions fully characterize the first-order behavior between the input signals and each node in the circuit. The Volterra operator that characterizes mixing between the supply noise and the input signal is defined by the A_{11}^{1} term. In this case, A_{11}^{1} operates on both the

RF input signal and the signal representing noise on the supply terminal

$$v_{\text{out}}(\omega_o \pm \omega_S) = A_{11}^1(j\omega_0, j\omega_S) \circ [Vi(\omega_0), Vs(\omega_S)] \quad (18)$$

where w_0 and w_S are the frequencies of the RF carrier and supply ripple, respectively. As previously noted, the A_{11}^1 operator is not fully symmetric in this representation because the supply noise and RF input signal follow substantially different paths to the output.

The A_{11}^1 operator is solved by including the cross terms in the VS in (9). The resulting operator is shown in (19). Here, the A_{11}^1 operator is organized in a clear manner by splitting the effects of the device parameters (gm_i, y_i, etc.), and the effects of the first-order operators, which are lumped into parameters K_1–K_4. In (19), $y_2 = go_2 + j(\omega_a + \omega_b)C_2$ is the second-order drain–source admittance, $y_S = (j(\omega_a + \omega_b)L_S)^{-1}$ is the source admittance, and constant K_0 in the denominator is evaluated at $j(\omega_a + \omega_b)$. The K_1, K_2, K_3, K_4 terms are frequency-dependent transfer functions that are a function of the first-order operators. These are shown in (20)–(23). Here, the frequency of the input RF signal is represented by ω_a and the frequency of supply noise is represented by ω_b

$$A_{11}^1(j\omega_a, j\omega_b) = y_S \frac{gmo_{11}K_1 + 2y_2K_2 + 2gm_2K_3 - 2gmb_2K_4}{K_0} \quad (19)$$

$$K_1(j\omega_a, j\omega_b) = A_{01}^2(j\omega_b)\left[1 + A_{10}^1(j\omega_a) - 2A_{10}^2(j\omega_a)\right] - A_{01}^1(j\omega_b)\left[1 - A_{10}^2(j\omega_a)\right] \quad (20)$$

$$K_2(j\omega_a, j\omega_b) = A_{01}^2(j\omega_b)\left[A_{10}^1(j\omega_a) - A_{10}^2(j\omega_a)\right] + A_{01}^1(j\omega_b)\left[A_{10}^2(j\omega_a) - A_{10}^1(j\omega_a)\right] \quad (21)$$

$$K_3(j\omega_a, j\omega_b) = A_{01}^2(j\omega_b)\left[1 - A_{10}^1(j\omega_a)\right] \quad (22)$$

$$K_4(j\omega_a, j\omega_b) = -A_{10}^2(j\omega_a)A_{01}^2(j\omega_b). \quad (23)$$

As seen in (19), upconversion of supply ripple results from second-order nonlinearity in several of the device parameters. Major contribution to upconversion happens through second-order nonlinearity of *output conductance* (go_2), *drain junction capacitance* (C_2), and *dependence of the forward transconductance on* v_{ds} (gmo_{11}). Source inductance provides degeneration and reduces the supply noise mixing. However, large values of source degeneration increase the contribution of *second order transconductance parameters* $(gm_2$ *and* $gmb_2)$.

Following the derivation of (4) and (10), the PSRR can be written as $\text{PSRR} = \text{dB}|(2A_{10}^1)/(A_{11}^1)|$, in which case many of the terms in (13) and (19) are cancelled. The resulting expression for the CMOS amplifier follows as

$$\text{PSRR} = \text{dB}\left|\frac{gm_1}{gmo_{11}K_1 + 2y_2K_2 + 2gm_2K_3 - 2gmb_2K_4}\right|. \quad (24)$$

In (24), the denominators in the expressions for A_{10}^1 and A_{11}^1 are cancelled. Also, there is no dependence on the signal amplitudes. This leaves straightforward dependency only on circuit variables, device parameters, and frequency. Consequently, the PSRR can be thought of as a signal independent circuit parameter and can be used to predict supply rejection for many input signals and noise levels.

The PSRR in (24) indicates which parameters make the circuit susceptible to supply noise. This makes it useful for amplifier configuration and design. High power supply rejection is achieved by limiting the effects of several circuit variables, while simultaneously increasing the forward transconductance. Specifically, to maximize PSRR, it is best to have a high ratio of gm_1 to all sources of second-order nonlinearity at the drain terminal. To improve PSRR, the designer may: 1) increase gm_1 to achieve higher forward gain; 2) reduce second-order conductive nonlinearity (go_2) at the drain terminal; 3) reduce the effects of nonlinear junction capacitances (C_2); or 4) reduce the transconductance cross term (gmo_{11}) by shielding the drain terminal from supply noise. In many cases, a cascode transistor may be highly effective at improving PSRR since it may shield the drain of the active transconductor from supply variation. The improvement may be limited to low frequencies, however, since the cascode will still have nonlinear junction capacitance C_{jd} affecting the output terminal.

V. Comparison to Measurement

A common-source class-A/AB PA was designed and fabricated in 180-nm CMOS to verify the distortion model and the spectral regrowth caused by power supply noise. The amplifier circuit consisted of thin oxide active nMOS devices with off-chip matching to allow the frequency band to be adjusted in the laboratory. The amplifier was sized to achieve a maximum output power of 15 dBm when driving a 50-Ω load. The voltage gain of the packaged amplifier was designed to be approximately 10 dB at 2.4 GHz with the input matched to 50 Ω and 300 pH of inductive source degeneration due to bond wires. A current-mirror bias network was included on-chip to set the quiescent point for the amplifier and filter board-level parasitic signals at the input terminal of the amplifier. The supply voltage for the thin-oxide devices was 1.8 V.

Fig. 4 shows the amplifier topology and bias network. Parasitic inductors are shown to represent the effects of the bond wires and printed-circuit board trace inductance. Not shown are the blocking and bypass capacitors that are placed at the board level. Fig. 5 shows the laboratory test setup. The test setup included voltage sources for biasing the amplifier, a variable RF signal generator, an arbitrary waveform generator to inject noise on the power supply, and a spectrum analyzer to measure the output harmonics. To minimize bond-wire parasitics, the chip was bonded directly to the board. A photograph of the test integrated circuit (IC) bonded to the board is shown in Fig. 6. Several downbonds to the ground plane were used to minimize the source inductance. The parasitic bond-wire inductance was deembedded with a network analyzer. Inductance at the input–output terminals was measured in the 2–4-nH range. Inductance between the source terminal and ground was deembedded with S-parameter measurements and was confirmed to

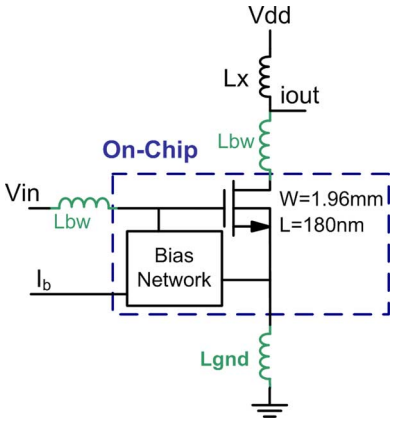

Fig. 4. Common-source amplifier model.

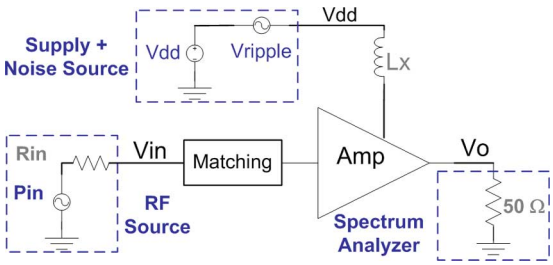

Fig. 5. Laboratory test setup.

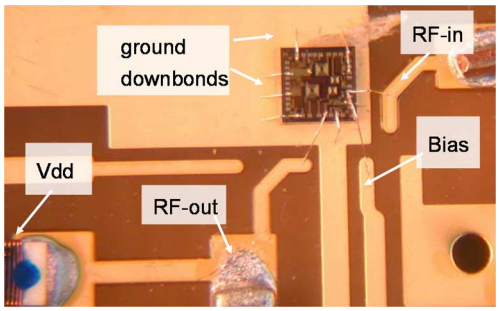

Fig. 6. Die bonded on the gold-plated test board. Die area is 1.4 mm × 1.4 mm.

be less than 300 pH due to multiple downbonds to the ground plane.

A. Sideband and PSRR Measurement

The input RF power was swept from −30 to 10 dBm at a carrier frequency of 2.4 GHz. Supply ripple was injected at a frequency of 1 MHz with amplitude of 50 mV to represent the first harmonic of the switching noise of a dc–dc converter. Fig. 7 compares measured results to hand analysis. As predicted by the VS analysis, the second-order supply ripple sideband varies linearly with input power. At low output power, the fundamental and sideband harmonics match hand analysis within 1–2 dB. At high output power, the amplifier experiences moderate to strong nonlinearity as the drain voltage starts to clip. The PSRR is reduces in this case because of strong conductive nonlinearities in the CMOS device when it enters compression. In this case, higher order terms are needed to maintain the accuracy of the VS analysis.

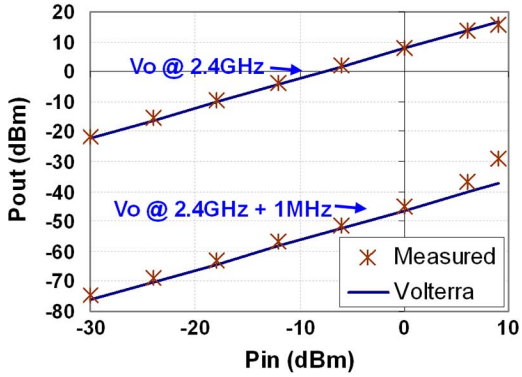

Fig. 7. Comparison of measured and calculated fundamental and ripple sideband power.

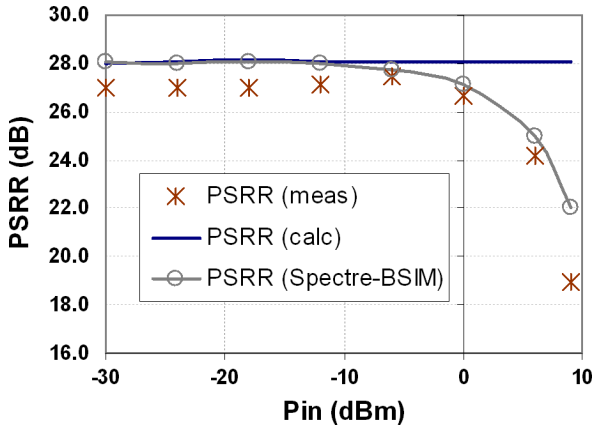

Fig. 8. Comparison of measured and calculated ripple sideband in dBc.

Fig. 8 shows the PSRR of the amplifier versus input power. From (3), PSRR is related to the sideband (dBc) measurement as $\text{PSRR (dBV)} = \text{Sideband (dBc)} + \text{Supply Noise (dBV)}$. It is noted that this ratio should be constant and independent of the input signal level for constant supply noise levels. As described in Section II, this is a useful figure-of-merit for constant or worst case supply noise analysis and represents the sideband dBc that would occur for a 1-V (0 dBV) supply ripple magnitude. In Fig. 8, this is also compared to the prediction in (24) using Volterra analysis, as well as simulation in Spectre with BSIM3v3 models. Sideband power is seen to match hand analysis within 1–2 dB for input powers less than 0 dBm. Similar to Fig. 7, the discrepancy between measured and calculated data increases as the amplifier enters saturation. The PSRR decreases in this case because the amplifier is more susceptible to power supply noise. Simulated date matches well with hand analysis at low power, but deviates as the amplifier enters saturation. Simulated data also matches measured data within 1–3 dB, except at high power. The deviation at low power is partly explained by variation in deembedded values for circuitry parasitics including inductive source degeneration. In Figs. 7 and 8, the VS analysis is seen to be accurate over a 30-dB range of output power. It is expected that this trend would continue to be accurate for input power less than −30 dBm because the amplifier would remain in the weakly nonlinear regime.

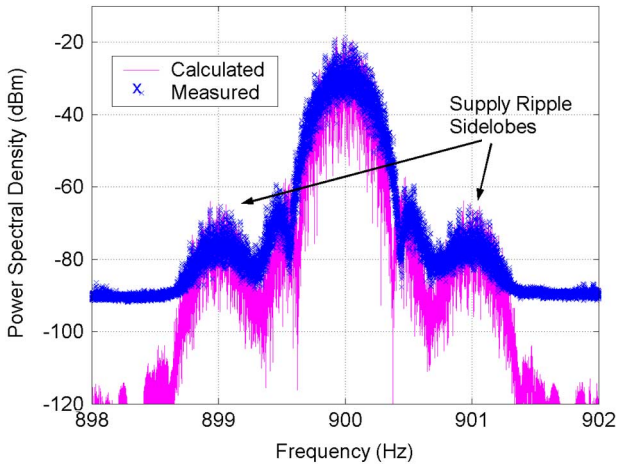

Fig. 9. Measured versus calculated power spectral density at 900 MHz.

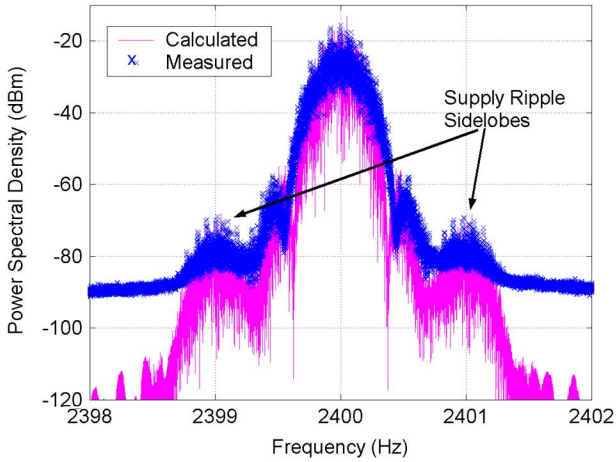

Fig. 10. Measured versus calculated power spectral density at 2.4 GHz.

B. Spectral Regrowth Measurements

Baseband in-phase (I) and quadrature (Q) signals were generated for 8-phase-shift keying (8-PSK) EDGE with a symbol rate of 270 kHz. The baseband signals were oversampled at 32 samples per symbol and saved in 1248-symbol-long data streams. Using the technique described in [7], the baseband signals were upconverted and applied to the Volterra model in the frequency domain to generate the predicted output spectrum. To study the generation of supply ripple sidelobes, only the first-order direct and second-order cross terms were used for the calculation. Spectral regrowth due to third-order nonlinearity was not included because it is well treated in [7] and [8] and is not dominant in supply ripple mixing.

The I and Q signals were upconverted and supplied to the CMOS amplifier in the laboratory using National Instruments' PXI-5421/5620 RF test system. To verify the model at different carrier frequencies, EDGE modulation was applied in the traditional 900-MHz carrier range, and also at 2.4 GHz. The output spectrum was measured and compared to the predictions of the Volterra analysis.

Fig. 9 shows the measured output spectrum overlaid with the spectrum generated with multiport VS analysis. The traditional EDGE spectrum is shown centered at 900 MHz. Due to supply ripple injected at 1 MHz, sidelobes appear centered at 899 and 901 MHz. The sidelobes are images of the EDGE spectrum and have a peak at around 50 dB below the main lobe. The calculated spectrum matches the measured spectrum within 1–3 dB across the frequency range, demonstrating the accuracy of the multiport Volterra model at 900 MHz. Fig. 10 shows similar spectral regrowth centered at 2.4 GHz ± 1 MHz. In the VS calculation case, the ripple sidelobes are clear since the noise floor is arbitrarily small. The measured data shows a noise floor of -90 dBm (for the settings used for National Instruments' PXI downconverter), but the sidelobes are still clear and match the predicted spectrum within 1–3 dB.

C. PSRR: Component-Level Analysis

Importantly, the Volterra analysis provides a tool to study the device-level mechanisms for amplifier nonlinearity. The contribution of the circuit-level nonlinearities can be broken down, as shown in Fig. 11. Here, the PSRR is shown for the three dominant sources of supply ripple upconversion, i.e.: 1) modulation of the forward transconductance by $Vdd(gmo_{11})$; 2) second-order output conductance (go_2); and 3) second-order drain junction capacitance (C_2). In Fig. 11, we are effectively plotting the PSRR as we add in the effect of dominant contributors to supply noise upconversion. It should be noted that when there is no source of supply noise upconversion, the PSRR is theoretically infinite. When the effect of gmo_{11} is added, PSRR is reduced from infinity to the edge of the shaded region in Fig. 11.

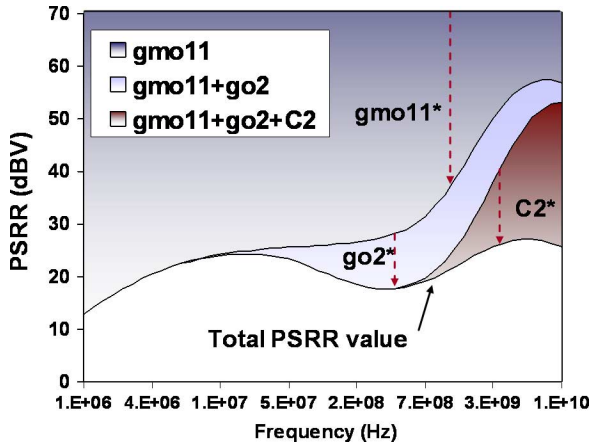

Fig. 11. PSRR versus carrier frequency, from VS analysis, showing contributions of dominant circuit-level nonlinearities. *Change in PSRR when effect of parameter is included (i.e., gmo_{11} is shown to reduce PSRR from infinite to the edge of the shaded region indicated in the legend).

At low frequencies, the effect of reactive elements is minimal since they look like shorts (inductors) or opens (capacitors). Therefore, the dominant impact of supply noise is that it modulates the forward transconductance by changing the $V_{\rm ds}$ of the transistor (i.e., the gmo_{11} term from (11) dominates). This is shown by first nulling the effects of the second-order drain–source admittance parameters go_2 and C_2. When the effects of go_2 and C_2 are included, the PSRR drops at moderate to high carrier frequencies. The second-order drain–source conductance (go_2 term) becomes important at frequencies where

the output resistance of the active device is comparable to the impedance of the choke inductor. The nonlinearity of the drain junction capacitance (C_2 term) is important at high frequency when the drain capacitance dominates the output impedance of the device. The peaks in the PSRR curve are related to resonance of the choke and source inductance. At high frequency, the PSRR increases because of the increasing impedance of the inductive degeneration. However, this effect is partially reduced by the nonlinearity of the output junction capacitance C_2. At low frequency, PSRR falls off with the impedance of the choke inductor because the forward gain is reduced. The effects of gm_2 and gmb_2 are only appreciable with high values of source degeneration. These terms are dominated by gmo_{11}, C_2, and go_2 in this example since there is only 300 pH of inductive degeneration. An additional potential source of supply-carrier intermodulation is high impedance in the input signal path. This causes the supply voltage to couple through the $C_{\rm gd}$ directly modulating the gate terminal. For low-frequency supply noise, the effect of $C_{\rm gd}$ coupling is small because the $jwC_{\rm gs}$ admittance is negligible. This effect is not included in (19)–(24) for simplicity, but can be captured by including the gate terminal as an additional node in the Volterra analysis.

As seen in Fig. 11, VS analysis provides a way to examine the performance of the circuit and design for robustness against power supply noise. In the common-source example, a cascode can increase PSRR substantially. The cascode topology increases the forward gain, and shields the drain of the active transconductance element from variations in Vdd. This reduces upconversion of supply noise through the gmo_{11}, go_2, and $C_{\rm gd}$ terms. Overall, this analysis demonstrates many benefits in providing insight into the circuit design procedure.

VI. Conclusion

A method of predicting the interaction of power supply noise with the RF carrier was presented and compared to measured data. Conventional distortion analysis was extended to a multiport formulation to predict supply ripple intermodulation with the RF signal. Relative measurement of ripple sideband power showed agreement within 1–2 dBc of prediction. Spectral regrowth of the EDGE spectrum due to supply ripple upconversion at 900 MHz and 2.4 GHz was shown to match within 1–3 dB. Multiport Volterra analysis was confirmed to be a valuable tool to predict upconversion of supply noise over a range of frequency and signal input power. The analysis can dramatically reduce simulation time, as also discussed in [7], by converting lengthy time-domain simulation to narrowband frequency-domain or mixed time–frequency-domain computation. This can provide insight into the design of RF amplifiers to provide improved power supply rejection, more robust topologies for system-on-chip (SOC) solutions, and improved efficiency and performance of polar and ET PAs.

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