High-Efficiency, 12V-to-1.5V DC-DC Converter Realized with Switched-Capacitor Architecture

Vincent W Ng, Michael D Seeman, Seth R Sanders
University of California, Berkeley
{vwng, mseeman, sanders}@berkeley.edu

Abstract

This paper presents a 12V-to-1.5V Switched-Capacitor (SC) DC-DC converter in a 0.18µm technology. This work shows that unlike the traditional buck converter, SC converters can achieve high efficiency even with a significant step-down conversion ratio. This circuit shows a peak efficiency of 93% at 200mA load and a maximum load of 1A. This work demonstrates the vast potential of SC converters for large voltage conversion in deep-submicron CMOS technologies when cost and efficiency are important.

Keywords: Switched-Capacitor, DC-DC converter

Introduction

After decades of voltage scaling, high step-down-conversion-ratios are required in point-of-load application where a DC-DC converter is placed close to an associated load. The traditional buck converter suffers from low efficiency or poor power device utilization when used in a high-conversion-ratio application [1]. As explained in [1] and later shown in Fig. 6, Switched Capacitor (SC) DC-DC converters, on the other hand, can sustain high efficiency with a high conversion ratio because each integrated power device only needs to block a fraction of the input voltage and supports a fraction of the output current. SC converters also enable the usage of more-efficient low-voltage transistors in a deep submicron technology to build a high voltage DC-DC converter. In this paper, we report on the design and test result of a 12V-to-1.5V SC converter in a 0.18µm CMOS technology with a peak output current of 1A and a peak efficiency of 93%. This design utilizes triple-well to enable junction isolation of each power device, so that no transistor sees a voltage over-stress, even though each terminal itself may be as high as 15V above the substrate. Latch-up concern is mitigated by the robustness of triple-well structures [2].

Architecture

Fig. 1 shows the schematic of the 8-to1 Dickson converter [3]. As explained in [1] and [3], the Dickson converter operates in two phases, and achieves voltage conversion through charge sharing among capacitors C1-C7. The phase in which a switch is turned on is indicated by the number in bracket next to the switch name in the figure; the switch is turned off in the other phase. The clock generator and the drivers of switches S1 and S2 are powered by the output voltage of 1.5V. The clocks are level-shifted to the appropriate driver by the level-shifter circuit shown in Fig. 2.

Capacitors C1-C10 are implemented using off-chip ceramic capacitors with values ranging from 0.47µF to 2.2µF. These values are determined by optimization method [1] and practical capacitance values. These capacitors have a much lower aggregate cost, aggregate PCB footprint and height than the single inductor used in the buck converter.

Switches S1-S4 are implemented using 0.18µm 1.8V NMOS transistors as they only need to block 1.5V. The other switches (S5-S14) need to block 3V, and are implemented using 0.6µm 5V transistors. Each of the 1.5V switches and 3V switches are 75mm wide and 16mm wide respectively. These widths are determined by optimization method [1] and effects of gate drive capacitance and parasitic resistances. Each switch is driven by its respective driver block, as indicated in Fig 1. Each driver block resides in a voltage domain locally powered from two of the capacitors C1-C10.

Circuit Design

Fig. 2 shows the details of the level-shifter circuit [4] that conveys the clock across voltage domains. Voltage domain 2 is repeated multiple times depending on the number of voltage domains, but is only shown once in the figure.

Active clamping circuits are implemented to limit the peak voltage level of each voltage domains during shutdown, when the converter no longer switches and the voltages of capacitors C1-C10 may drift in an unanticipated manner.

During startup, the SC converter is initially isolated from the input source with a single full-voltage-rated pass transistor while an auxiliary linear regulator charges up the output rail. The SC converter then operates in charge-pump (boost) mode to charge up all the capacitors to pre-determined values. The pass transistor is then activated, followed by turn-off of the

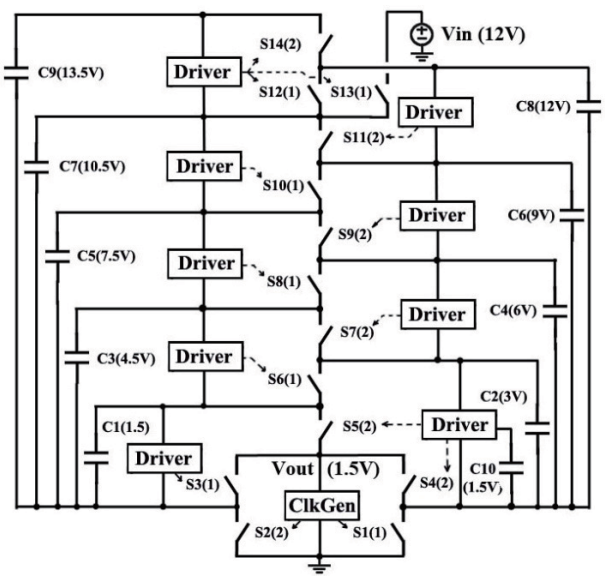

Fig. 1: Schematic of the overall circuit. The numbers in bracket indicate their respective clock phases. The dotted arrows show the respective driver block that drives each switch

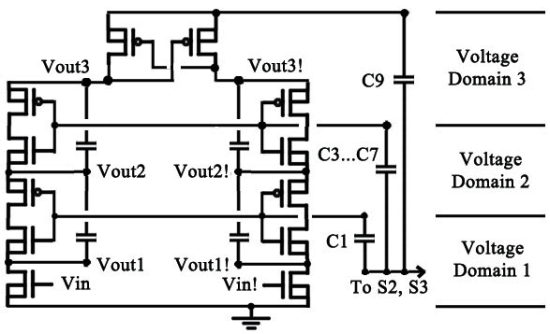

Fig. 2: Schematic of the level-shifter circuit. S2, S3 and C1-C9 correspond to the capacitors and switches in Fig. 1

linear regulator. Helper transistors [5], as shown in Fig. 3, are implemented to enable operating the circuit in boost mode since the main switches are not utilized before the capacitors are charged up. The auxiliary linear regulator and the full-voltage-rated pass transistor are not included in this design.

Layout and Experimental Results

Fig. 4 shows the die photo of the circuit. All switches are located at the periphery of the die to minimize the on-chip metal resistances. Multiple bond pads are placed in parallel for each 1.5V switch terminal, which sees the biggest impact from parasitic resistances [1]. Decoupling capacitors are added in the middle empty space to reduce the effects of parasitic inductances of the bond-wires, which can cause ringing. Including the decoupling capacitors, total active area is $3mm^2$. In the future, solder bump interconnect will allow a reduction in the total die area, as well as power loss since parasitic resistances of bond-wires and on-chip metal account for 50% of the total power loss at 1A load current.

Fig. 5 shows the test result of 1.43V output at 200mA load current, 1MHz switching frequency and with 24µF of decoupling output capacitance. Fig. 6 shows the 93% peak efficiency of this work, and compares this work with other works from industry and literature. This work has a higher efficiency than the surveyed buck and SC converters. Unlike this work, most SC converters are designed for low-conversion-ratio applications, and they also suffer from reduced efficiency at high conversion ratios. Our topology demonstrates superior performance compared to previous work largely due to improvements in the architecture, circuit design and better device utilization.

This work reports on the circuit designs that allow the usage of deep-submicron CMOS technologies to build a high voltage DC-DC converter. This work shows that the SC converter has a huge potential of achieving higher-efficiency and lower-cost than the buck converter in high-conversion-ratio applications, which is currently dominated by the latter.

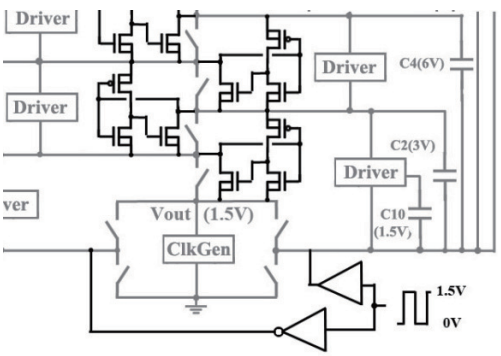

Fig. 3: Schematic of the helper switches (in black) that enable boost mode. The part in gray is a portion of the circuit in Fig. 1

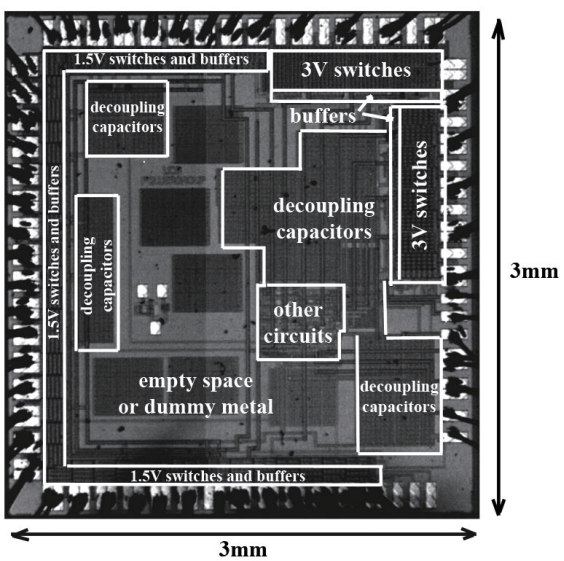

Fig. 4: The die photo of the fabricated design.

Acknowledgement

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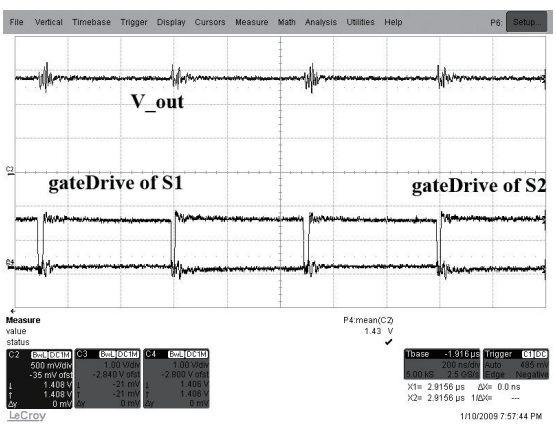

Fig. 5: The output voltage level (V_out) and gate drive signal of switches S1 and S2. V_out has a scale of 500mV/div whereas the other two signals have a scale of 1V/div.

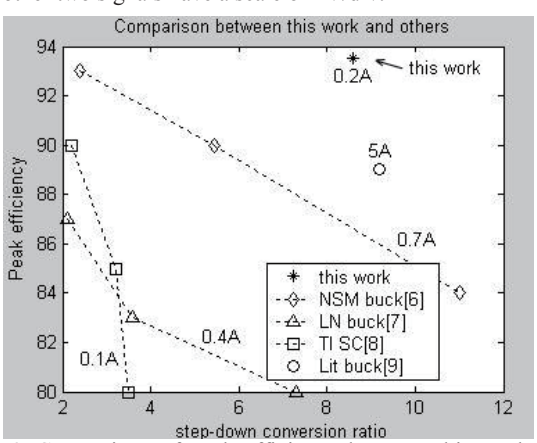

Fig. 6: Comparison of peak efficiency between this work and others in industry and literature. The label indicates output current level in which the converter achieves peak efficiency.