Lossless Voltage Regulation and Control of the Resonant Switched-Capacitor DC-DC Converter

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***Abstract*—This paper presents an approach for nominally lossless regulation of the output voltage, and for design of tight closed-loop voltage control of a resonant switched-capacitor (ResSC) dc-dc converter. A switching pattern for the ResSC dc-dc converter that enables wide range lossless voltage regulation and zero voltage switching (ZVS) is developed. An appropriate small signal model is derived based on the generalized averaging method. In view of the dynamics of the developed small signal transfer functions, a compensation method based on a minor phase loop is introduced to stabilize the system. The steady state and transient responses of the system are evaluated based on the developed model. The performance of the proposed controller is verified by a switch-based simulation in a design example for on-chip power delivery application.**

I. Introduction

Switched-capacitor (SC) based power converters have shown great promise for enabling full integration in recent research, due to the favorable high energy density of on-chip capacitors [1] [2] [3]. However, power density in standard switched capacitor converters is limited by the available capacitor density of a given technology, along with frequency of operation and a trade-off with efficiency. Recently, resonant switched-capacitor (ResSC) based converters have been proposed as an approach that can reduce the intrinsic charge-sharing loss in SC operation, by introducing a small inductor in series with the flying capacitor [4] [5]. This approach enables converters with higher efficiency and power density for full or near-full integrated designs. Specifically, by avoiding charge sharing losses, substantially larger voltage swings can be sustained on the working capacitors, enabling this increased power density, while not compromising efficiency.

In addition, by strategic design of the switch gating pattern, lossless voltage regulation of the ResSC is enabled. To date, some regulation methods have been proposed for the ResSC converter [6] [7] [8]. By decoupling the phase control of two stacked sections of the ResSC circuit, lossless voltage regulation is enabled. With this modality, the circuit can best be viewed as a stacked series resonance converter. Thus, the well known control methodologies based on frequency tuning, phase-shifting, and/or phase-plane all can be brought to bear on the problem. In the particular embodiment studied in this paper for a high frequency IC application, a nominally fixed phase angle is applied between the upper and lower half-bridge networks. Frequency adjustment is then the remaining control input. In order to effect nominally lossless zero-voltage switching, operation above resonance is maintained, in conjunction with properly adjusted deadtimes. Parasitic capacitances associated with devices, flying capacitor bottom and top plates, and inductor capacitances constitute the contributing components to potential dynamic switching losses.

In this work, the authors follow the framework of developing an analog control based on the small signal model. The steady state operation of the ladder type 2-to-1 ResSC is first analyzed. Operation above resonance is presumed to effect zero voltage switching (ZVS). Based on the generalized averaging method [9], the state space small signal model of the converter is derived. According to the dynamics of the model, the authors develop a compensation method relying on a phase feedback minor loop. The switch-based simulations show the effectiveness of the developed model and proposed regulation scheme. The remainder of the paper is organized as follows: Section II introduces the operation of the ResSC with enabled ZVS feature; Section III presents the large signal phasor model and steady state of analysis with ZVS output range; Section IV presents the small signal model and control design based on the dynamic analysis; Section V presents the verification of the developed model and proposed controller from both small signal

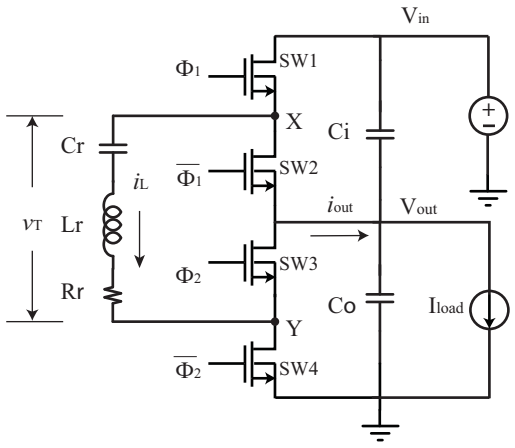

Fig. 1. A Ladder Type 2-to-1 Resonant Switched-capacitor DC-DC Converter

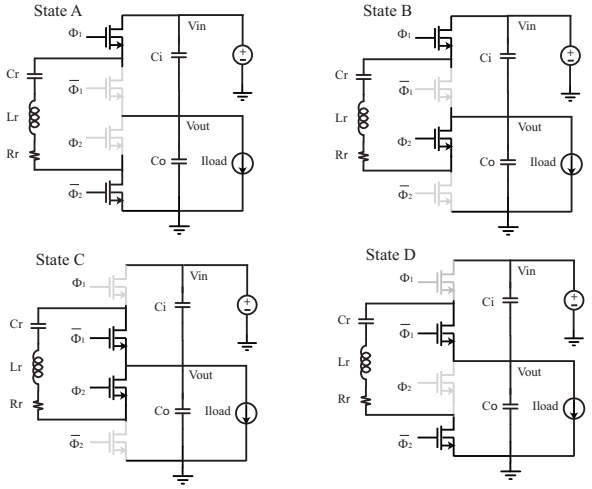

Fig. 2. Different States of the ResSC

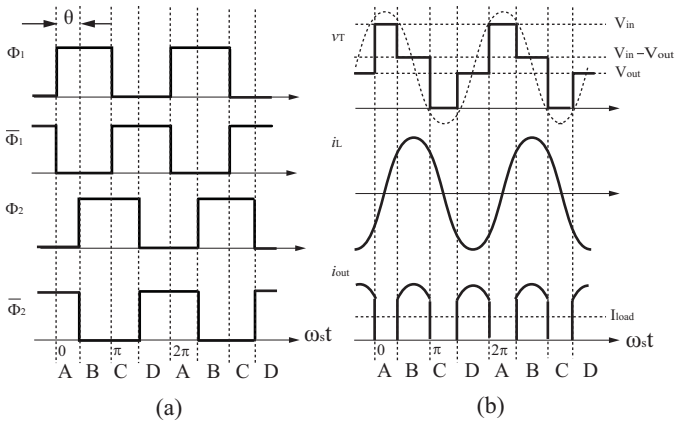

Fig. 3. (a) Switch Gating Patterns of the ResSC (b) Waveforms of the Tank Voltage, Inductor Current and Output Current

based and switch based simulation; Section VI concludes the paper.

II. Operation with Zero Voltage Switching

A ladder type 2-to-1 resonant switched-capacitor converter is shown in Fig. 1. C_r and L_r form the resonant tank. C_i and C_o are decoupling capacitors. R_r represent all the series resistance within the tank which includes the switch resistance, and the ESR of the inductor and capacitors. There are two complementary switch pairs SW_1/SW_2 and SW_3/SW_4. Each switch pair is driven by a square wave with 50% duty cycle. The switching of SW_1/SW_2 leads that of SW_3/SW_4 by a phase angle of θ. Fig. 3(a) shows the gating signals for each switch. With this switching pattern, the converter has four different switch states: A, B, C, and D, as shown in Fig. 2. Fig. 3(b) shows the representative waveforms of the tank voltage v_T, the inductor current i_L and the output current i_{out}, when operating above resonance.

Zero voltage switching (ZVS) for all four switches is desirable to improve the converter efficiency. More precisely, the tank current i_L needs to flow into node X and out of node Y before turning SW_1 or SW_4 on, in which case I_L needs to be negative given reference direction defined in Fig. 1. Similarly, a positive tank current favors the soft turn-on of both SW_3 and SW_2. By operating the converter under the proposed switching sequence above resonance, the tank current naturally meets the ZVS requirement for all four switches.

However, this condition is not true for all possible operation points. In order to benefit from the ZVS, the zero crossing of the tank current should be constrained within the interval set by switching actions of the top switch pair and the bottom switch pair. This leads to an acceptable output range with ZVS for proposed ResSC operation, which will be illustrated in Section III after the large signal phasor model is introduced.

III. Large Signal Model and Steady State Analysis

Fig. 4(a) shows a simplified circuit model of the resonant converter in Fig. 1. We view the system as an LCR tank driven by two square waves V_s and V_o at nodes X and Y. Assuming the Q of the tank is high, as enforced by design, we can further simplify the system by considering only the fundamental sinusoidal components of the square waves and use phasors to describe the system. $\overrightarrow{V_X}$ (the sending phasor) and $\overrightarrow{V_Y}$ (the receiving phasor) represent phasors of two driving signals.The magnitudes of $\overrightarrow{V_X}$ and $\overrightarrow{V_Y}$ are $\frac{2}{\pi}(V_{in}-V_{out})$ and $\frac{2}{\pi}V_{out}$ respectively and $\overrightarrow{V_X}$ leads $\overrightarrow{V_Y}$ by a fixed phase angle of θ. $\overrightarrow{V_T}$ represents the phasor of tank

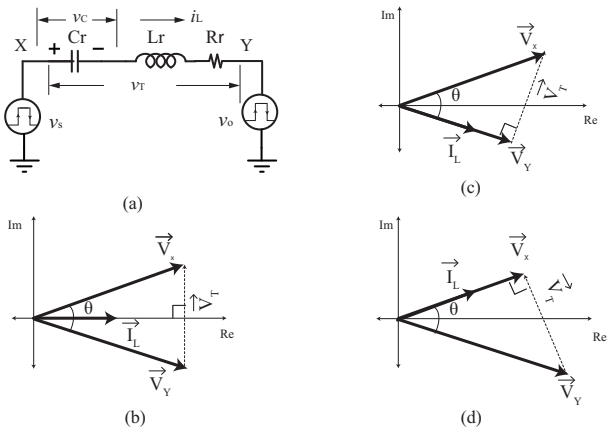

Fig. 4. Large Signal Phasor Model of the ResSC

voltage which is the difference between $\overrightarrow{V_X}$ and $\overrightarrow{V_Y}$. $\overrightarrow{I_L}$ represents the phasor of inductor current which should be perpendicular to the tank voltage phasor under high Q assumption. Phase angle θ is a design parameter, selected based on desired voltage regulation range, and on efficiency considerations.

As discussed above, in order to benefit from ZVS operation, the zero crossing current i_L should happen between the switching actions of SW_1 and SW_3. In phasor domain, this means the tank current phasor $\overrightarrow{i_L}$ should be contained within the phase angle set by the sending phasor $\overrightarrow{V_Y}$ and the receiving phasor $\overrightarrow{V_X}$.

Nominally for a 2-to-1 converter, we have $V_{out} = \frac{1}{2}V_{in}$. In this case, the sending and receiving phasor have the same magnitude such that current phasor is aligned in the middle of the phase angle as shown in Fig. 4(b). However, as the output voltage is modulated, the magnitude of the sending and receiving phasor adjust. This leads to the movement of the position of the current phasor. As the output voltage decreases, the current phasor $\overrightarrow{I_L}$ moves closer to the receiving phasor $\overrightarrow{V_X}$. Therefore, the minimum output voltage with ZVS happens when the tank current is aligned with the receiving phasor, as shown in Fig. 4(c). Similarly, the case of maximum output voltage happens when the tank current is aligned with the sending phasor, as shown in Fig. 4(d). From the geometry of the right triangle, the ideal output voltage range with ZVS is therefore given by:

$$\frac{V_{in}\cos\theta}{1+\cos\theta} < V_{out} < \frac{V_{in}}{1+\cos\theta} \tag{1}$$

We can see that the output range with ZVS can be adjusted by properly choosing θ. This offers the major benefit of the resonant switched-capacitor converter over conventional switched-capacitor converter, since the latter sacrifices efficiency to achieve the regulation of the output voltage. In the design example for VIN=2V and a 2-to-1 topology, with $\theta = \frac{\pi}{4}$, the output can be losslessly adjusted from 0.83 to 1.17. As can be seen, larger angles θ result in greater adjustment range, but at the cost of degraded power factor at sending and receiving terminals with attendant efficiency costs.

To obtain an analytic expression for the steady state operation, we apply the generalized averaging method [9] to the state-space equations of the converter which read:

$$\begin{aligned}
\frac{di_L}{dt} &= \frac{1}{L_r}[(V_{in}-v_{out})s_i - v_{out}s_o - ... \\
&\qquad - v_{out}s_o - i_L R_r - v_c] \\
\frac{dv_C}{dt} &= \frac{1}{C_r} i_L \\
\frac{dv_{out}}{dt} &= \frac{1}{C_o}[s_o s_i i_l - (1-s_i)(1-s_o)i_L - I_{load}]
\end{aligned} \tag{2}$$

where s_i and s_o represent the switching function of $SW1$ and $SW3$, which takes the form:

$$\begin{aligned}
s_i &= \frac{1}{2}\{sign[sin(\omega t)]+1\} \\
s_o &= \frac{1}{2}\{sign[sin(\omega t-\theta)]+1\}
\end{aligned} \tag{3}$$

Applying operator $\langle\bullet\rangle_1$ to the i_L and v_C state equations and operator $\langle\bullet\rangle_0$ to the v_{out} state equation, we obtain:

$$\begin{aligned}
\frac{d\langle i_L\rangle_1}{dt} &= -j\omega\langle i_L\rangle_1 + \frac{1}{L_r}[(V_{in}-\langle v_{out}\rangle_0)\langle s_i\rangle_1 - ... \\
&\qquad - \langle v_{out}\rangle_0\langle s_o\rangle_1 - \langle i_L\rangle_1 R_r - \langle v_C\rangle_1] \\
\frac{d\langle v_C\rangle_1}{dt} &= -j\omega\langle v_C\rangle_1 + \frac{1}{C_r}\langle i_L\rangle_1 \\
\frac{d\langle v_{out}\rangle_0}{dt} &= \frac{1}{C_o}(\langle s_o\rangle_{-1}\langle i_L\rangle_1 + \langle s_o\rangle_1\langle i_L\rangle_{-1} + ... \\
&\qquad + \langle s_i\rangle_{-1}\langle i_L\rangle_1 + \langle s_i\rangle_1\langle i_L\rangle_1 - I_{load})
\end{aligned} \tag{4}$$

where $\langle\bullet\rangle_k$ represent the kth order complex Fourier coefficient, which is also equivalent to the phasor transformation in [10]. Using high Q assumption and neglecting the output voltage ripple, the first order Fourier coefficient $\langle i_L\rangle_1$ and $\langle v_C\rangle_1$ and the zero order Fourier coefficient $\langle v_{out}\rangle_0$, which is real, capture the most significant properties of the tank and the output. We then decompose the complex coefficients into their real and imaginary parts

$$\begin{aligned}
\langle i_L\rangle_1 &= X_{i_L} + jY_{i_L} \\
\langle v_C\rangle_1 &= X_{v_C} + jY_{v_C}
\end{aligned} \tag{5}$$

and with

$$\langle s_i \rangle_1 = -j\frac{1}{\pi}$$
$$\langle s_o \rangle_1 = -j\frac{1}{\pi}e^{-j\theta} \tag{6}$$

The real fifth order state space equations are obtained:

$$\begin{aligned}
\frac{dX_{i_L}}{dt} &= -\frac{R_r}{L_r}X_{i_L} + \omega Y_{i_L} - \frac{1}{L_r}X_{v_C} + \frac{1}{L_r}\frac{2}{\pi}sin\theta V_{out} \\
\frac{dY_{i_L}}{dt} &= -\omega X_{i_L} - \frac{R_r}{L_r}Y_{i_L} - \frac{1}{L_r}Y_{v_C} + ... \\
&\quad + \frac{1}{L_r}\frac{2}{\pi}(1+cos\theta)V_{out} - \frac{1}{L_r}V_{in} \\
\frac{dX_{v_C}}{dt} &= \frac{1}{Cr}X_i + \omega Y_{v_C} \\
\frac{dY_{v_C}}{dt} &= -\omega X_{v_C} + \frac{1}{Cr}Y_{v_C} \\
\frac{dV_o}{dt} &= \frac{1}{C_o}[-\frac{1}{\pi}sin\theta X_{i_L} - \frac{1}{\pi}(1+cos\theta)Y_{i_L}) - I_{load}]
\end{aligned} \tag{7}$$

With that, we obtain the steady state equation that sets the operating point

$$\begin{aligned}
I_{load} = -\frac{1}{\pi}\frac{\frac{2}{\pi}\omega C_r}{(1-\frac{\omega^2}{\omega_o^2})^2 + (\frac{\omega}{\omega_o Q})^2}[sin\theta(1-\frac{\omega^2}{\omega_o^2})V_{in} - ... \\
-(1+cos\theta)\frac{\omega}{\omega_o Q}(V_{in}-2V_o)]
\end{aligned} \tag{8}$$

with

$$\omega_o = \frac{1}{\sqrt{LrC_r}}$$
$$Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_r} \tag{9}$$

From Eq. 8, the operating points of the converter (ω, V_o and I_{load}) are uniquely determined given certain V_{in}, θ. The proposed method uses the switching frequency ω as the tuning parameter for the output voltage regulation under varying load and setpoint commands. The phase angle is chosen for the expected output range and is not tuned dynamically.

IV. Small Signal Model and Control Design

To obtain the small signal model, we apply the small signal pertubation to Eq. 7. Then the real fifth-order small signal state space matrix is obtained as Eq. 10. Based on that, the small signal transfer functions from the switching frequency to the output voltage ($\| H \|_{\omega \to v_o}$) and frequency to the resonant current

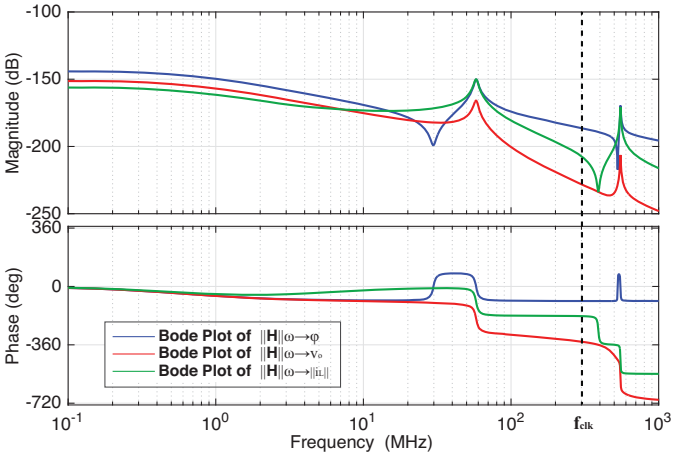

Fig. 5. Bode Plot of $H_{\omega \to \phi}$, $H_{\omega \to v_o}$ and $H_{\omega \to \|i_L\|}$

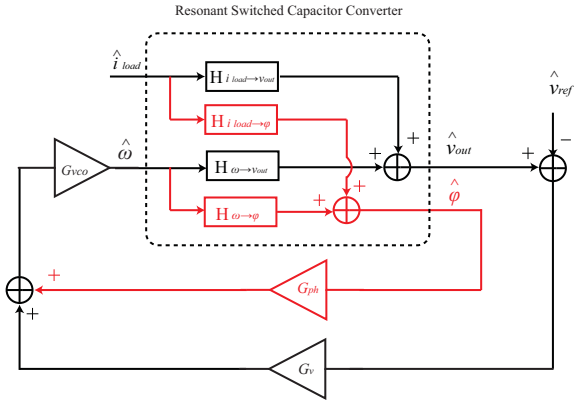

Fig. 6. Small Signal Block Diagram of Close Loop System

($\| H \|_{\omega \to \|i_L\|}$ and $\| H \|_{\omega \to \phi}$) are evaluated using Matlab.

Consider an reasonably achievable design example for the chip-level power delivery application with $L_r = 1nH, C_r = 405pF, R_r = 25m\Omega, C_o = 10nF$, a set of operating points, according to Eq. 8, give $f_{clk} = 300MHz, Vin = 2V, Vout = 1V, I_{load} = 500mA, \theta = \pi/4$. The Bode plots of the transfer functions are shown in Fig. 5. We can see from the Bode plot of $H_{\omega \to v_o}$ that there is a dominate pole introduced by the output capacitor, contributing a 90° phase lag and magnitude drop, followed by two complex conjugate poles, contributing another 180° phase lag and a large resonant peak in the magnitude response around the 50MHz. This makes it challenging to do compensation with a pure voltage loop at high crossover frequency. However, looking at the transfer function of $H_{\omega \to \phi}$, a 180° phase lead, thanks to the complex conjugate zeros at a lower frequency than the resonant poles, is present. Therefore, we propose to take advantage of the phase lead in the current phase transfer function by adding in a phase loop to stabilize

$$\begin{bmatrix} \frac{d\hat{x}_{i_L}}{dt} \\ \frac{d\hat{y}_{i_L}}{dt} \\ \frac{d\hat{x}_{v_C}}{dt} \\ \frac{d\hat{y}_{v_C}}{dt} \\ \frac{d\hat{v}_o}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_r}{L_r} & \Omega & -\frac{1}{L_r} & 0 & \frac{1}{L_r}\frac{2}{\pi}\sin\theta \\ -\Omega & -\frac{R_r}{L_r} & 0 & -\frac{1}{L_r} & \frac{1}{L_r}\frac{2}{\pi}(1+\cos\theta) \\ \frac{1}{C_r} & 0 & 0 & \Omega & 0 \\ 0 & \frac{1}{C_r} & -\Omega & 0 & 0 \\ -\frac{1}{C_o}\frac{1}{\pi}\sin\theta & -\frac{1}{C_o}\frac{1}{\pi}(1+\cos\theta) & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{x}_{i_L} \\ \hat{y}_{i_L} \\ \hat{x}_{v_C} \\ \hat{y}_{v_C} \\ \hat{v}_o \end{bmatrix} + \begin{bmatrix} Y_{i_L} & 0 \\ -X_{i_L} & 0 \\ Y_{v_C} & 0 \\ -X_{v_C} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix} \begin{bmatrix} \hat{\omega} \\ \hat{i}_{load} \end{bmatrix}$$

$$\begin{bmatrix} \hat{v}_o \\ \| \hat{i}_L \| \\ \hat{\phi}_{i_L} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ \frac{X_{i_L}}{\|i_L\|^2} & \frac{Y_{i_L}}{\|i_L\|^2} & 0 & 0 & 0 \\ -\frac{Y_{i_L}}{\|i_L\|^2} & \frac{X_{i_L}}{\|i_L\|^2} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{x}_{i_L} \\ \hat{y}_{i_L} \\ \hat{x}_{v_C} \\ \hat{y}_{v_C} \\ \hat{v}_o \end{bmatrix} \tag{10}$$

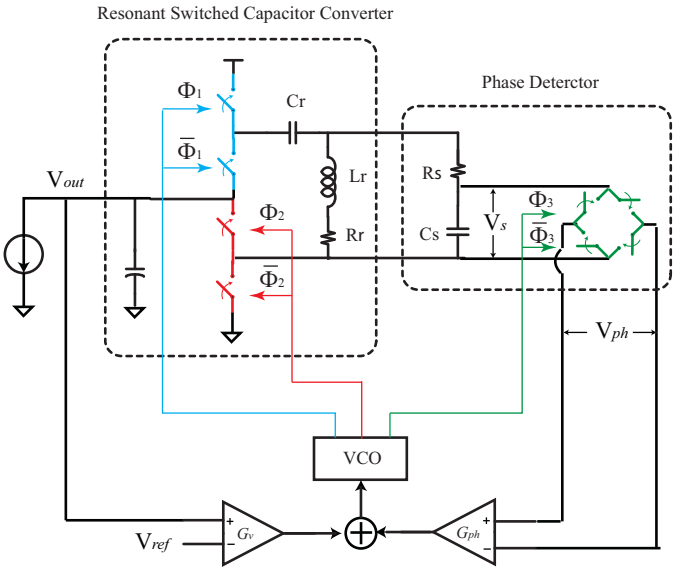

Fig. 7. Circuit Implementation of the Close Loop Resonant Switch Capacitor Converter

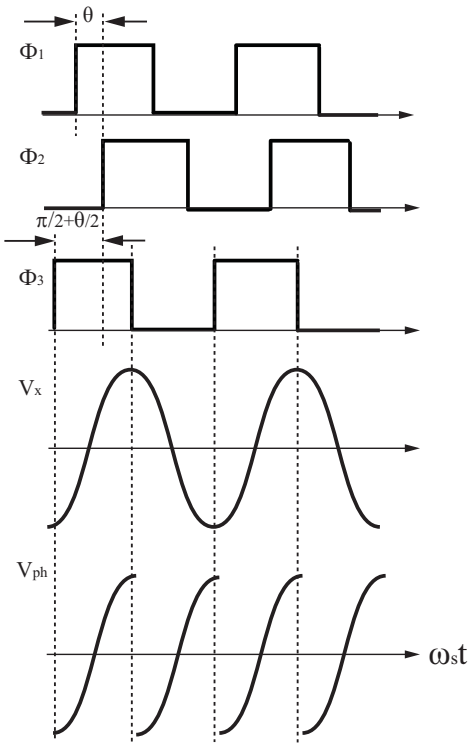

Fig. 8. Waveform of Phase Detector

the system. With that, a proportion-integral (PI) voltage loop is used for reduction of the DC error. The degree of compensation can be adjusted by properly choosing respective gains of the phase loop and voltage loop. Fig. 6 shows the small signal control block diagram.

V. Simulation Verification and Circuit Implementation

To verify the small signal model and proposed control methodology. We implement the converter and control loop using switch model based simulator PLECS. In order to implement the phase loop, we use a passive phase sensing scheme as shown in Fig. 7. The R_s and C_s form a passive "lossless" current sensor. With the matched time constants of $R_s \cdot C_s$ and L_r/R_r, the voltage across C_s (V_s) replicates the voltage drop on the parasitic resistance of the inductor. Moreover, as the inductor frequency is much higher than the corner frequency set by L_r/R_r, a slight mismatch of the time constants would not result in any significant error in the phase information captured by V_s. V_s is then mixed with a reference clock through an H-bridge. Fig. 8 shows the waveform of the reference clock (Φ_3), V_s and V_{ph}. The reference clock (Φ_3) is shifted 90° ahead relative to the middle of the top (Φ_1) and bottom clock(Φ_2). The DC component of the output (V_{ph}) from the mixer approximates the phase

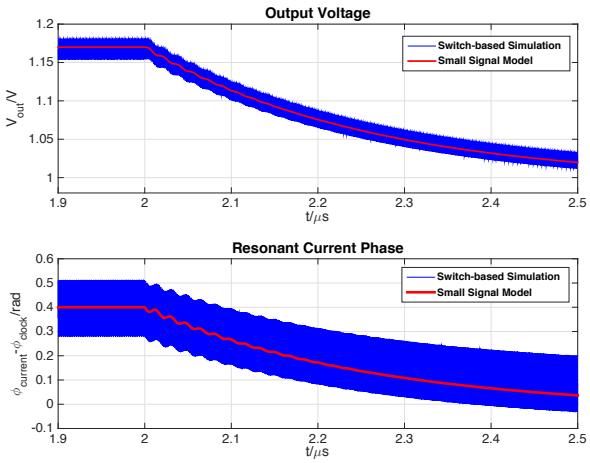

Fig. 9. Open Loop Comparison of Small Signal Model and Switch Based Simulation

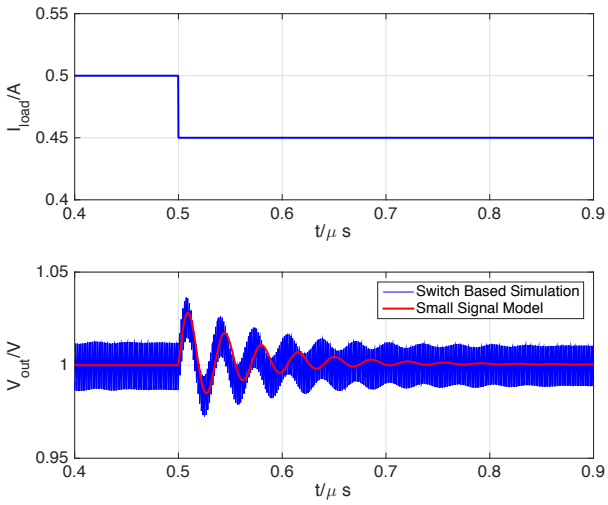

Fig. 10. Load Transient Comparison of Small Signal Model and Switch Based Circuit Simulation

error if the phase error is small:

$$\langle V_{ph}\rangle_0 = \parallel I_L R_r \parallel \frac{2}{\pi} sin\theta \approx \parallel I_L R_r \parallel \frac{2}{\pi}\theta \qquad (11)$$

The scaling effect caused by the current magnitude is accounted for in the gain of G_{ph}. The design here can be extended as one phase leg of a multi-phase converter.

With the developed small signal mode, a control design with proposed dual loop is presented

$$\begin{aligned} G_{ph}(s) &= G_1 \frac{1}{1+\frac{s}{p}} \\ G_v(s) &= G_2 \frac{s+z}{s} \end{aligned} \qquad (12)$$

where, $G_1 = 4, G_2 = \frac{1}{10}, p = 1.01e8, z = 6.28e8$. The low pass filter in the phase loop is used for reducing the high frequency harmonics of the phase error. In a multi-phase system, the low pass filter can be eliminated due to the harmonics cancellation from interleaving. The voltage loop consists of a simple PI controller for management of DC error. The gains of phase and voltage loops are selected so that closed-loop sytem is stable and well compensated. The small signal signal dynamics of the converter are verified with open loop simulation. Fig. 9 shows the dynamic response of the output voltage and current phase under a frequency step of $1MHz$, we see that circuit simulation match the developed small signal model very well. Fig. 10 shows the closed-loop transient response of the voltage output under a $50mA$ load step. The overshoot and response time from the switch based circuit simulation match well with the prediction from the developed small signal model.

VI. Conclusion

Operation and regulation considerations of the ResSC circuit have been introduced. After exploring the operating strategies and large signal characteristics of this promising circuit, a detailed development of the circuit dynamics has been undertaken using a harmonic averaging methodology. The method and models developed lead to simple strategies for control design and implementation.

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