Digital PWM IC Control Technology and Issues

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Digital Control Advantages

- implement advanced control schemes
  - multi-mode control (high/low power modes)
  - adaptive algorithms
  - spread-spectrum switching for EMI reduction
- flexibility and programmability
- integrate supervisory functions - fault detection, management, and reporting
- communicate with other digital devices - voltage scaling
- immunity to analog component variations and noise
- largely automated digital design flow
Digitally-Controlled Buck Converter

$V_{ref}$

digital PWM controller

$V_d$

$\Delta V_{adc}$

$\Delta V_{dpwm}$

quantizers

power train

$V_{in}$

$L$

$C$

load

$I_o$

$V_d$ --

$V_{in}$

$V_x$

$V_{out} = DV_{in}$

discrete duty ratio

$0$

$DT$

$T$
Quantization Resolution Issues

- Microprocessor VRM example

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$V_{out}$</th>
<th>$\Delta V_{dpwm}$</th>
<th>$N_{dpwm}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 V</td>
<td>1 V</td>
<td>5 mV</td>
<td>11 bits</td>
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</table>

- IC Digital PWM (DPWM) implementation with $f_{sw} = 1$ MHz requires
  - $2^{11} \times 1$ MHz = 2 GHz clk in counter-comp. scheme
  - $2^{11} = 2048$ stages in a ring-oscillator-mux scheme
- Analogous requirement on A/D sampling process
Limit Cycling

- Possible limit cycling in steady state at freq. < fsw
- Hard to predict amplitude and frequency
- Output noise, EMI

Resolution (DPWM) < Resolution (ADC)
Limit Cycling Avoided

- Resolution (DPWM) > Resolution (ADC)
- Use integral term in control law
No-Limit-Cycle Conditions

1. Resolution (DPWM) > Resolution (ADC)
2. Integral control is used
3. Nyquist stability criterion satisfied
   (quantization modeled with describing function)
Digital Dither (2-bit)

switched voltage waveform before the output LC filter:

average duty cycle:

- $Dc_1$
- $Dc_1 + \frac{1}{4}LSB$
- $Dc_1 + \frac{1}{2}LSB$
- $Dc_1 + \frac{3}{4}LSB$
- $Dc_2 = Dc_1 + LSB$

low frequency pattern
high frequency pattern (lower ripple)
Experimental Example

\[ N_{dpwm} = 7 \text{ bit hardware} \]
\[ N_{adc} = 9 \text{ bit} \]
\[ V_{in} = 5 \text{ V}, \quad V_{ref} = 1.5 \text{ V}, \quad f_{sw} = 250 \text{ kHz} \]
CMOS Hardware Ckt Cells: (1) DPWM

- Ring-MUX scheme
- 5-bit DPWM hardware + 5-bit digital dither
- 1 µA at 600 kHz PFM sampling frequency
- 0.015 sq. mm in 0.25 micron CMOS
(2) Ring-ADC Architecture

- $\Delta V \rightarrow \Delta I \rightarrow \Delta f \rightarrow D_e$
- Windowed quantization range
- Insensitive to switching noise
- Digital block synthesizable

- Automatic monotonicity
- Wide Vo operating range
- 16 mV/step, 80 mV window, 0.15mm$^2$ in 0.25 µm CMOS
Application Example: Handset Power Management

Battery

\[ V_{in}: 5.5-2.8 \text{ V} \]

Buck converter system

\[ V_x, L, C \]

Controller

\[ V_{ref} \]

Cellular phone chip set

\[ V_o: 1.0-1.8 \text{ V}, \text{ tolerance 2-3\%} \]

\[ I_o: 0-400 \text{ mA} \]

Ctrl (PWM)

Ctrl (PFM)
• Dual mode controller
• Digital Pulse Width Modulator (DPWM)
• Power switches, drivers
• On-chip power management – input voltage to 5.5 V
PFM Mode Diagram & Switching Behavior

- Converter discontinuous conduction
- Fixed on-time control
- Zero-DC-bias comparator for low power
Load Transient Response

Vin = 3.2 V, Vo = 1.2 V. Load step 100 mA

- PWM mode: both steady-state voltages in ADC zero-error bin
- PFM mode: voltage ripple <25mV @100 mA
Efficiency: PWM and PFM Modes

- PWM efficiency drops off at low $I_o$
- PFM efficiency high at low $I_o$
- Composite efficiency high over wide $I_o$ range

$V_{in} = 4.5$ V
$V_o = 1.5$ V
Advanced Functions: Multi-mode & On-Line Optimizing Control

Discontinuous Conduction Mode

Continuous

<table>
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<tr>
<td>Pulse Skip.</td>
<td>Fixed Freq.</td>
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Discontinuous Conduction Mode

Continuous

Variable switching frequency

Control switch

Synchronous rectifier

PID control

Control switch

Synchronous rectifier

Adaptive power-minimization control

Continuous

Variable switching frequency

Control switch

Synchronous rectifier

Adaptive power-minimization control
Discontinuous Conduction Mode at Light Load

- Efficient operation over wide load range critical to battery life in mobile applications
- Turn synch. rectifier off when inductor current crosses zero
- Higher efficiency due to reduced rms current

![Diagram showing control switch, synch. rectifier, inductor current, and avg load current]
Synch. Rect. Turn-off Timing
Synch. Rect. Turn-off Timing (light load data range)

- Local minimum due to resonant switching
- Continuous cond. mode
- Discontinuous cond. mode
- Synch. rect. on
- Force synch. rect. off
- Synch. rect. off
Synch. Rect. Turn-on Timing
Synchronous Rectifier Timing Adaptation

- Synch. rect. timing as function of load current is adjusted to minimize power loss
Summary

- See www-power.eecs.berkeley.edu for pubs and more details;
- Fundamental issues addressed: quantization resolution, sampling, limit cycling
- Low-power, robust CMOS analog-digital interface
- More than 3-fold quiescent current reduction for portable applications
- Power management function integrated in low-voltage CMOS process
- Enables tunable, programmable compensator, direct communication with digital systems, etc